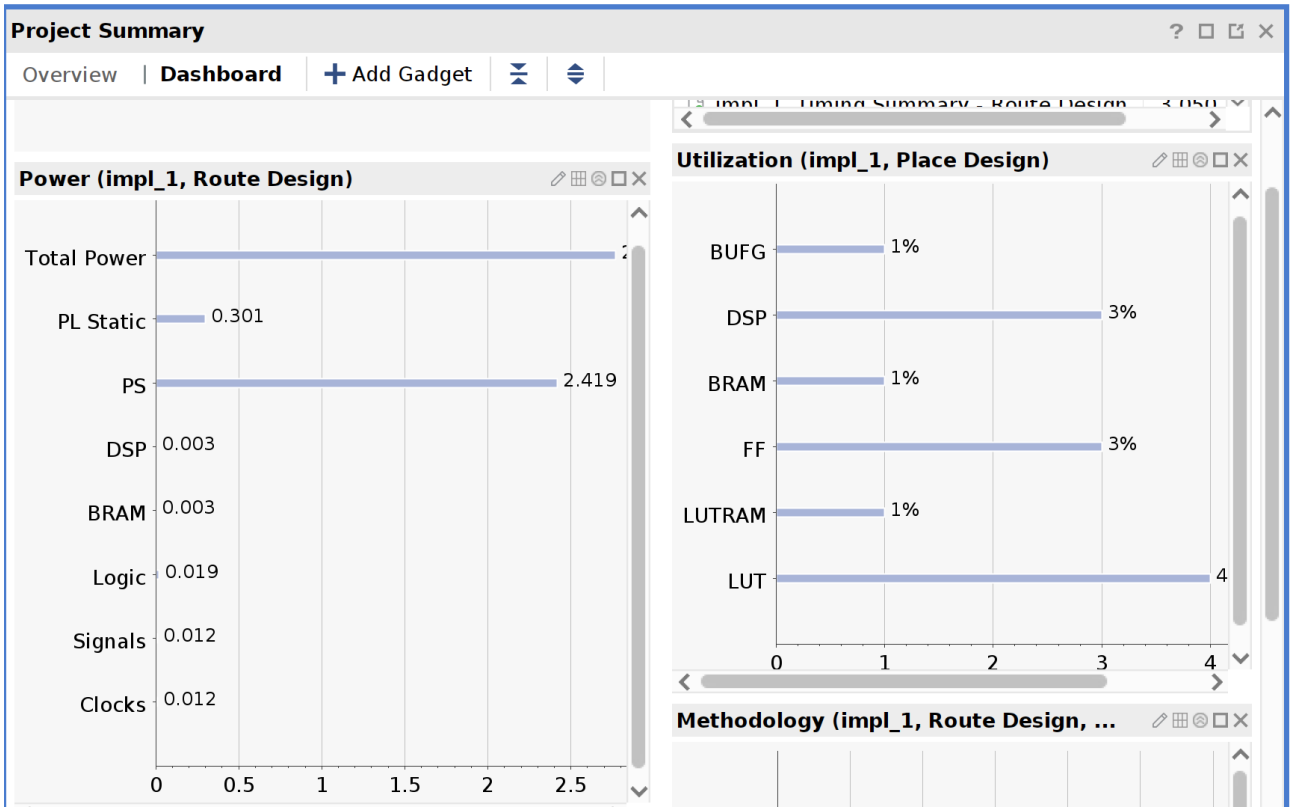
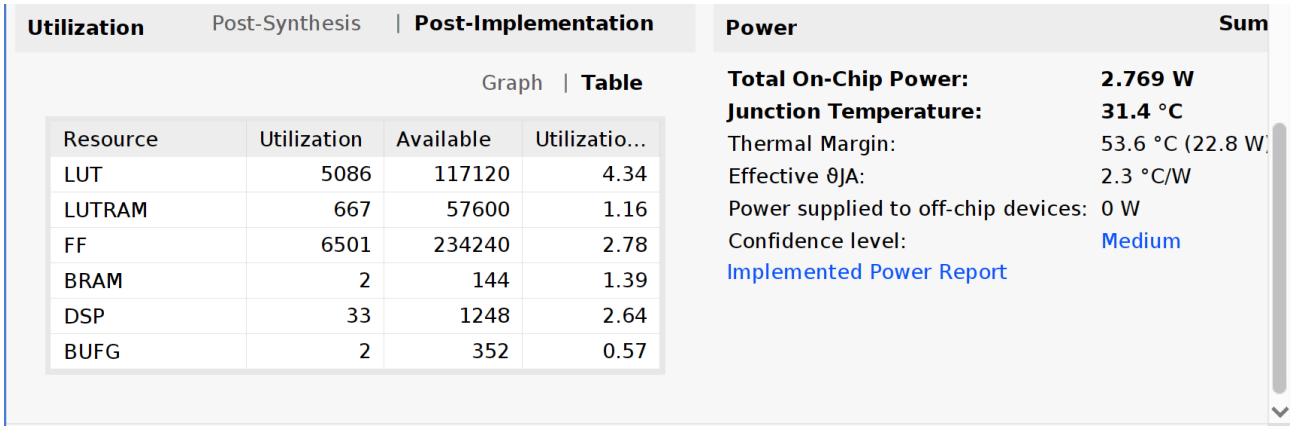
1.
It is a FIR system with a buffer to store the values if they arrive the module before been handled. In this lab, professor and TAs provide two different way to connect the module to the cpu system. One is MAXI and the other is Stream. Following would compare the performance and other factors that shows the difference between utilization of AXI and Stream.

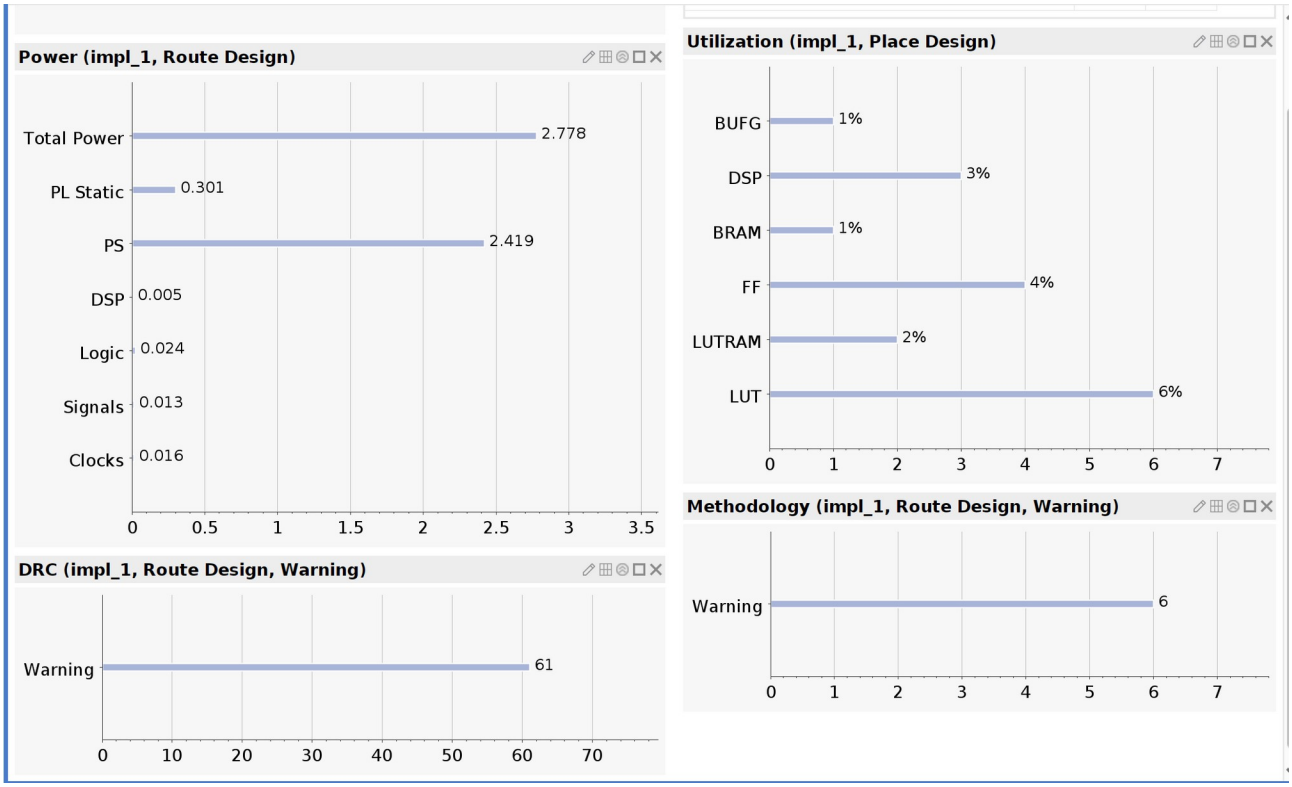
2. Scream shot

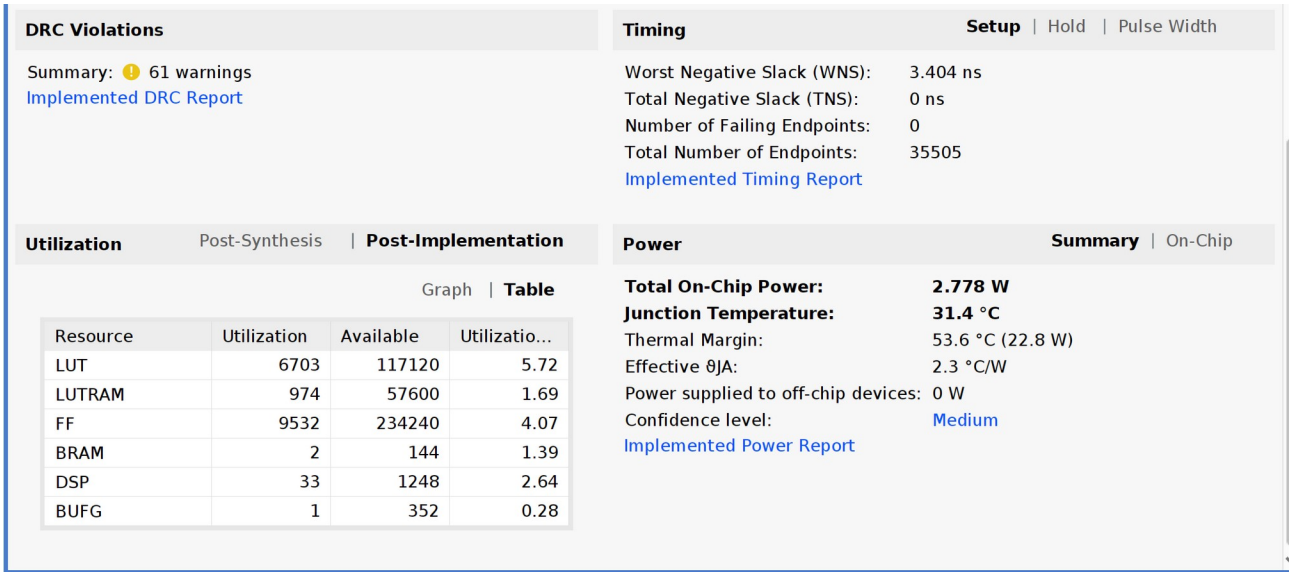
(1-1). Utilization of MAXI





(1-2). Utilization of Stream





DRC Violations

Summary: 61 warnings
Implemented DRC Report

Timing — **Setup** | Hold | Pulse Width

Worst Negative Slack (WNS):	3.404 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	35505

Implemented Timing Report

Utilization — Post-Synthesis | **Post-Implementation**

Graph | **Table**

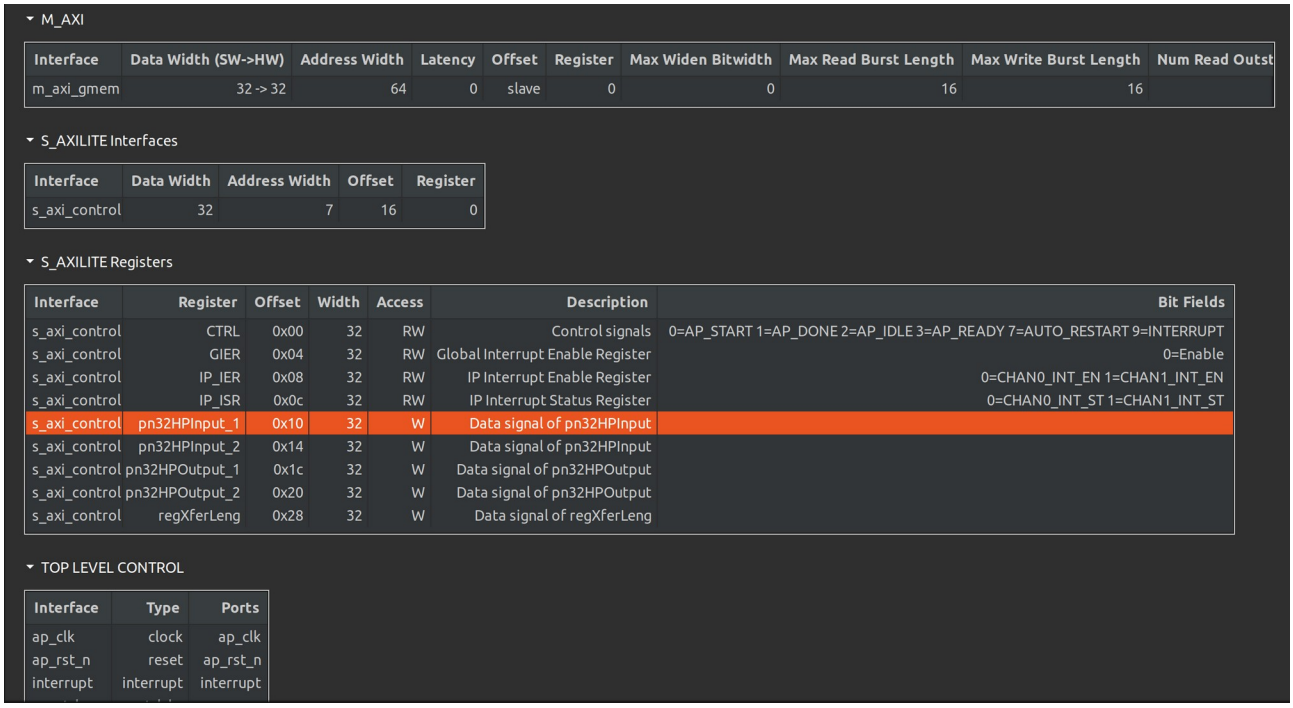
Resource	Utilization	Available	Utilizatio...
LUT	6703	117120	5.72
LUTRAM	974	57600	1.69
FF	9532	234240	4.07
BRAM	2	144	1.39
DSP	33	1248	2.64
BUFG	1	352	0.28

Power — **Summary** | On-Chip

Total On-Chip Power:	**2.778 W**
Junction Temperature:	**31.4 °C**
Thermal Margin:	53.6 °C (22.8 W)
Effective θJA:	2.3 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Medium

Implemented Power Report

(2-1) Hardware interface of MAXI



M_AXI

Interface	Data Width (SW->HW)	Address Width	Latency	Offset	Register	Max Widen Bitwidth	Max Read Burst Length	Max Write Burst Length	Num Read Outst
m_axi_gmem	32 -> 32	64	0	slave	0	0	16	16	

S_AXILITE Interfaces

Interface	Data Width	Address Width	Offset	Register
s_axi_control	32	7	16	0

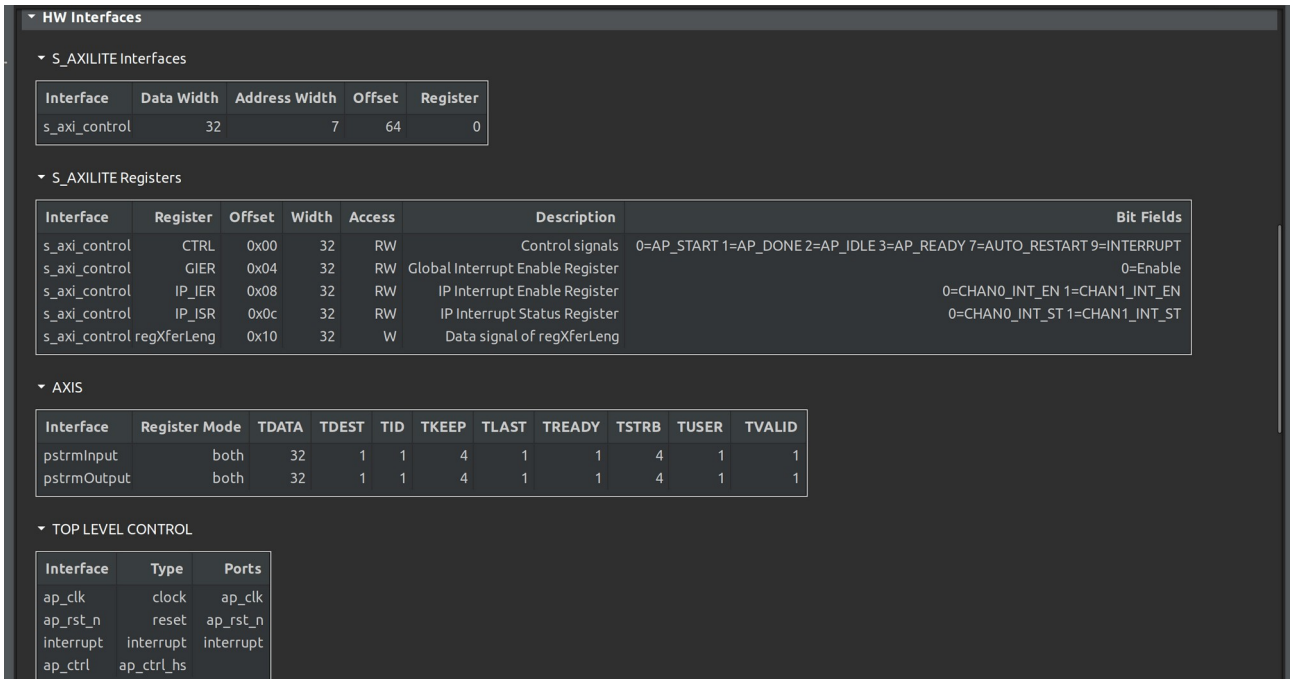
S_AXILITE Registers

Interface	Register	Offset	Width	Access	Description	Bit Fields
s_axi_control	CTRL	0x00	32	RW	Control signals	0=AP_START 1=AP_DONE 2=AP_IDLE 3=AP_READY 7=AUTO_RESTART 9=INTERRUPT
s_axi_control	GIER	0x04	32	RW	Global Interrupt Enable Register	0=Enable
s_axi_control	IP_IER	0x08	32	RW	IP Interrupt Enable Register	0=CHAN0_INT_EN 1=CHAN1_INT_EN
s_axi_control	IP_ISR	0x0c	32	RW	IP Interrupt Status Register	0=CHAN0_INT_ST 1=CHAN1_INT_ST
s_axi_control	pn32HPInput_1	0x10	32	W	Data signal of pn32HPInput	
s_axi_control	pn32HPInput_2	0x14	32	W	Data signal of pn32HPInput	
s_axi_control	pn32HPOutput_1	0x1c	32	W	Data signal of pn32HPOutput	
s_axi_control	pn32HPOutput_2	0x20	32	W	Data signal of pn32HPOutput	
s_axi_control	regXferLeng	0x28	32	W	Data signal of regXferLeng	

TOP LEVEL CONTROL

Interface	Type	Ports
ap_clk	clock	ap_clk
ap_rst_n	reset	ap_rst_n
interrupt	interrupt	interrupt

(2-2) Hardware Interface of Stream



HW Interfaces

S_AXILITE Interfaces

Interface	Data Width	Address Width	Offset	Register
s_axi_control	32	7	64	0

S_AXILITE Registers

Interface	Register	Offset	Width	Access	Description	Bit Fields
s_axi_control	CTRL	0x00	32	RW	Control signals	0=AP_START 1=AP_DONE 2=AP_IDLE 3=AP_READY 7=AUTO_RESTART 9=INTERRUPT
s_axi_control	GIER	0x04	32	RW	Global Interrupt Enable Register	0=Enable
s_axi_control	IP_IER	0x08	32	RW	IP Interrupt Enable Register	0=CHAN0_INT_EN 1=CHAN1_INT_EN
s_axi_control	IP_ISR	0x0c	32	RW	IP Interrupt Status Register	0=CHAN0_INT_ST 1=CHAN1_INT_ST
s_axi_control	regXferLeng	0x10	32	W	Data signal of regXferLeng	

AXIS

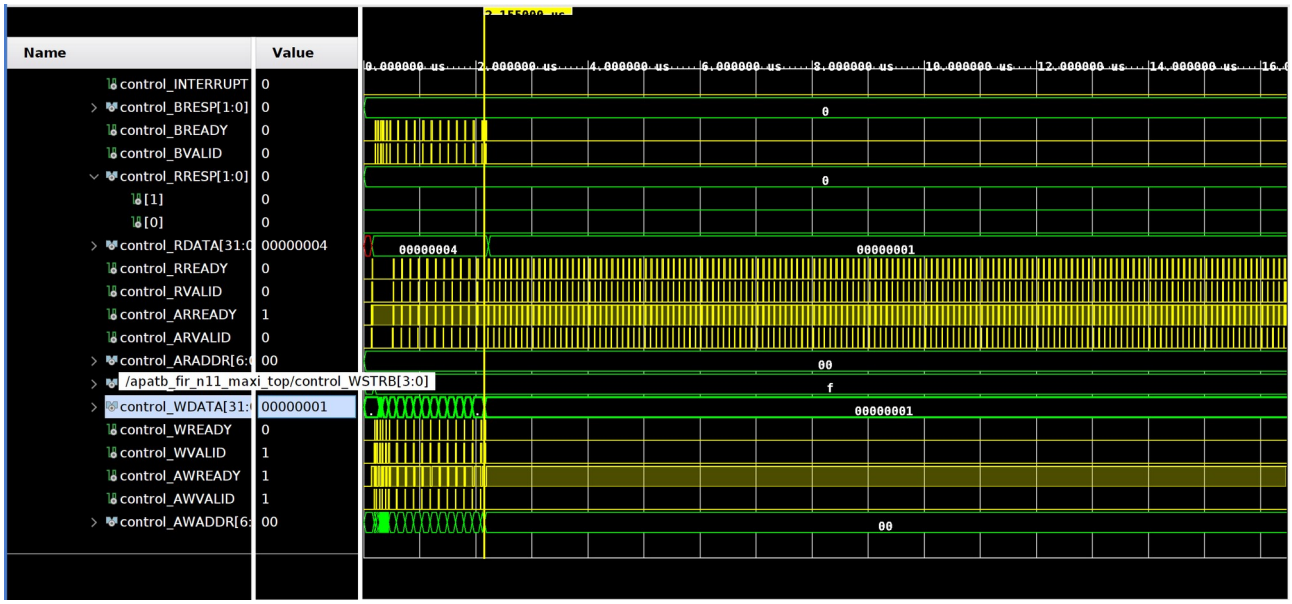
Interface	Register Mode	TDATA	TDEST	TID	TKEEP	TLAST	TREADY	TSTRB	TUSER	TVALID
pstrmInput	both	32	1	1	4	1	1	4	1	1
pstrmOutput	both	32	1	1	4	1	1	4	1	1

TOP LEVEL CONTROL

Interface	Type	Ports
ap_clk	clock	ap_clk
ap_rst_n	reset	ap_rst_n
interrupt	interrupt	interrupt
ap_ctrl	ap_ctrl_hs	

(3-1) Co-simulation transcript/waveform & performance of MAXI

```
## run all
////////////////////////////////////////////////////////////////////////////////
// Inter-Transaction Progress: Completed Transaction / Total Transaction
// Intra-Transaction Progress: Measured Latency / Latency Estimation * 100%
//
// RTL Simulation : "Inter-Transaction Progress" ["Intra-Transaction Progress"] @ "Simulation Time"
////////////////////////////////////////////////////////////////////////////////
// RTL Simulation : 0 / 1 [n/a] @ "125000"
// RTL Simulation : 1 / 1 [n/a] @ "19675000"
////////////////////////////////////////////////////////////////////////////////
$finish called at time : 19735 ns : File "/home/chenchingwen/Course2023/SoC/lab2/course-lab_2/hls_ip/solution1/sim/verilog/fir_n11_maxi.autotb.v" Line 438
## quit
INFO: [Common 17-206] Exiting xsim at Fri Sep 29 19:43:00 2023...
INFO: [COSIM 212-316] Starting C post checking ...
>> Start test!
>> Comparing against output data...
>> Test passed!
-----------------------
INFO: [COSIM 212-1000] *** C/RTL co-simulation finished: PASS ***
INFO: [COSIM 212-211] II is measurable only when transaction number is greater than 1 in RTL simulation. Otherwise, they will be marked as all NA. If user wants
INFO: [HLS 200-111] Finished Command cosim_design CPU user time: 13.33 seconds. CPU system time: 1.87 seconds. Elapsed time: 14.01 seconds; current allocated mem
INFO: [HLS 200-112] Total CPU user time: 14.77 seconds. Total CPU system time: 2.39 seconds. Total elapsed time: 26.12 seconds; peak allocated memory: 772.504 MB
Finished C/RTL cosimulation.
```



(3-2) Co-simulation transcript/waveform &performance of Stream

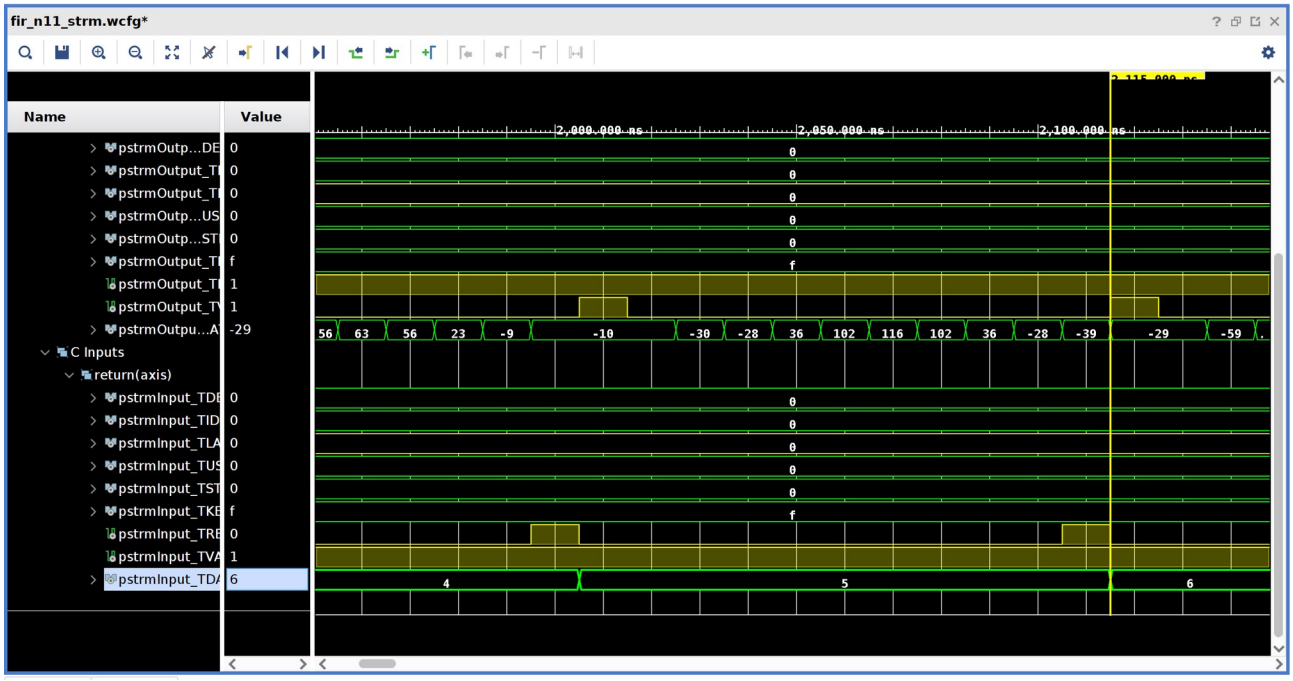
Synthesis Summary(solution1) FIR.cpp Co-simulation Report(solution1) ×

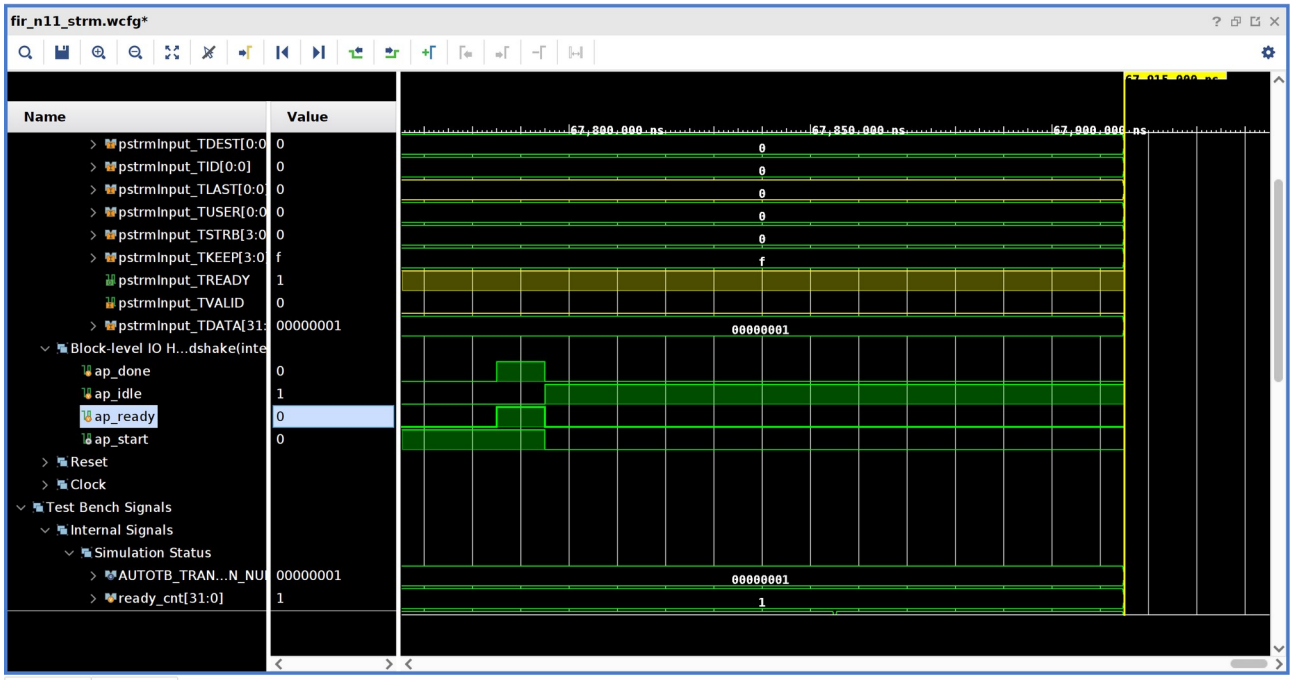
Modules & Loops	Avg II	Max II	Min II	Avg Latency	Max Latency	Min Latency
fir_n11_strm				6603	6603	6603
fir_n11_strm_Pipeline_XFER_LOOP				6600	6600	6600

Console × Errors Warnings Guidance Properties Man Pages Git Repositories

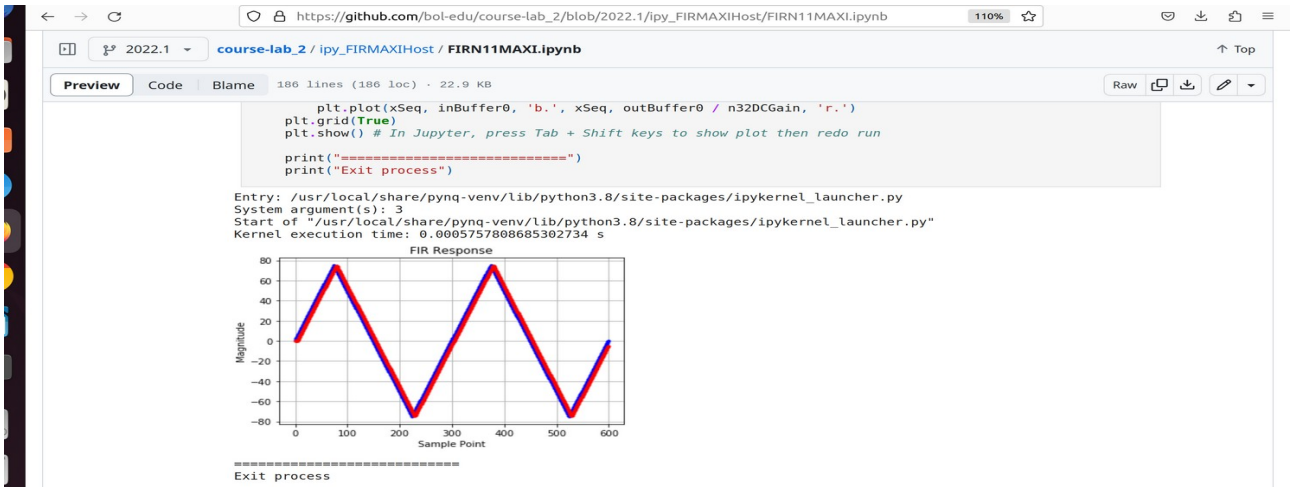
Vitis HLS Console

```
## add_wave /apatb_fir_n11_strm_top/pstrmInput_TVALID -into $tb_return_group -color #ffff00 -radix hex
## add_wave /apatb_fir_n11_strm_top/pstrmInput_TDATA -into $tb_return_group -radix hex
## save_wave_config fir_n11_strm.wcfg
## run all
////////////////////////////////////////////////////////////////////////////////
// Inter-Transaction Progress: Completed Transaction / Total Transaction
// Intra-Transaction Progress: Measured Latency / Latency Estimation * 100%
//
// RTL Simulation : "Inter-Transaction Progress" ["Intra-Transaction Progress"] @ "Simulation Time"
////////////////////////////////////////////////////////////////////////////////
// RTL Simulation : 0 / 1 [n/a] @ "125000"
// RTL Simulation : 1 / 1 [n/a] @ "67855000"
////////////////////////////////////////////////////////////////////////////////
$finish called at time : 67915 ns : File "/home/chenchingwen/Course2023/SoC/lab2/course-lab_2/hls_ip_stream/solution1/sim/verilog/fir_n11_
## quit
INFO: [Common 17-206] Exiting xsim at Fri Sep 29 20:26:59 2023...
INFO: [COSIM 212-316] Starting C post checking ...
>> Start test!
>> Comparing against output data...
>> Test passed!
-----------------------
INFO [HLS SIM]: The maximum depth reached by any hls::stream() instance in the design is 600
INFO: [COSIM 212-1000] *** C/RTL co-simulation finished: PASS ***
INFO: [COSIM 212-211] II is measurable only when transaction number is greater than 1 in RTL simulation. Otherwise, they will be marked as
INFO: [HLS 200-111] Finished Command cosim_design CPU user time: 16.18 seconds. CPU system time: 2.72 seconds. Elapsed time: 17.8 seconds;
INFO: [HLS 200-112] Total CPU user time: 17.64 seconds. Total CPU system time: 3.05 seconds. Total elapsed time: 29.76 seconds; peak alloc
Finished C/RTL cosimulation.
```

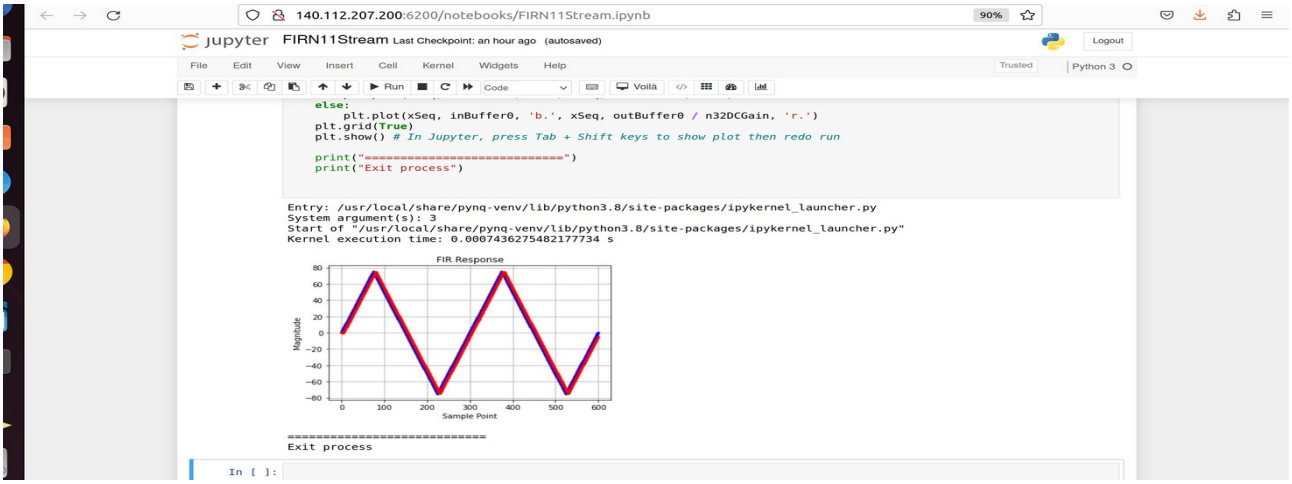




(4-1) jupyter notebook result for MAXI



(4-2) jupyter notebook result for Stream



5. Observations

(1). Utilization: Stream method consumes more resources(LUT, FF, etc) than MAXI one.
(2). Execution time: Stream version consumes about 0.00075s while MAXI version consumes 0.00058s

Base on above observation, We can conclude that the MAXI version is a better choice with respect to the resource utilization(power consumption) and execution time.