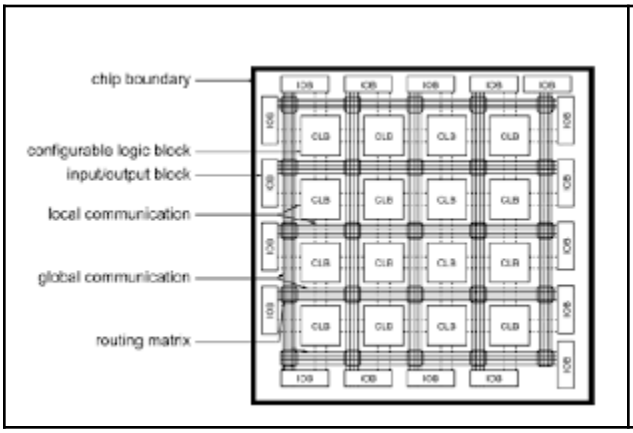


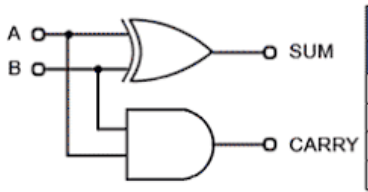


Table 4.1.1

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

FPGA concepts: digital logic

1. Half Adder
2. Full Adder
3. Ripple Carry Adder (RCA)
4. Multiplexer (MUX)
5. 7 Segment display decoder
6. Linear Feedback Shift register (LFSR)
7. Register-Based FIFO
8. UART

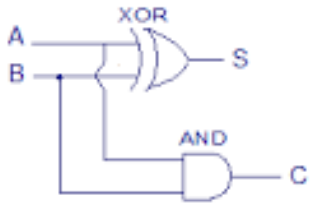
Half Adder

- Adds two single-bit binary numbers.
- Produces outputs: SUM (XOR of inputs) and CARRY (AND of inputs).
- Fundamental building block for larger arithmetic circuits such as adders, ALUs, and processors.

Inputs		Outputs	
A	B	S	C
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

Truth table

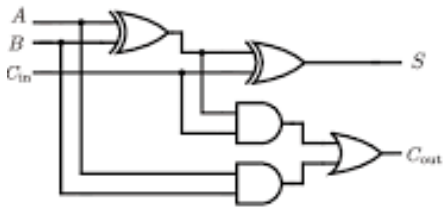
Schematic



Realization

Full Adder

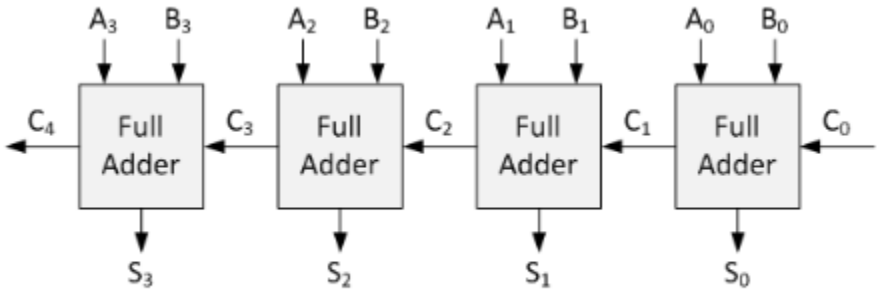
- Extends the half adder by including a carry-in input.
- Enables chaining of multiple adders to add multi-bit numbers.
- Backbone of multi-bit adders, multipliers, and arithmetic logic units (ALUs).



Inputs			Outputs	
A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Ripple Carry Adder (RCA)

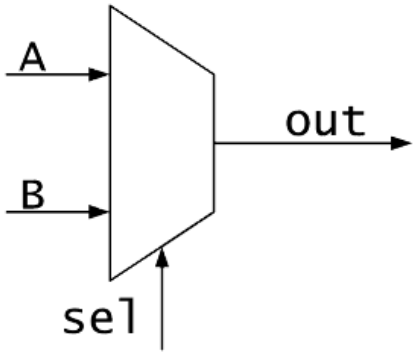
- Chains together multiple full adders to create a multi-bit adder.
- Carry-out of one stage feeds into the carry-in of the next stage.
- Simple implementation often used in FPGA-based processors and signal-processing blocks.



Ripple Carry Adder (4-bit) Block Diagram

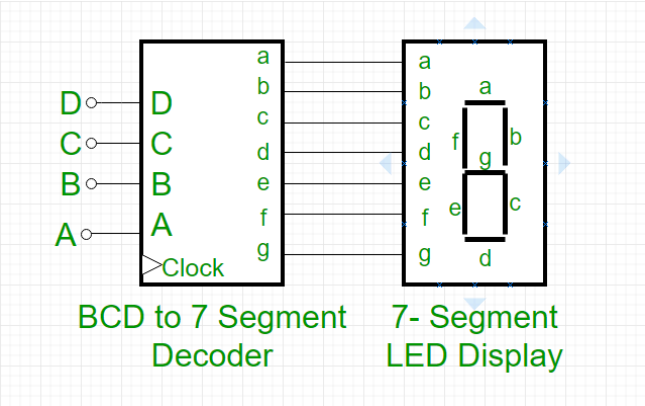
Multiplexer (MUX)

- Digital switch that selects one of many inputs based on select signals.
- Commonly used to control data paths, state transitions, and resource sharing.
- Optimized into lookup tables (LUTs), the core configurable logic elements inside FPGAs.



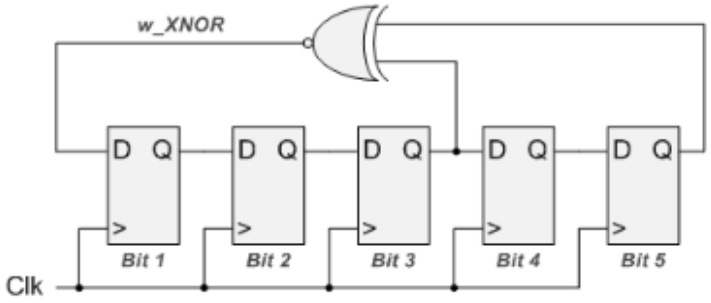
7-Segment Display Decoder

- Converts 4-bit binary or hexadecimal input into signals that drive a 7-segment display.
- Displays numbers 0–9 and letters A–F in a human-readable format.
- Useful for counters, timers, and debugging FPGA projects with visual output.



Linear Feedback Shift Register (LFSR)

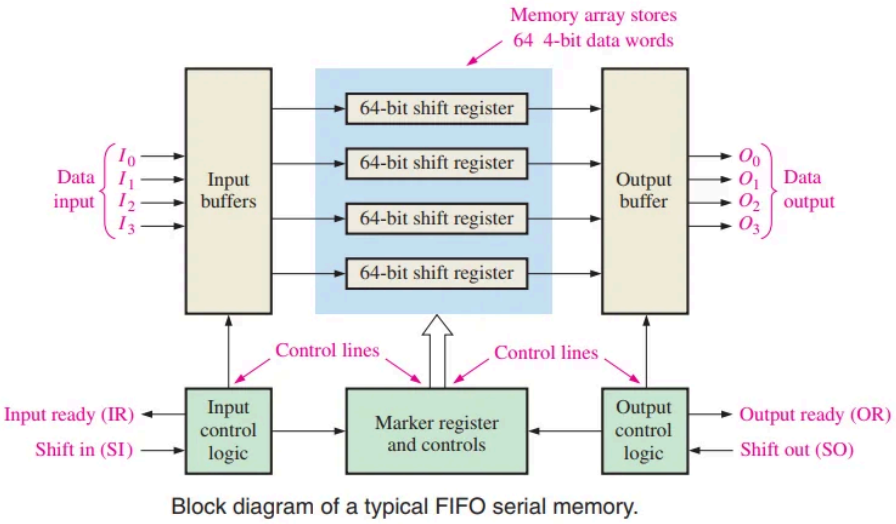
- Shift register where the new input bit is generated by XORing certain “tap” positions.
- Produces a pseudo-random binary sequence.
- Used in random number generation, error detection (CRC), and signal scrambling.



5-Bit LFSR using XNOR gates

Register-Based FIFO

- Buffer that temporarily stores data in first-in, first-out order.
- Uses registers, head/tail pointers, and flags like FULL and EMPTY.
- Essential for data buffering, clock domain crossing, and reliable communication between subsystems.



Block diagram of a typical FIFO serial memory.

UART (Universal Asynchronous Receiver-Transmitter)

- Serial communication protocol that transmits data one bit at a time.
- Frames data with start and stop bits, enabling communication without a shared clock.
- Common FPGA I/O interface for PC-to-FPGA or device-to-device communication.