**ASSINGMENT # 01**

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1) **Data-Level Parallelism(DLP)** arises because there are many data items that can be operated on at the same time.

2) **Task-Level Parallelism(TLP)** arises because tasks of work are created that can operate independently and largely in parallel.

3) Instruction Level Parallelism (ILP): ILP exploits **data-level parallelism** at modest levels with compiler help using ideas like **pipelining** and at medium levels using ideas like speculative **execution**.

4)  Improvement through **architecture changes** 7x slower computers if only relied on technological improvements.

5)  Intel joined **IBM** and **SUN** in declaring that High Performance can be achieved through **multiple** processors on a single chip, rather than a **single Uni** processor.

6)  ILP generally exploited through **compiler** or **hardware** (Programmer need not be concerned).

7) TLP (Thread Level Parallelism) and DLP (Data Level Parallelism) must be exploited by **programmer.**

8) Prior to mid-1980s, performance was mainly achieved through **technological** improvement.

9) **PMDs**   applies to the collection of wireless devices with multimedia user interfaces like cell phones, tablets etc.

10) **supercomputers** differ by emphasizing floating point performance and by running large, communication, intensive batch programs that can run for week at a time

11) **Parallelism**  at multiple levels is now the driving force of computer design.

12) **Energy** and **cost** are primary constraints.

13) **Pentium 4** and **Mobile Pentium 4** both offer , different clock rates ,different memory systems, making more effective for low –end computers.

14) **Thread-Level Parallelism** exploit either data level parallelism or task-level parallelism in a tightly coupled hardware model that allows for interaction among parallel treads.

15) **Request-Level Parallelism** exploit parallelism among largely decoupled tasks specified by the programmer or the operating system.

16)  Two processors with same ISA and almost same organization, but different hardware are

**AMD** **Opteron 64** and **Intel Pentium 4**.

17) **WSCs** emphasize interactive **applications**, large-scale **storage**, dependability, and high Internet bandwidth.

18) The largest of the clusters are called **warehouse-scale** computers. In that they are designed so that tens of thousands of servers can act as one

19) Due to **compilers** and **OS** new architectures get better acceptance in the market.

20) **Reduced Instruction** Set Computer architectures were proposed in early 1980s.

21) Elimination of architecture dependent **assemblers** through high level languages and their compilers.

22)  Major focus of RISC architectures is on exploitation of  **ILP**  through pipeliningand **multiple** instruction issue.

23) Efficient use of **Cache** Sophisticated organization and optimization of **cache**.

24) Standardized, **vendor-independent** OS reduced the cost and risk of launching a new **architecture**.

25) **Intel** adapted many innovations that were pioneered by **RISC designs**.