**PROJECT REPORT**

**Design Verification Essentials Training 2022**

**Title**

**AHB LITE PROTOCOL DUT**

**Project 3**

**Group members**

1. Muhammad Saqib Saif
2. Arlan Shafique
3. Saleem Raza
4. Muhammad Basit

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# **Introduction**

The task was given to us for verification of a design which was working on AHB-lite protocol before this we were able to verify some functionality of a design which was working on the same protocol. The design documents were given to us with the specification document. Total 4 of the group members we were and the team lead was M Saqib Saif, work was divided into 4 members as in the Table 1 .1 Individual Tasks, Posts and learnings.

## **Methodology**

The procedure we followed was a little simple we gathered all the material in one place and ordered it according to the importance of the documents. We first have to understand the design features. Meanwhile, we have to connect the DUT to testbench and in the meanwhile, we have to write the different test schemes for our dut testing. With all these things in parallel, we have to plan the code coverage as well. We divided the tasks according to the expertise of the team members. Design understanding feature understanding and document review were up to Arslan meanwhile he was joining the DUT with testbench as this will help him in better understanding of dut working as our testbench was already written and tested in projects 1 and 2 so we have to join our new dut to our previous testbench. Saleem was given the task of managing the monitor class so that he will be able to understand the working of the monitor and the interface of **DUT** with the testbench on the monitor side. Basit was given the task of understanding the testbench scoreboard so that if there is any kind of change, we want to do he would be able to do that. Me as a team lead was monitoring all the work and was writing some different stimuli we have to apply on the DUT and managing the Generator and driver for good test generation. We had to perform the directed test with the **burst**, random Test with **burst**. When all the members were full on set on their given individual tasks, we joined all the things together for creating a full-on DUT verification environment.

## **Individual Workings**

**Table 1.1 Individual Tasks, Posts and learnings**

|  |  |  |  |
| --- | --- | --- | --- |
| **Name** | **Post** | **Tasks** | **Learning** |
| **M Saqib Saif** | *Lead* | 1. Manage the Team and take the project to completion 2. Generating Stimulus and driving it to DUT 3. Overall whole tasks progress and working of other members 4. Helping other members in completing their tasks as well 5. If group is stuck in any situation getting help from other group team leads 6. Overall make the environment working | 1. Managing the Team 2. Collaboration with others 3. Making the Test bench general 4. Resolving Problems 5. How to let others to be comfortable to work with me |
| **Arsalan Shafique** | *Designer* | 1. He has the expertise in designing as well as verification so we decided to give him the design side works 2. He had to join the DUT to testbench 3. He had to understand the full working of DUT and its specification document 4. He was a vice team lead 5. He had to manage the monitor class | 1. He was able to understand the design well and tell others about design specs 2. He was able to understand the joining of DUT 3. He was able to learn the working of monitor and team work |
| **Saleem Raza** | *Viewer / Inspector* | 1. He had to manage the scoreboard 2. Code coverage 3. Completing the project 1 | 1. Able to complete the project 1 2. Able to accurately manage the scoreboard 3. Code coverage |
| **M Basit** | *Viewer* | 1. He had to understand all the working procedures 2. He had to complete the project 1 3. He had to understand the basic concept on verification environment | 1. Completed the project 1 2. Learned the full working of Layered test bench 3. Understood the basic hierarchy of verification environment |

# Summary

The project was about the verification of a DUT given which is working on AHBlite protocol. Testbench was already written due to previous project 1. We have to use that testbench for the new DUT so that we will understand the working of a generalized testbench. The tests were conducted and we were able to devise that DUT was unable to give results on Burst as devised in the specification document. Which according to our point of view the BUG is. We were able to perform the following tests

1. Random test with zero burst
2. Random test with single burst
3. Random test with incremented burst
4. Directed test with zero burst
5. Directed test with single burst
6. Directed test with incremented burst

At last, we all were able to fully understand the working of layer test bench and how to make it generalized for different DUTs of same protocol. All members worked very hard as UVM was also started besides the project.

NOTE : : Project GOOGLE drive link : : https://drive.google.com/file/d/1f2NOttld\_LXizpRlegH9Fu0Vh8eBTdWW/view?usp=sharing

EDA playground link : :

https://edaplayground.com/x/mXV5