ENERGY EFFICIENT 6T SRAM FOR MULTIMEDIA APPLICATIONS

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ABSTRACT

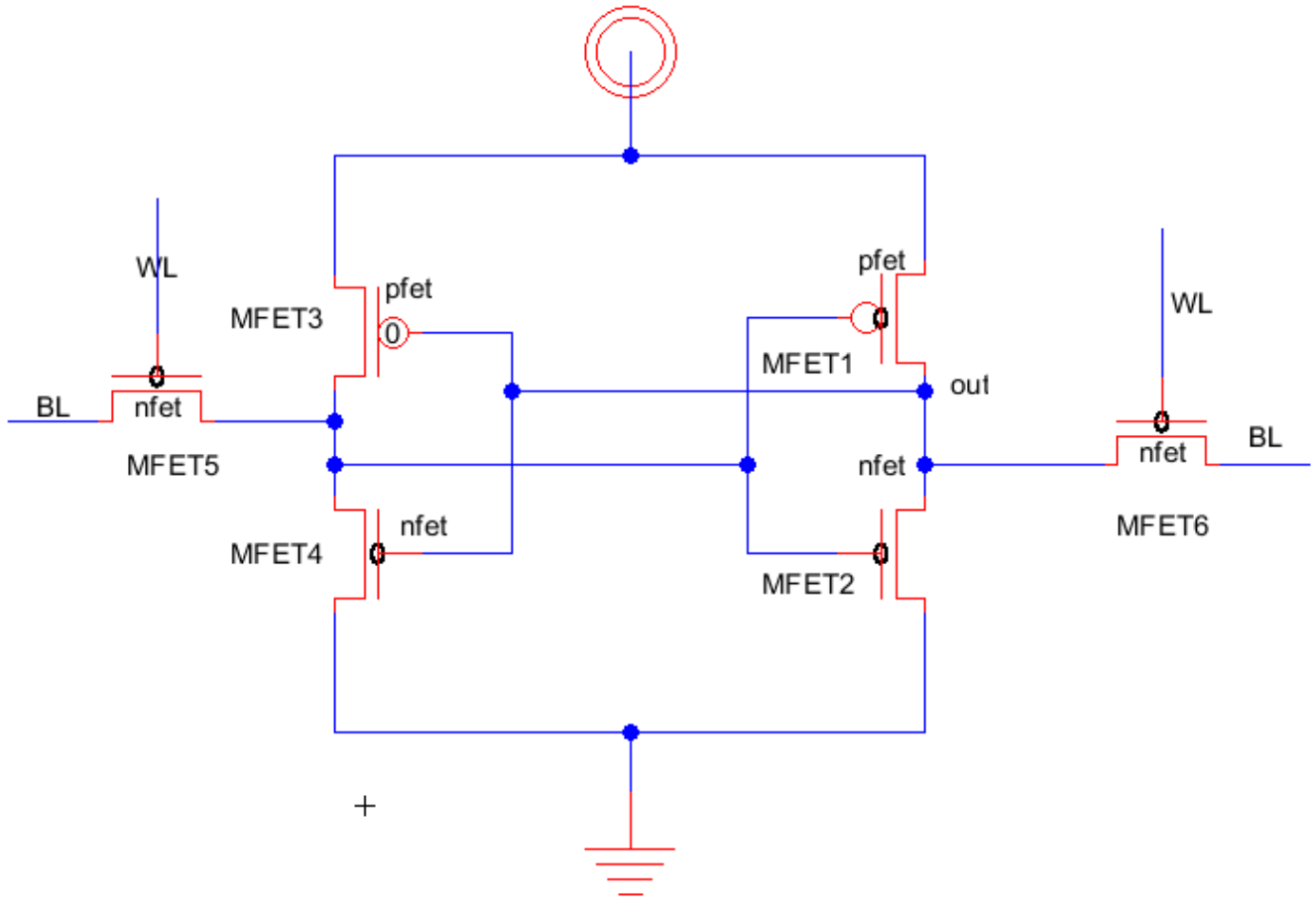
- An aggressive scaling of the technology and the increasing the number of the transistor counts are the major challenge of the design of the Integrated Circuit (IC). Nowadays data storage is gaining more importance in human life.
- All electronic and digital devices need memory for reducing the power consumption. The concept of “more data in less space” is useful for increasing the system performance and overall system efficiency. Generally we used semiconductor memory as “SRAM”. SRAM can be abbreviated “Static Random Access Memory”.
- Many VLSI chip can have SRAM memory because of their large storage capacity and fast accessing time. Where, the word static indicates that it does not need to be habitually refreshed but the DRAM need habitually refreshed.
- DRAM can be abbreviated as “Dynamic Random Access Memory” which is another type of memory. Both the memories can be classified from “Random Access Memory: (RAM). The power analysis of 6 transistor SRAM is compared with existing circuit.

INTRODUCTION

Nowadays one of the widely used electronic device or electronic circuit is SRAM. Stability in SRAM when designed using the Complementary Metal–Oxide– Semiconductor (CMOS) technologies generally depend on the SNM. SRAM memory technology is used because of its speed and robustness. As the device is scaled down in sizes several design challenges arise in the nanometer size SRAM design. In an SRAM cell operation generally supply voltage scaling is performed.

EXISTING METHOD

6T SRAM:

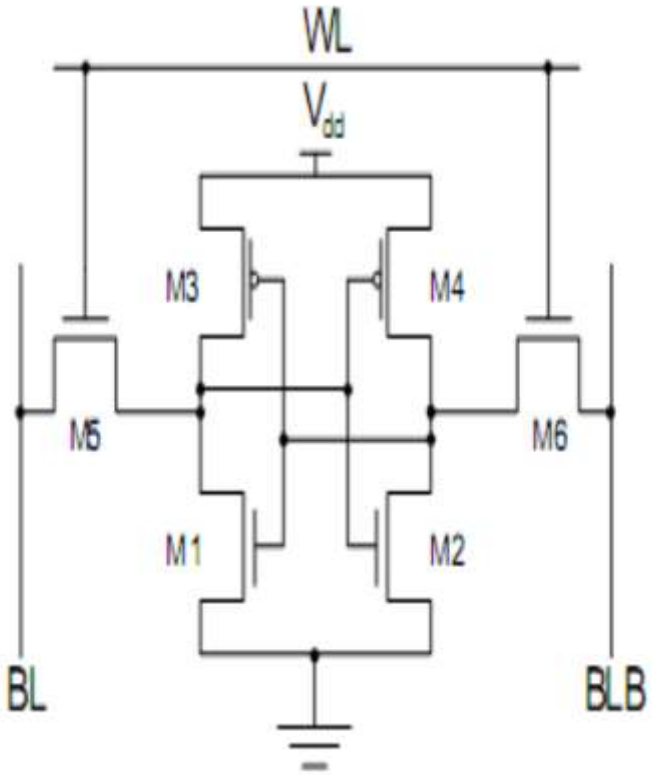


ANALYSIS

Circuits	Area (nm^2)	Power (W)	Current (A)	Delay (nS)
6T-SRAM - Read	2160	328.74n	365.26n	0.20
6T-SRAM - write	2160	203.16u	225.74u	0.16

PROPOSED METHOD

Advanced technologies are unfortunately affected by a number of undesired side effects. Increased the level of the leakage current is one of the major reason of undesired side effect in the circuit. Hence, delay fault, higher power consumption and leakage current represent a significant challenge for the employ of current based parametric test quiescent test and all current based test methods. A more serious effect caused by high leakage current is the functionality failing of the SRAM cell, which can be modelled with data retention faults where the cell loses it is stored value due to leakage currents.



PROPOSED METHODOLOGY

- Technology used : GDPK 45nm in Cadence Virtuoso
- Tools Used : Cadence Virtuoso, ADE_L, Netlist Simulation

ALGORITHM FOR CIRCUIT DESIGN

Step-1: The GPDK 45 nm Technology launched.

Step-2: EDA-PDKs-GPDK 0.45 created.

Step-3: Path created from CDS.Lib.

Step-4: Opened the terminal window type virtuoso.

Step-5: Designed circuit drag and drop method.

Step-6: For read operation the values set in SRAM WL 0.9V, BL 0.9V and BL-BAR -0.9V.

Step-7: Save and run the circuit.

Step-8: If errors are there go back to the circuit. Check and modify the circuit.

Step-9: If no errors then launch ADE_L.

Step-10: Run time set as 20 ns for all circuits.

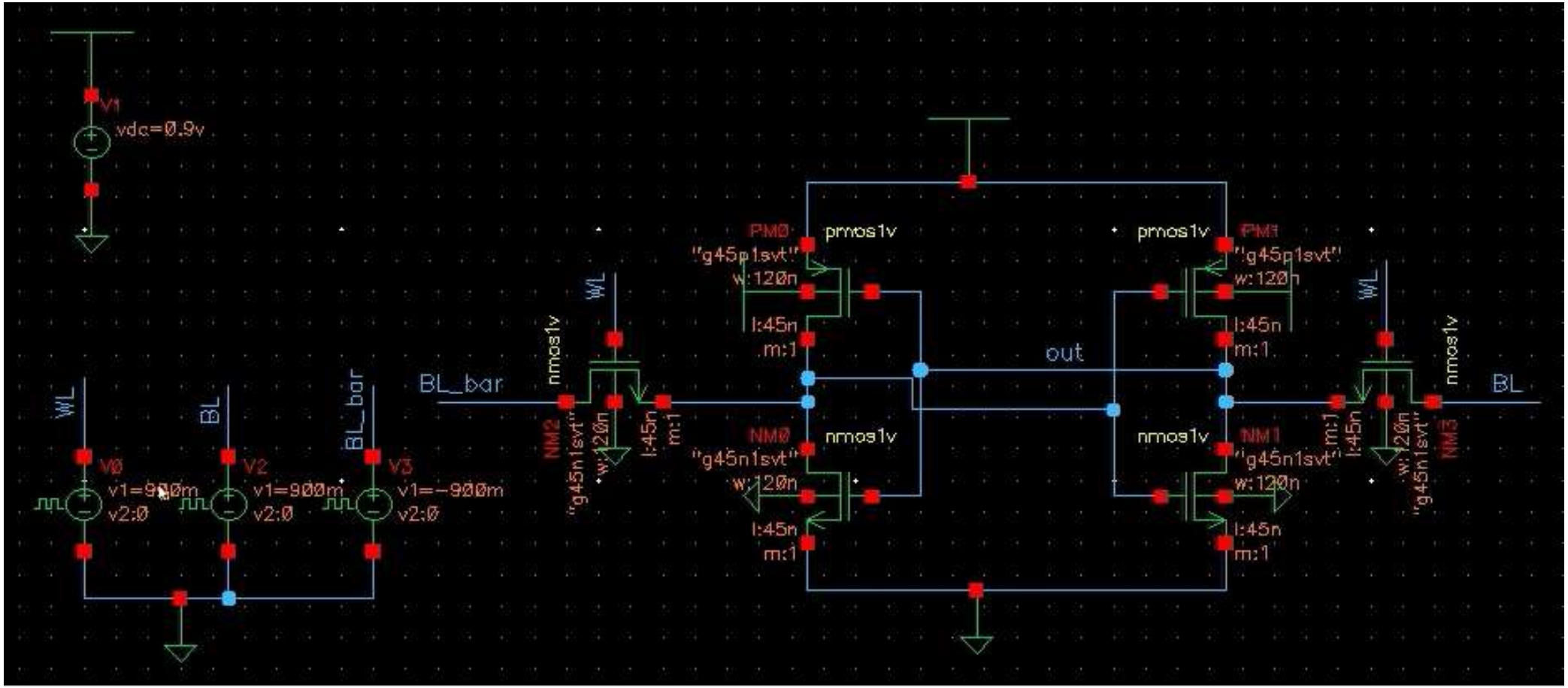
Step-11: From analyse chosen fixed transition time 20 ns.

Step-12: From output-to be plotted by selecting WL, BL, BL_BAR and OUTPUT pins from schematic diagram.

Step-13: Run the circuit from netlist.

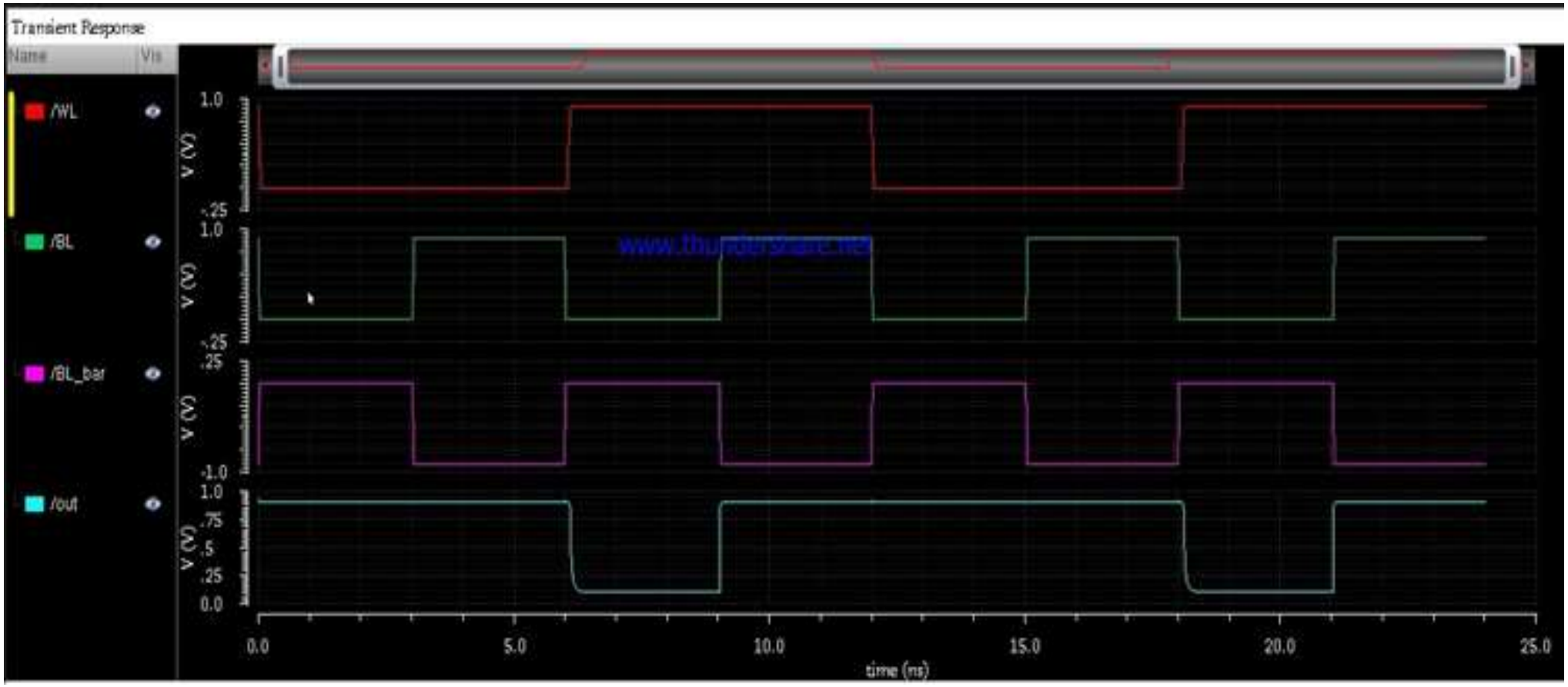
Step-14: For result analysis selected transient operating points from print and observed the supply i, pwr, v.

6T SRAM

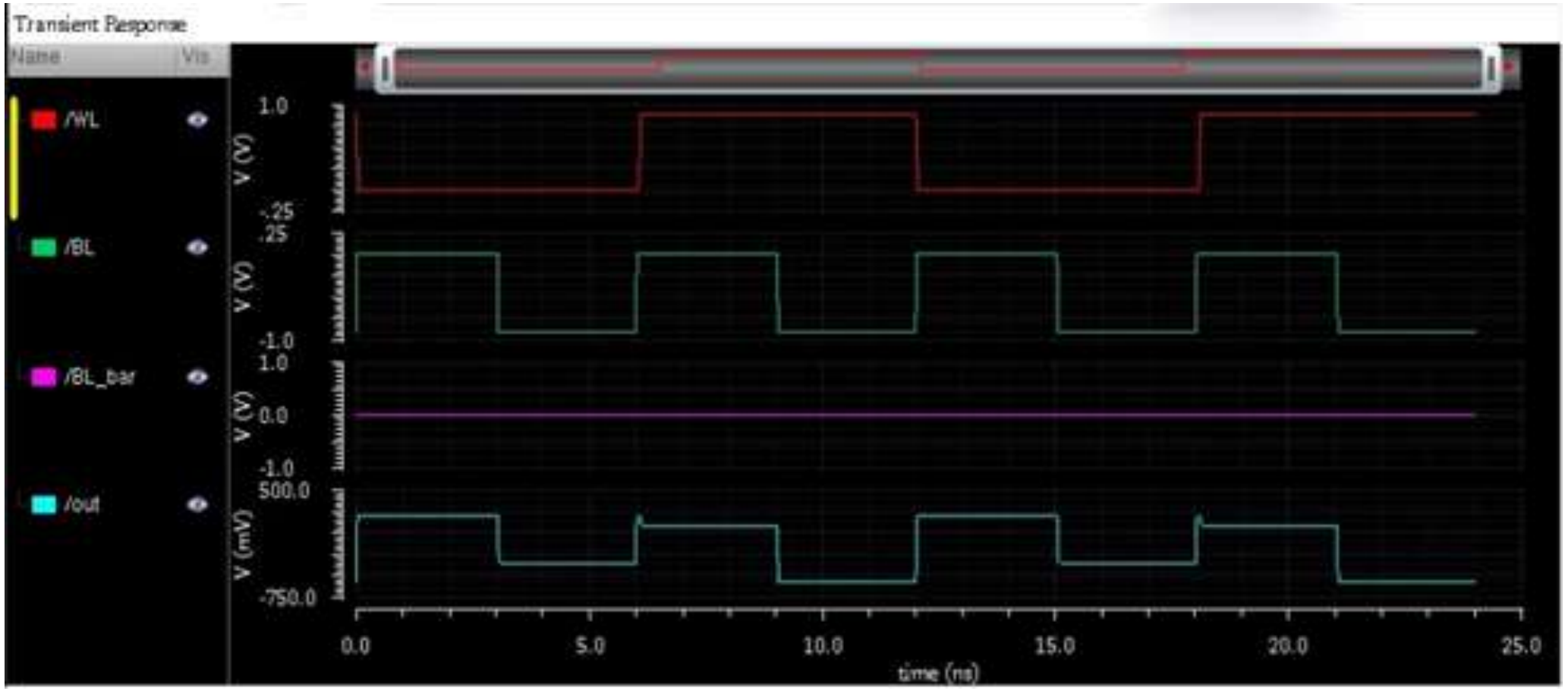

V1
vdc=0.9v
WL
BL
BL_bar
V0
v1=900m
v2:0
V2
v1=900m
v2:0
V3
v1=-900m
v2:0
BL_bar
nmos1v
WL
NM2
"g45n1svt"
w:120n
l:45n
m:1
PM0
pmos1v
"g45p1svt"
w:120n
l:45n
m:1
NM0
nmos1v
"g45n1svt"
w:120n
l:45n
m:1
out
pmos1v
PM1
"g45p1svt"
w:120n
l:45n
m:1
nmos1v
NM1
"g45n1svt"
w:120n
l:45n
m:1
WL
nmos1v
BL
NM3
"g45n1svt"
w:120n
l:45n
m:1

RESULTS

6T SRAM READ OPERATION:



6T SRAM WRITE OPERATION:



ANALYSIS

Circuits	Area (nm^2)	Power (uW)	Current (uA)	Delay (nS)
6T-SRAM - Read	32400	10.508	48.672	0.1
6T-SRAM - write	32400	75.588	31.0636	0.06

APPLICATIONS

- Digital Electronic devices with storage elements.
- Embedded Systems.
- Used in manufacturing of Processors.
- Applied in industries.

CONCLUSION

The reduced leakage current and power dissipation compared to standard 6T, makes the new approach attractive for nano scale technology regime, in which process variation is a major design constraint.

FUTURE SCOPE

Present days the digital communication plays an important role. In this digital communication systems the FIR filters using more appropriate. Present 4-tap FIR filters are designed by using D-Flip flops for storing of previous responses. Here replacing of D-flip flop with SRAM is necessary in future.

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Journal Article

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THANK YOU