Anish Saxena

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Education

Year	Academic Qualification	Institution	CGPA/%
2017-2021 (expected)	B.Tech, ME	Indian Institute of Technology, Kanpur	9.0/10.0
2017	CBSE – XII	St. Kabir School, Ahmedabad	94.4%
2015	CBSE – X	St. Kabir School, Ahmedabad	10.0/10.0

Work Experience

Intel Labs, India *Processor Architecture Research Lab*
Architecture Research Intern May 2020 - Sep. 2020

- Implemented and analyzed new and recent research ideas, improved the performance of non-inclusive cache hierarchy.
- Extended a state-of-the-art **research simulator**, collected memory traces, and performed functional cache simulations.
- **Reduced simulation time by more than 10**× and maintained greater than 99% correlation to full simulation.
- **Devised efficient implementations to track novel parameters** that affect cache policy, like reuse distance.
- Developed custom cache policies and examined performance against oracular policies like Belady for workload traces.

CAR3S Group, IIT Kanpur *Prof. Biswabandan Panda*
Group Member Apr. 2019 - Jun. 2020

- Improved accuracy of attacks that exploit instruction execution latency variation caused by processor caches.
- Identified that core frequency and OS scheduling determine latency, modelled them as functions of system noise.
- Introduced noise-aware calibration, periodic feedback, and victim profiling to optimize baseline attacks.
- **Designed and implemented DABANGG**, a novel set of refinements to efficiently incorporate optimizations.
- Conducted experiments, **mounted attacks on AES and RSA cryptosystems** in OpenSSL and GnuPG libraries.
- **First author** of the work **under submission** to the IEEE Symposium on Security and Privacy, 2021; **funded by NXP Semiconductors**; accessible at `iacr://2020/637`.

New York Office, IIT Kanpur *Prof. Manindra Agrawal*
Computer Systems Intern May 2018 - Jul. 2018

- Led a team of 4 to develop the infrastructure stack of a scalable and fault-tolerant microservice-based web portal.
- **Implemented Spinnaker from scratch** to deploy Docker images continuously and immutably to Kubernetes cluster.
- Configured the pipeline to be auto-triggered by Concourse Continuous Integration (CI) workflow for Spinnaker.
- Integrated Clair static vulnerability analysis tool to flag buggy Docker images and safely fail the build in CI stage.
- Added Canary analysis stage to the pipeline, **integrated Locust load testing framework** in this stage.

Honors and Awards

- **Semiconductor Research Corporation Member**, Sole undergraduate student in Indian Research Program
- **Aditya Birla Group Scholarship Recipient**, Awarded to 15 students from all IITs and BITS
- **KVPY Fellow**, Awarded by IISc Bangalore

Positions of Responsibility

- **Coordinator**, *Programming Club IIT Kanpur* *2019 - 2020*

Projects

Compression Algorithms for Caches *Project Member*
CAR3S Group, IIT Kanpur Jul. 2020 - present

- Mentored by Prof. Biswabandan Panda and **funded by Qualcomm Research** to improve performance of SoCs.
- Collected Memory Access Traces (MAT) to analyze patterns and design compression algorithms for cache hierarchy.
- **Extended QEMU**, the emulator used by Android Studio, collected MAT from Android 9.0 API with x86_64 ABI.
- **Modified Valgrind**, a memory profiling framework, collected MAT natively from ARMv8-A devices.
- **Extended ChampSim**, a trace-driven simulator, utilized MAT and ran fine-grained memory simulations.

Organic Grocery App *Project Manager*
Agnys Waste Management Pvt. Ltd. Jul. 2019 - Nov. 2019

- Coordinated a team of 4, developed an Android application to sell locally-sourced organic fruits and vegetables.
- Used Flutter for app development, Firebase for infrastructure, and integrated a payments mechanism.

Campus Sustainability Challenge *Team Leader*
7th Inter-IIT Tech Meet, IIT Bombay Oct. 2018 - Dec. 2018

- Led a team of 6 to propose and implement solutions for waste generated on the institute campus.
- Integrated sensors in composting drums, captured Biogas, reduced PNG consumption in hostel messes by 14%.
- Configured E-Waste Management Software to model waste generation, perform analysis, and suggest optimal solution.

E-Waste Management Software *Prof. Indranil Saha*
Course Project Aug. 2017 - Nov. 2017

- Developed in Visual C++, recorded E-Waste generation and predicted optimal combination of recycling techniques.
- **Modelled the prediction algorithm** from scratch and took economic and environmental parameters into account.
- Accurate for dataset with upto 10 million entries; accessible at `github://Anish-Saxena/E-Waste-Management/`.

Skills

Programming: C++, C, Python, Golang, Bash
Cloud: Docker, Kubernetes, Concourse, Spinnaker
Frameworks: Pthreads, OpenMP, CUDA, Locust
Utilities: Git, Vim, LaTeX, GDB, ANTLR, Valgrind, QEMU

Miscellaneous

- Delivered technical talks in CAOS Reading Group.
- Incorporated Systems Reading Group, compiled resources to familiarize one with systems concepts and research topics.
- Mentored a group of 5, implemented a 16-bit, in-order, pipelined processor in Verilog, tested it on FPGAs.
- Participated in national-level quizzes, debates, and extempores; two-time regional finalist of TCS IT Wiz Quiz.

Relevant Coursework

Programming for Performance[i]	Data Structures & Algorithms	Introduction to Programming[A]	Operating Systems[A]
Advanced Computer Architecture[i]	Computer Architecture[A*]	Topics in Operating Systems	Computer Organization[A]
Non Classical Logic	Linear Algebra	Applied Numerical Methods[i]	Multivariable Calculus

A∗: grade for exceptional performance A: grade i: in progress