

# 1. Description

## 1.1. Project

Project Name	newseqen
Board Name	custom
Generated with:	STM32CubeMX 6.6.1
Date	02/02/2023

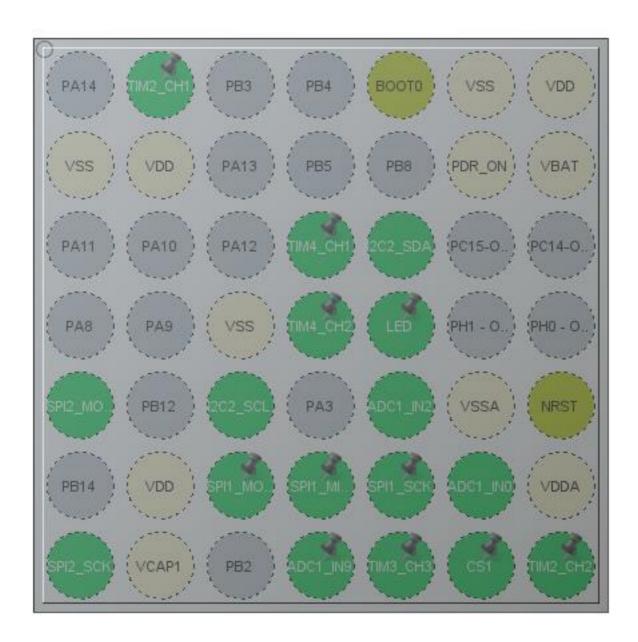
## 1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F411
MCU name	STM32F411CEYx
MCU Package	WLCSP49
MCU Pin number	49

## 1.3. Core(s) information

Core(s)	Arm Cortex-M4	

# 2. Pinout Configuration



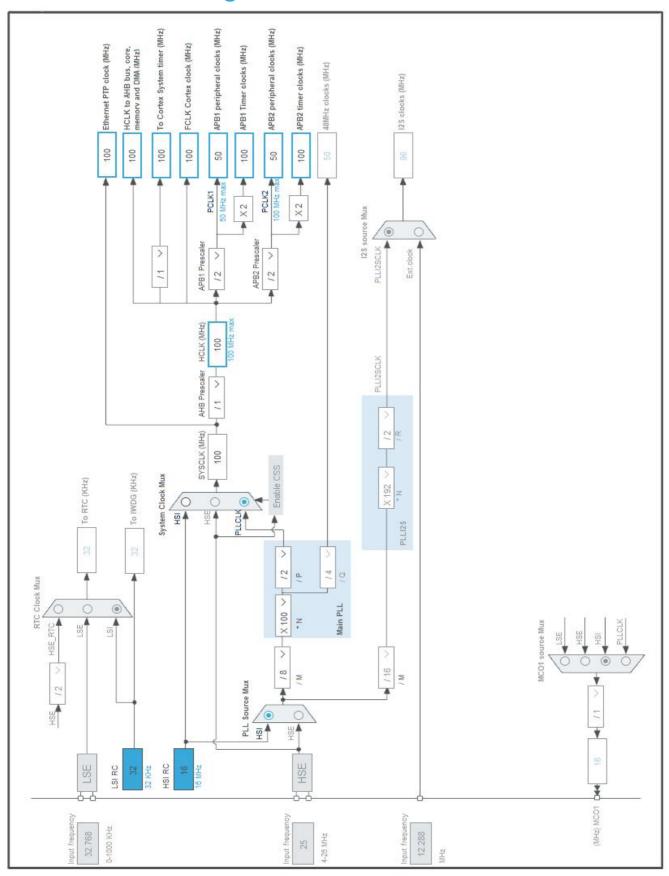
WLCSP49 (Top view)

# 3. Pins Configuration

Pin Number WLCSP49	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
4.0	· ·	1/0	TIMO CLIA	
A2	PA15	I/O	TIM2_CH1	
A5	BOOT0	Boot		
A6	VSS	Power		
A7	VDD	Power		
B1	VSS	Power		
B2	VDD	Power		
B6	PDR_ON	Power		
B7	VBAT	Power		
C4	PB6	I/O	TIM4_CH1	
C5	PB9	I/O	I2C2_SDA	
D3	VSS	Power		
D4	PB7	I/O	TIM4_CH2	
D5	PC13-ANTI_TAMP *	I/O	GPIO_Output	LED
E1	PB15	I/O	SPI2_MOSI	
E3	PB10	I/O	I2C2_SCL	
E5	PA2	I/O	ADC1_IN2	
E6	VSSA	Power		
E7	NRST	Reset		
F2	VDD	Power		
F3	PA7	I/O	SPI1_MOSI	
F4	PA6	I/O	SPI1_MISO	
F5	PA5	I/O	SPI1_SCK	
F6	PA0-WKUP	I/O	ADC1_IN0	
F7	VDDA	Power		
G1	PB13	I/O	SPI2_SCK	
G2	VCAP1	Power		
G4	PB1	I/O	ADC1_IN9	
G5	PB0	I/O	TIM3_CH3	
G6	PA4 *	I/O	GPIO_Output	CS1
G7	PA1	I/O	TIM2_CH2	

<sup>\*</sup> The pin is affected with an I/O function

# 4. Clock Tree Configuration



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# 5. Software Project

## 5.1. Project Settings

Name	Value
Project Name	newseqen
Project Folder	C:\Users\Bobon\Documents\GitHub\newseqen
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.27.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

## 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

## 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_DMA_Init	DMA
4	MX_ADC1_Init	ADC1
5	MX_SPI2_Init	SPI2
6	MX_TIM3_Init	TIM3
7	MX_TIM4_Init	TIM4
8	MX_I2C2_Init	I2C2
9	MX_TIM2_Init	TIM2
10	MX_SPI1_Init	SPI1

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# 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F411
MCU	STM32F411CEYx
Datasheet	DS10314_Rev6

### 6.2. Parameter Selection

Temperature	25
Vdd	1.7

## 6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

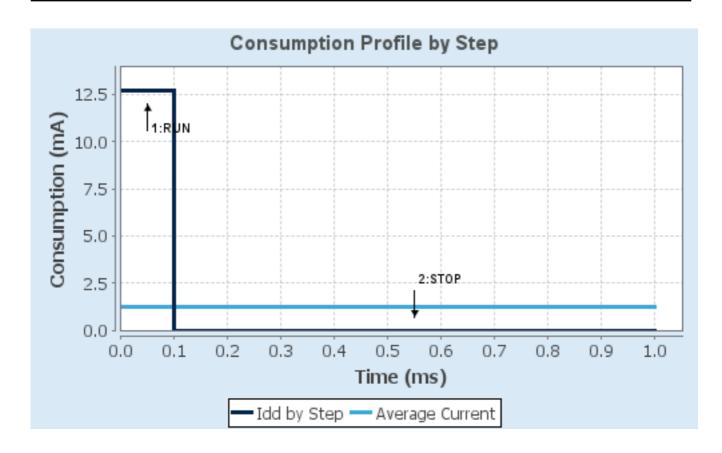
## 6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	1.7	1.7
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	SRAM	n/a
CPU Frequency	100 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LPLV Flash-
		PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	12.7 mA	9 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	125.0	0.0
Ta Max	103.9	105
Category	In DS Table	In DS Table

## 6.5. Results

Sequence Time	1 ms	Average Current	1.28 mA
Battery Life	3 months, 19	Average DMIPS	125.0 DMIPS
	days, 6 hours	-	

## 6.6. Chart



# 7. Peripherals and Middlewares Configuration

7.1. ADC1 mode: IN0 mode: IN2 mode: IN9

7.1.1. Parameter Settings:

ADCs\_Common\_Settings:

Mode Independent mode

ADC\_Settings:

Clock Prescaler PCLK2 divided by 4 \*

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment
Scan Conversion Mode Enabled

Scan Conversion Mode Enabled

Continuous Conversion Mode Enabled \*

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Enabled \*

End Of Conversion Selection EOC flag at the end of all conversions \*

ADC\_Regular\_ConversionMode:

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None Rank 1

Channel 9 \*
Sampling Time Channel 9 \*

ADC\_Injected\_ConversionMode:

Number Of Conversions 2 \*

External Trigger Source Injected Conversion launched by software

External Trigger Edge None
Injected Conversion Mode None
Injected Rank 1

Channel 0
Sampling Time 56 Cycles \*

Injected Offset 0
Injected Rank 2 \*

Channel 2 \*
Sampling Time 56 Cycles \*

Injected Offset 0

WatchDog:

Enable Analog WatchDog Mode false

7.2. I2C2 I2C: I2C

#### 7.2.1. Parameter Settings:

#### **Master Features:**

I2C Speed Mode Fast Mode \*

I2C Clock Speed (Hz) 400000

Fast Mode Duty Cycle Duty cycle Tlow/Thigh = 2

**Slave Features:** 

Clock No Stretch Mode Disabled
Primary Address Length selection 7-bit
Dual Address Acknowledged Disabled
Primary slave address 0
General Call address detection Disabled

#### 7.3. RCC

### 7.3.1. Parameter Settings:

#### **System Parameters:**

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled
Data Cache Enabled

Flash Latency(WS) 3 WS (4 CPU cycle)

**RCC Parameters:** 

HSI Calibration Value 16
TIM Prescaler Selection Disabled

HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

**Power Parameters:** 

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

#### 7.4. SPI1

### **Mode: Full-Duplex Master**

### 7.4.1. Parameter Settings:

#### **Basic Parameters:**

Frame Format Motorola

Data Size 8 Bits

First Bit MSB First

**Clock Parameters:** 

Prescaler (for Baud Rate) 4

Baud Rate 12.5 MBits/s \*

Clock Polarity (CPOL) Low
Clock Phase (CPHA) 1 Edge

**Advanced Parameters:** 

CRC Calculation Disabled
NSS Signal Type Software

#### 7.5. SPI2

#### **Mode: Transmit Only Master**

### 7.5.1. Parameter Settings:

#### **Basic Parameters:**

Frame Format Motorola

Data Size 8 Bits

First Bit MSB First

**Clock Parameters:** 

Prescaler (for Baud Rate) 128 \*

Baud Rate 390.625 KBits/s \*

Clock Polarity (CPOL) Low
Clock Phase (CPHA) 1 Edge

**Advanced Parameters:** 

CRC Calculation Disabled
NSS Signal Type Software

#### 7.6. SYS

Timebase Source: SysTick

#### 7.7. TIM2

**Combined Channels: Encoder Mode** 

## 7.7.1. Parameter Settings:

0
Up
65535 *
Division by 4 *
Disable
Disable (Trigger input effect not delayed)
Reset (UG bit from TIMx_EGR)
Encoder Mode TI1
Falling Edge *
Direct
No division
2 *
Falling Edge *
Direct
No division
2 *

#### 7.8. TIM3

mode: Clock Source

**Channel3: PWM Generation CH3** 

### 7.8.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) 2544 \*

Internal Clock Division (CKD) No Division auto-reload preload Enable \* **Trigger Output (TRGO) Parameters:** Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed) Trigger Event Selection Reset (UG bit from TIMx\_EGR) **PWM Generation Channel 3:** Mode PWM mode 2 \* Pulse (16 bits value) Enable Output compare preload Disable Fast Mode High **CH** Polarity 7.9. TIM4 **Combined Channels: Encoder Mode** 7.9.1. Parameter Settings: **Counter Settings:** Prescaler (PSC - 16 bits value) 0 Counter Mode ДD Counter Period (AutoReload Register - 16 bits value ) 65535 Internal Clock Division (CKD) No Division auto-reload preload Disable **Trigger Output (TRGO) Parameters:** Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed) Reset (UG bit from TIMx\_EGR) Trigger Event Selection **Encoder: Encoder Mode Encoder Mode TI1** Parameters for Channel 1 \_\_\_\_ Polarity Falling Edge \* IC Selection Direct Prescaler Division Ratio No division Input Filter 2 \* \_ Parameters for Channel 2 \_\_\_\_ Polarity Falling Edge \* Direct IC Selection Prescaler Division Ratio No division Input Filter 2 \*

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\* User modified value

# 8. System Configuration

# 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA2	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	
	PA0-WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	
I2C2	PB9	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High	
	PB10	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High	
SPI1	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI2	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
TIM2	PA15	TIM2_CH1	Alternate Function Push Pull	Pull-up *	Low	
	PA1	TIM2_CH2	Alternate Function Push Pull	Pull-up *	Low	
TIM3	PB0	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	Pull-up *	Low	
	PB7	TIM4_CH2	Alternate Function Push Pull	Pull-up *	Low	
GPIO	PC13- ANTI_TAMP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Very High	CS1

## 8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream4	Peripheral To Memory	Low

### ADC1: DMA2\_Stream4 DMA request Settings:

Mode: Circular \*
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable \*
Peripheral Data Width: Half Word
Memory Data Width: Half Word

## 8.3. NVIC configuration

## 8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM3 global interrupt	true	0	0
DMA2 stream4 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 global interrupt	unused		
TIM2 global interrupt	unused		
TIM4 global interrupt		unused	
I2C2 event interrupt			
12C2 event interrupt	unused		
· ·	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
FPU global interrupt		unused	

## 8.3.2. NVIC Code generation

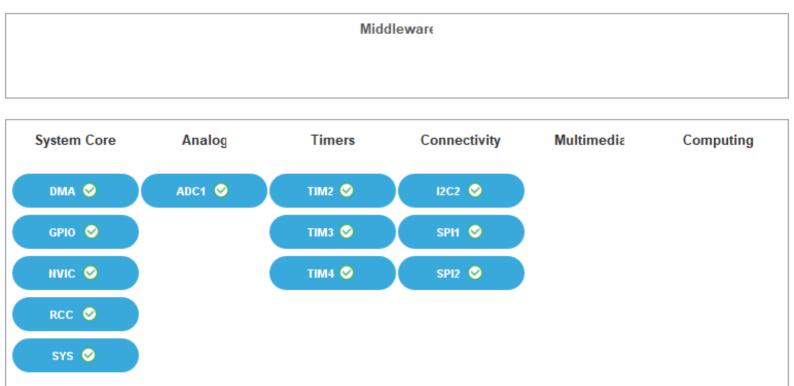
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
TIM3 global interrupt	false	true	true
DMA2 stream4 global interrupt	false	true	true

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Configuration	Report

\* User modified value

# 9. System Views

- 9.1. Category view
- 9.1.1. Current



## 10. Docs & Resources

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stm8\_embedded\_software\_solutions.pdf

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