Electronic Devices and Circuits I 2EI4
Design Project #4 - CMOS XOR GATE

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Summary

Logic gates are one of the fundamental building blocks of all digital components. Logic gates are primarily composed of various transistors and more specifically, either MOSFETs or BJTs. In this design project the MOSFET implementation of a transistor will be more closely examined.

Firstly, before jumping into the implementation of a digital logic gate it is important to understand how a MOSFET's characteristics can be used to design a logic gate. MOSFET transistors can act as voltage-controlled switches, where specific voltages applied at its gate terminal will cause the MOSFET to conduct current across its source and drain terminals. Additionally, there are two primary types of MOSFETs utilized in logic gate designs; N-MOS and P-MOS. As examined in the lectures it was noted that the N-MOS turns on (conducts) when a high enough voltage is applied to the gate and it turns off (stops conducting) when the gate voltage is low enough [2]. Conversely, the P-MOS turns off (stops conducting) when a high enough voltage is applied to the gate and it turns on (conducts) when the gate voltage is low enough.

Utilizing these gates in conjunction results in CMOS logic (Complementary MOS). In this scenario the state of NMOS and PMOS transistors compliments each other. This is evident in the CMOS inverter which will be used in this design project and its characteristics will be highlighted below.

Throughout the design process, the key principles for CMOS that were taught in lecture were heavily utilized [2]. These principles state that in a CMOS gate there are two networks; The upper block consists of PMOS transistors called the pull-up network (PUN) and the bottom block consists of NMOS transistors called the pull down network (PDN). Therefore, due to the nature of both networks, only one of the networks can be activated at a time. Using the above principles an XOR logic gate can be designed utilizing CMOS logic and MOSFET transistors.

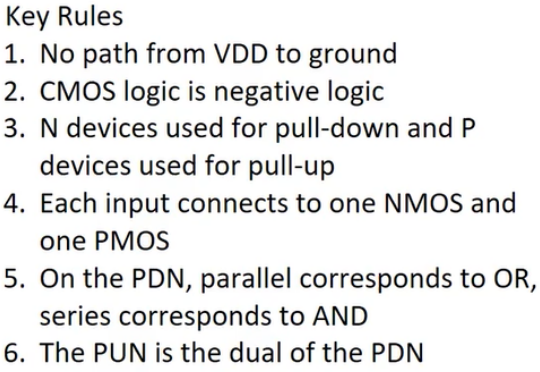


Figure 1: Key Rules of CMOS logic [2023 2EI4 Week 10 Lecture][2]

Circuit Schematic

To design the XOR COS circuit I began by deriving a boolean expression for the XOR gate utilizing negative logic and DeMorgan's theorem.

Truth table for an XOR gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Boolean expression for an XOR gate

$Y = A \oplus B$

$Y = \overline{A}B + A\overline{B}$ → Applying DeMorgan's theorem to the equation results in …

$Y = \overline{\overline{\overline{A}B + A\overline{B}}}$

$Y = \overline{(\overline{A}B) \bullet (A\overline{B})}$

$Y = \overline{(A + \overline{B}) \bullet (\overline{A} + B)}$

$Y = \overline{AB + \overline{A}\overline{B}}$

Table 2.1
Postulates and Theorems of Boolean Algebra

Postulate 2	(a)	$x + 0 = x$	(b)	$x \cdot 1 = x$
Postulate 5	(a)	$x + x' = 1$	(b)	$x \cdot x' = 0$
Theorem 1	(a)	$x + x = x$	(b)	$x \cdot x = x$
Theorem 2	(a)	$x + 1 = 1$	(b)	$x \cdot 0 - 0$
Theorem 3, involution		$(x')' = x$		
Postulate 3, commutative	(a)	$x + y = y + x$	(b)	$xy = yx$
Theorem 4, associative	(a)	$x + (y + z) = (x + y) + z$	(b)	$x(yz) = (xy)z$
Postulate 4, distributive	(a)	$x(y + z) = xy + xz$	(b)	$x + yz = (x + y)(x + z)$
Theorem 5, DeMorgan	(a)	$(x + y)' = x'y'$	(b)	$(xy)' = x' + y'$
Theorem 6, absorption	(a)	$x + xy = x$	(b)	$x(x + y) = x$

Figure 2: Deriving a boolean expression for an XOR gate that obeys CMOS logic [3]

Once a boolean expression for the CMOS gate has been derived, it can be implemented into the pull-down network (PDN) and then subsequently mirrored on the top pull-up network (PUN). As seen below in figure 4, the PDN network contains the inputs A in series with B which is then in parallel with the inputs $\overline{A}$ in series with $\overline{B}$. Then, a mirror of the PDN is implemented into the PUN using P-MOS transistors. The mirroring process involves converting series networks into parallel networks and vice

versa. The final circuit can be seen in figure 4. Lastly, to ensure that we are able to pass a complemented input to the XOR CMOS gate we must pass that input through a CMOS inverter. A CMOS inverter can be seen below in figure 3. The PDN consists of a single N-MOS transistor and the PUN consists of a single P-MOS transistor. Due to the characteristics of the transistors we can determine the expected characteristics of a CMOS inverter as seen in the table below.

CMOS inverter characteristics

Vin	PMOS	NMOS	Vout
0	1 (PMOS conducts and pulls Vout up to VDD)	0 (NMOS does not conduct)	1 (VDD)
1	0 (PMOS does not conduct)	1 (NMOS conducts and pulls Vout down to ground)	0 (GND)

Figure 3: Characteristics of a CMOS Inverter

The finalized XOR CMOS circuit utilizes a total of 12 MOSFETs. The PDN utilizes 4 N-MOS transistors while the PUN utilizes 4 P-MOS transistors. Additionally we require an 4 additional transistors (2 N-MOS & 2 P-MOS transistors) to implement 2 CMOS inverters for the complemented inputs $\overline{A}$ and $\overline{B}$

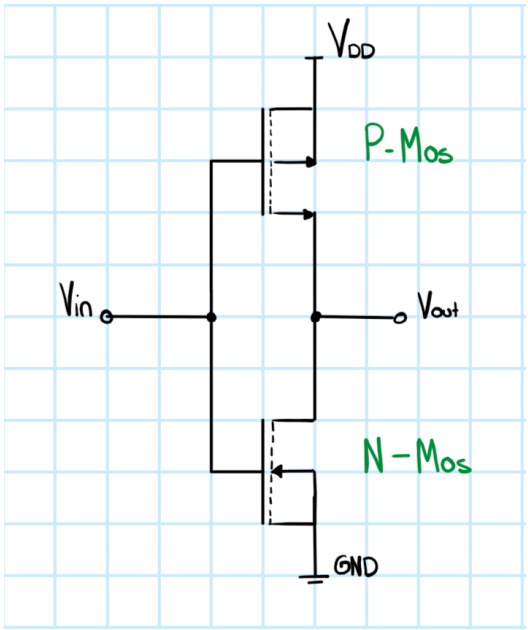


Figure 4: CMOS Inverter

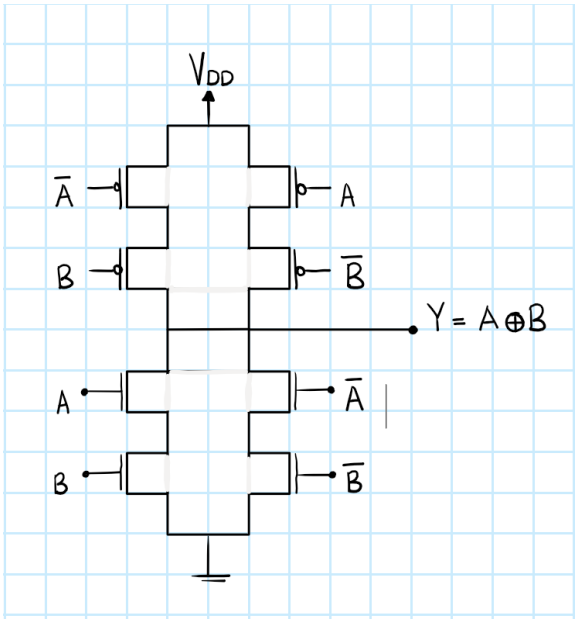


Figure 5: CMOS XOR Gate

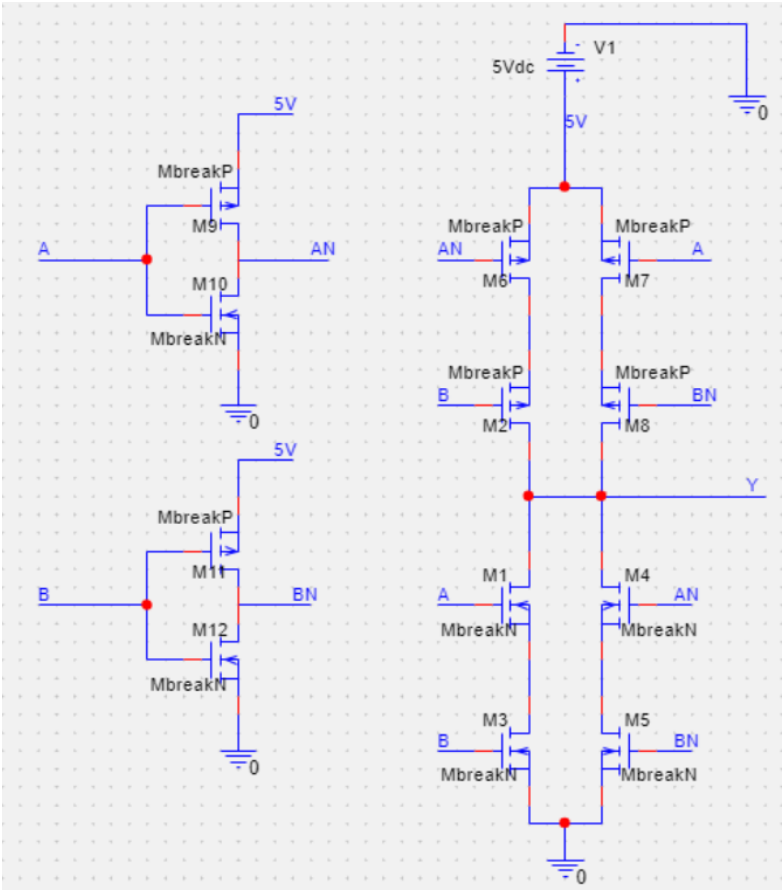


Figure 6: XOR CMOS schematic in PSpice

Ideal Sizing

Determining the ideal sizing of our XOR CMOS circuit allows us to minimize the time delay of the entire circuit. To achieve the ideal delay for a CMOS circuit it requires a symmetric circuit. Therefore, the ratio between the pull down network (composed of N-MOS components) and the pull up network (composed of P-MOS) should be 1:1. This ensures that both networks are symmetric and thus have the smallest time delay possible.

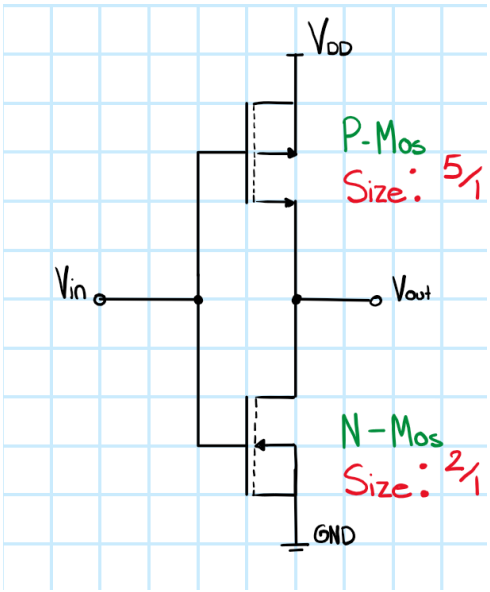
Given the symmetric nature of the circuit we must ensure that both the pull up network (PUN) and pull down network (PDN) have the same time delay. By examining the relationship for the time delay (low to high and high to low) in figure 7 we know that the conduction by electrons in N-MOS transistors are significantly faster than the conduction by holes present in P-MOS transistors. More specifically, electron conduction is faster by a factor of 2.5. This is because the electron mobility ratio of electrons to holes is 2.5. Therefore we cannot use the same size ratio for both NMOS and PMOS transistors since the PMOS will have a larger equivalent resistance and thus a larger transition time delay. Therefore, we must utilize the ideal ratio between PMOS and NMOS transistors of 2.5:1. This will result in the following size ratio: ($(\frac{W}{L})_p = \frac{5}{1}$ & $(\frac{W}{L})_n = \frac{2}{1}$

The above PMOS and NMOS ratios correspond to the ratios seen in the reference/unit CMOS inverter as seen in figure 8. To design a circuit that is symmetric we can design it in reference to the unit/reference CMOS inverter. The delay is dictated by two properties; The load capacitance and the average effective resistance during transition. As seen in figure 7, the average effective resistance is inversely proportional to the size of the transistor. Therefore, we can determine the ideal transistor size that will result in the ideal time delay. We can determine the ideal transistor size by finding the longest series path which corresponds to the worst case scenario time delay and adjusting its size to match the reference transistor size.

$\tau_{pHL} = 0.69 R_C C_L$
$\tau_{pLH} = 0.69 R_P C_L$

$R_N \propto \frac{1}{k}$
$k = k'(\frac{W}{L})$
$k' = \mu Cox \rightarrow$ Given that Cox is fixed
$\mu = \frac{\mu_e}{\mu_p} = 2.5 \rightarrow$ Electron mobility ratio of electrons to holes

Figure 7: Ideal sizing ratio between N-MOS and P-MOS



The average effective resistance is related to the electron mobility in a transistor as seen in the figure below. Additionally, we know that the P-MOS majority carriers are holes while the N-MOS majority carriers are electrons. From the relationship described below we know that electrons have a mobility that is 2.5 times higher than holes. As such, for a P-MOS to have the same effective resistance it must be larger by a factor of 2.5.

Figure 8: Reference/Unit CMOS Inverter

The worst-case scenario time-delay involves at most 2 MOSFETs which is seen in every branch of the CMOS XOR gate

Therefore comparing the equivalent resistance to the reference resistance…

$R_A + R_B = R_{ref}$

Let $R_A = R_B$

$2R = R_{ref}$

$R = \frac{R_{ref}}{2}$

From figure 7 we know that $R_N \propto \frac{1}{(\frac{W}{L})}$

$\frac{R_{ref}}{2} \propto \frac{1}{(\frac{W}{L})}$

We know that

$(\frac{W}{L})_A = (\frac{W}{L})_B = 2n$

Therefore the ideal sizing ratio with respect to the reference CMOS inverter for both NMOS and PMOS is $2n$ and $2p$

Figure 9: Individual transistor size

Given the above statement we cannot implement the ideal sizing in our hardware design because the $(W)idth$ & $(L)ength$ of a transistor are fixed physical parameters that were manufactured into the IC which cannot be changed. It is expected that the circuit will not achieve the ideal time delay since we are

limited to the sizing provided by the IC manufacturer. Therefore, if the provided PMOS transistor is smaller than the ideal ratio it could result in a significantly larger and slower time delay. On the other hand if the provided PMOS transistor is larger than the ideal ratio it could lead to a smaller and faster time delay. As seen above it is quintessential for a designer to balance all of the various factors when designing a CMOS logic gate.

Testing

For the physical circuit model, a total of 12 MOSFETs were used (6 PMOS and 6 NMOS). As a result, the CD4007B IC chip was utilized as it contained the desired number of transistors. The final physical circuit model can be seen in the figure below.

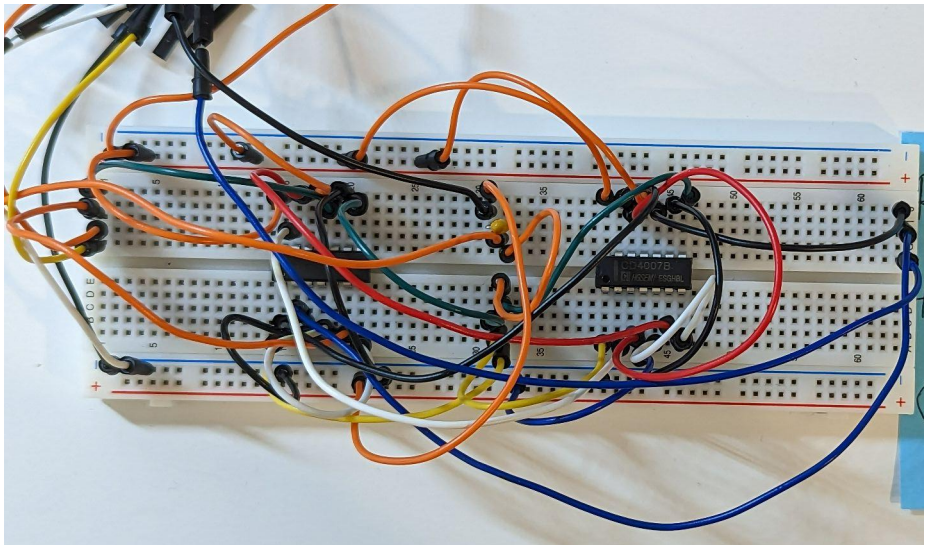


Figure 10: CMOS XOR gate physical circuit

Functional Testing

For testing the functionality of the CMOS XOR gate we needed to ensure that the circuit received specific inputs it would output a specific voltage that would correspond to the truth table mentioned in the previous sections. To test this the input voltages were set to be square waves with an offset of 2.5V and an amplitude of 2.5V but they were out of phase by 90 degrees. Additionally, digital IO pins were placed at both inputs as well as the output to track the logic states. As seen in figure 11 below, the designed CMOS XOR gate responds exactly as expected. When both inputs are a logic low (0V) or a logic high (5V) the output is also a logic low (0V). Likewise, when both inputs are complements of each other (A = 0V & B = 5V or A = 5V & B = 0V) then the output is also high (5V).

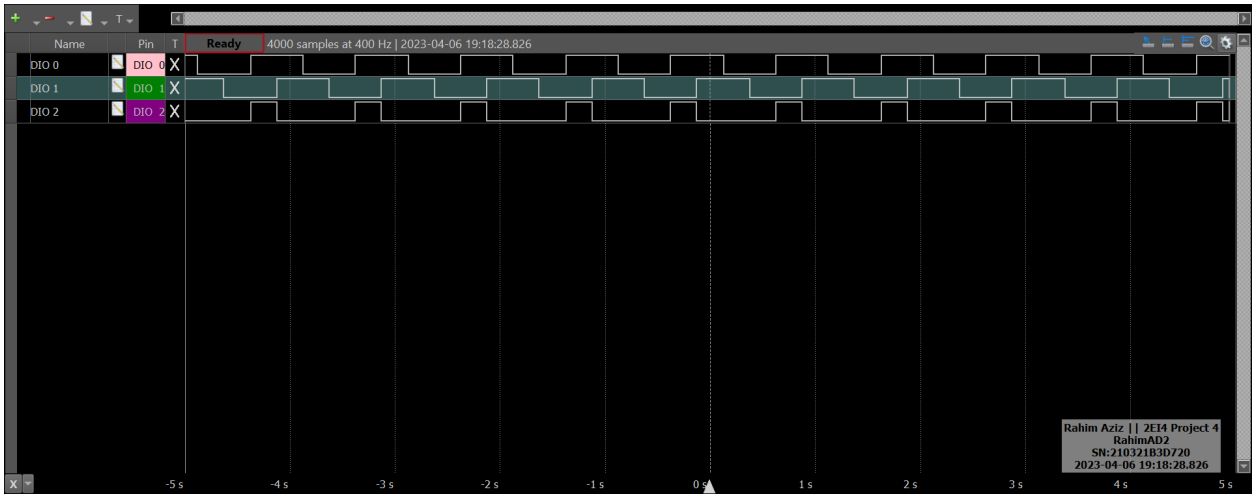


Figure 11: Logic Testing the CMOS XOR gate (DIO 0: A, DIO 1: B, DIO 2: Vout)

Static Testing

For static level testing we set one of the inputs to a logic high (+5V) and the second input to a square wave between 0V and 5V. Once data was collected we reversed the inputs to see the effects of the different inputs. In figure 12 below, the input corresponding to A was set to a logic high which resulted in $V_H = 2.59V$ and $V_L = 2.08mV$. When the inputs were swapped such that B was set to a logic high the resulting voltages were, $V_H = 4.25V$ and $V_L = 33.6mV$. The variations in the logic high voltage could be a result of either faulty wires or a greater internal resistance within the wiring for one of the inputs. Similarly, if one input is connected to a voltage source with a higher impedance than the other input, it may experience a larger voltage drop and result in a lower VH level. Additionally this could also be due to a potentially damaged IC. Utilizing the results where $V_H = 4.25V$ and $V_L = 33.6mV$ we can determine the percentage error for V_H. $\frac{4.25-5}{5} \times 100\% = -15\%$

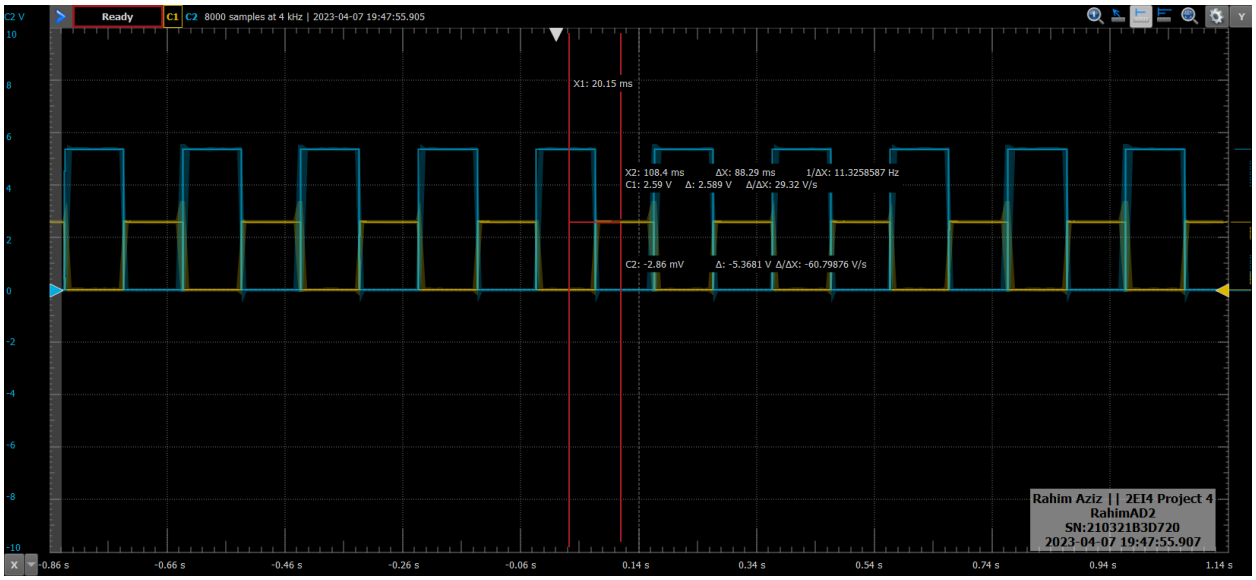


Figure 12: Static Testing (A = DC 5V B = Square Wave, offset = 2.5V, amplitude = 5V)

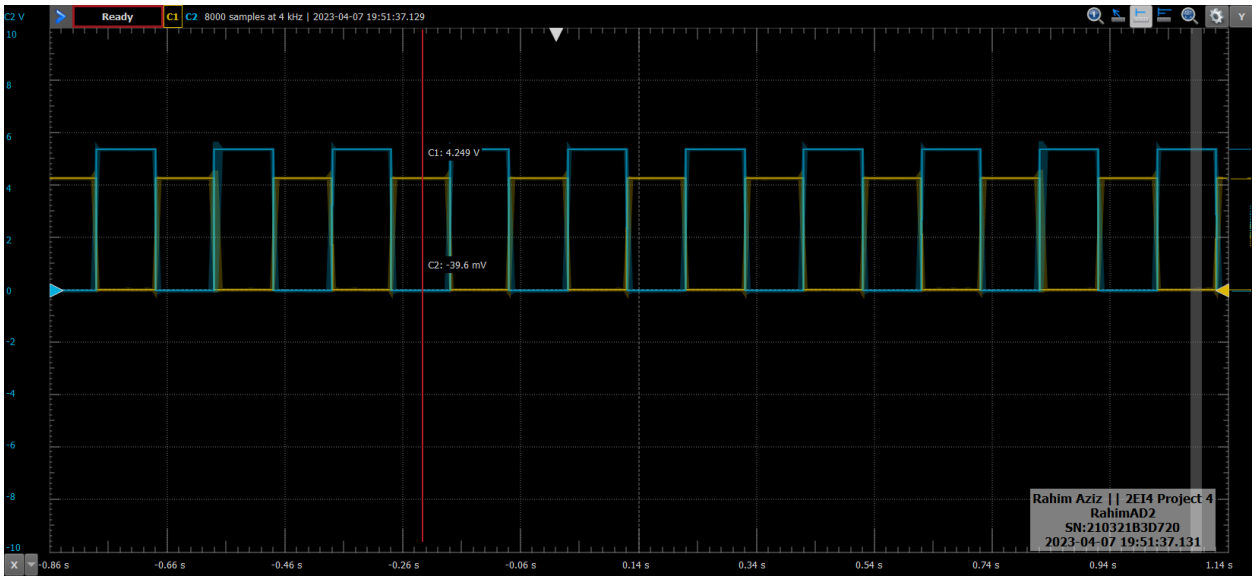


Figure 13: Static Testing (A = Square Wave, offset = 2.5V, amplitude = 5V B = DC 5V)

Maximum input voltage for a logic low (V_{IL}) and the minimum input voltage for a logic high (V_{IH})

To determine the V_{IL} and V_{IH} of this circuit we set the input voltage of B to a logic high (5V) and the input voltage of A to a square wave with an offset of 2.5V and an amplitude of 2.5V. By continuously decreasing the amplitude until the circuit logic levels failed we could determine the V_{IL} and V_{IH}. The figure below depicts the input voltage and output voltage prior to logic level failure as the amplitude was decremented. Therefore from the graph it can be determined that $V_{IL} = 3.03V$ and that $V_{IH} = 1.94V$. Additionally to confirm these results a voltage transfer characteristics graph was plotted in figure 15. We can see that at the aforementioned input voltages ($V_{IL} = 3.03V$ and that $V_{IH} = 1.94V$), the output voltage begins to enter the saturation region where the logic level is indeterminate.

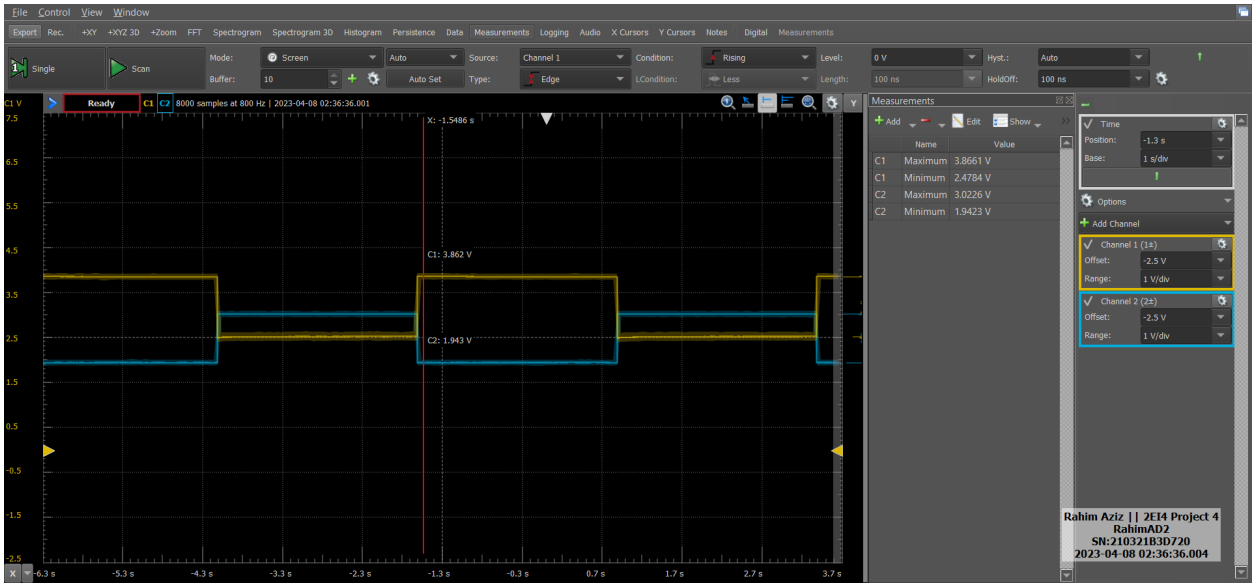


Figure 14: CMOS XOR voltage input & output prior to logic level failure

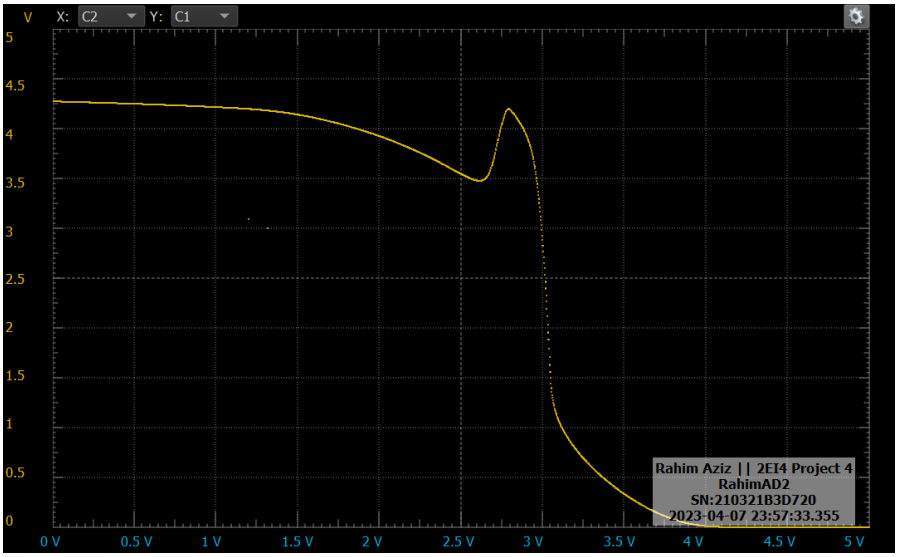


Figure 15: CMOS XOR voltage transfer characteristics

Timing

The next step in the process was to perform timing analysis on the circuit. This analysis would be able to determine the transition delay between the low-to-high and high-to-low states. This was accomplished by attaching a 100nF capacitor (CM104) to the output and measuring the voltage across it. Additionally, the input voltage B was set to DC 5V while the input voltage A was set to a square wave with an amplitude =2.5V, offset=2.5V, and a frequency set to 500mHz. From the graph below it was determined that the rise time was $t_{rise} = 421\ us$ and the fall time was $t_{fall} = 387\ us$. Next, we can determine the high-to-low propagation delay by measuring from 50% of the time taken for the input pulse to go low-to-high to 50% of the time it takes for the output to go from high-to-low. From the graph it was determined that $\tau_{pHL} = 156\ us$. For the low-to-high propagation delay we perform the exact same test as above but for the opposite state transition. From the graph it was determined that $\tau_{pLH} = 112\ us$. To determine the overall propagation delay we can utilize the following formula, $\tau_p = \frac{\tau_{pHL}+\tau_{pLH}}{2} = \frac{156+112}{2} = 134\ us$.

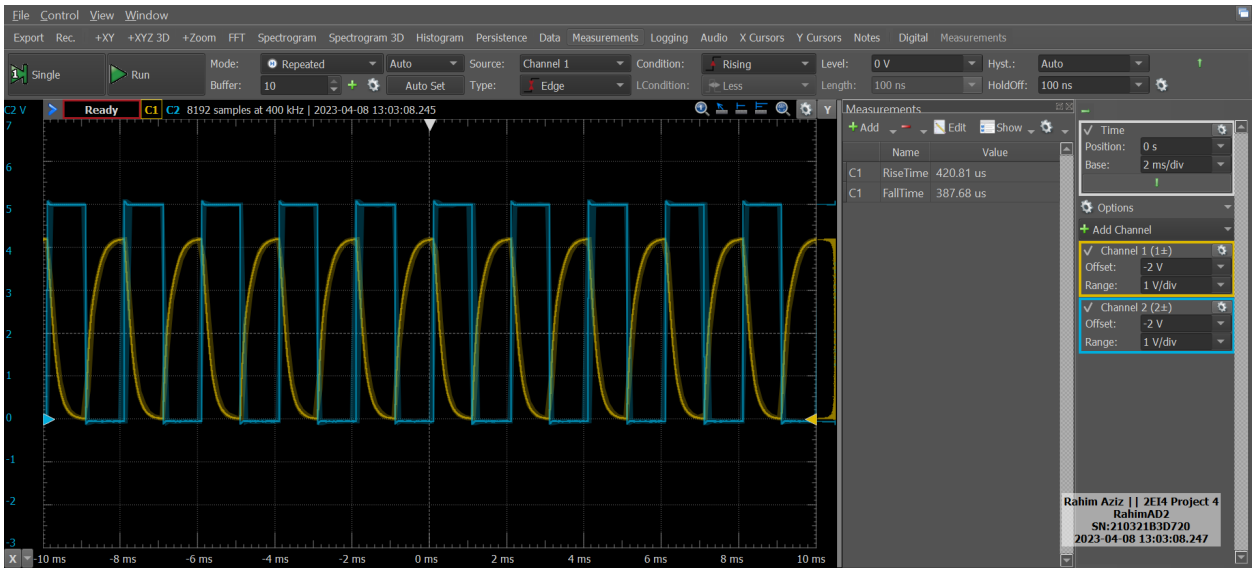


Figure 16: Timing analysis using a 100nF capacitive load

Data Sheet

MC140007UB → LINK

References

[1] A. S. Sedra, K. C. Smith, T. C. Carusone, and V. Gaudet, Microelectronic circuits, 8th ed. New York, NY: Oxford University Press, 2019.

[2] “Week 3: Digital Fundamentals,” class notes for COMP ENG 2DI4, Department of Electrical and Computer Engineering, University of McMaster, Fall, 2022.

[3] “Week 10: Digital Logic,” class notes for ELEC ENG 2EI4, Department of Electrical and Computer Engineering, University of McMaster, Winter, 2023.