Electronic Devices and Circuits I 2EI4

Design Project #2 - “Ideal” Voltage Controlled Switches

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Test Plan

As mentioned in deliverable 1, a real switch has various non-idealities that will affect the performance of the physical circuit. Therefore, for each circuit we will specify a test plan to quantify the non-idealities and the performance of our design. [2]

Switch Type 1 - Test Plan

For the purpose of testing this circuit $V_{supply} =+ 5V$, $V_1 = 5V$ and $V_{control}$ will be a square wave that oscillates between 0V and 5V at a frequency of 500mHz. The first non-ideality is that in the ON state ($V_{control} =+ 0V$) we expect a small voltage drop, ($V_{out} < V_{in}$) since a real switch provides a quantifiable resistance. The metric for this non-ideality would be tested by measuring the voltage at the output node and measuring the voltage at the input node would allow us to compute the voltage drop across our switch. The second non-ideality is that in the OFF state ($V_{control} =+ 5V$) there is expected to be some leakage current as a real switch will not have infinite resistance. Therefore, the metric for this non-ideality would be to measure the voltage at the output and divide it by the resistance value to determine the current flowing through the switch. Additionally in the previous deliverable another non-ideality was the fact that a real switch cannot completely conduct bidirectionally, which will be proven by the two above test metrics. The final non-ideality is that a real switch will operate only over a specific input range supply. Therefore, the metric for this non-ideality would be to input a ramp function ($0\ to\ 5V$) to the supply voltage and determine at what values does the switch begin operating outside of its expected behaviors.

Switch Type 2 - Test Plan

The test plan for the type 2 switch is very similar to the test plan for the type 1 switch. For the purpose of testing this circuit $V_{supply} =+ 5V$, $V_1 = 5V$ and $V_{control}$ will be a square wave that oscillates between 0V and 5V at a frequency of 500mHz. The first non-ideality is that in the ON state ($V_{control} =+ 0V$) we expect a small voltage drop, ($V_{out} < V_{in}$) since a real switch provides a quantifiable resistance. The metric for this non-ideality would be tested by measuring the voltage at the output node (V_A & V_B) and measuring the voltage at the input node would allow us to compute the voltage drop across our switch. The second non-ideality is that in the OFF state ($V_{control} =+ 5V$) there is expected to be some leakage current as a real switch will not have infinite resistance. Therefore, the metric for this non-ideality would be to measure the voltage at the output (V_A & V_B) and divide it by the resistance value to determine the current flowing through the switch. Additionally in the previous deliverable another non-ideality was the fact that a real switch cannot completely conduct bidirectionally, which will be proven by the two above test metrics. The final non-ideality is that a real switch will operate only over a specific input range supply. Therefore, the metric for this non-ideality would be to input a ramp function ($0\ to\ 5V$) to the supply voltage and determine at what values does the switch begin operating outside of its expected behaviors.

Switch Type 1

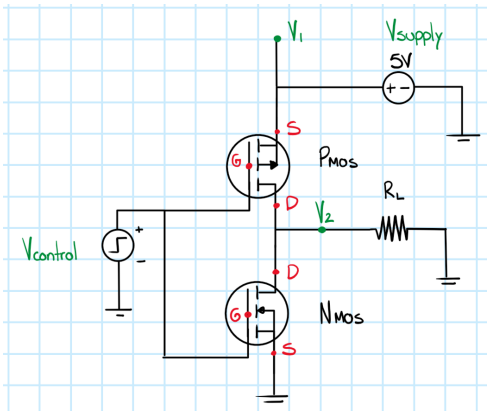

Figure 1: Switch Type 1; Initial Schematic Drawing

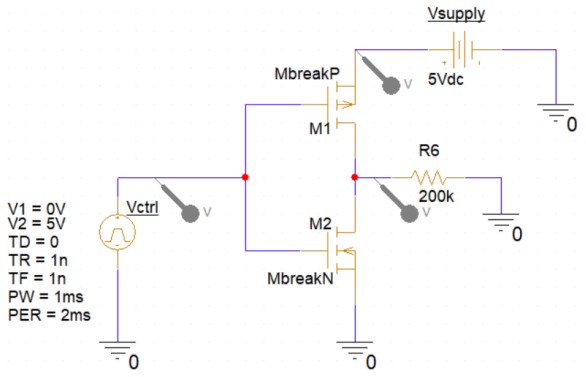

Figure 2: Switch Type 1; PSpice Schematic

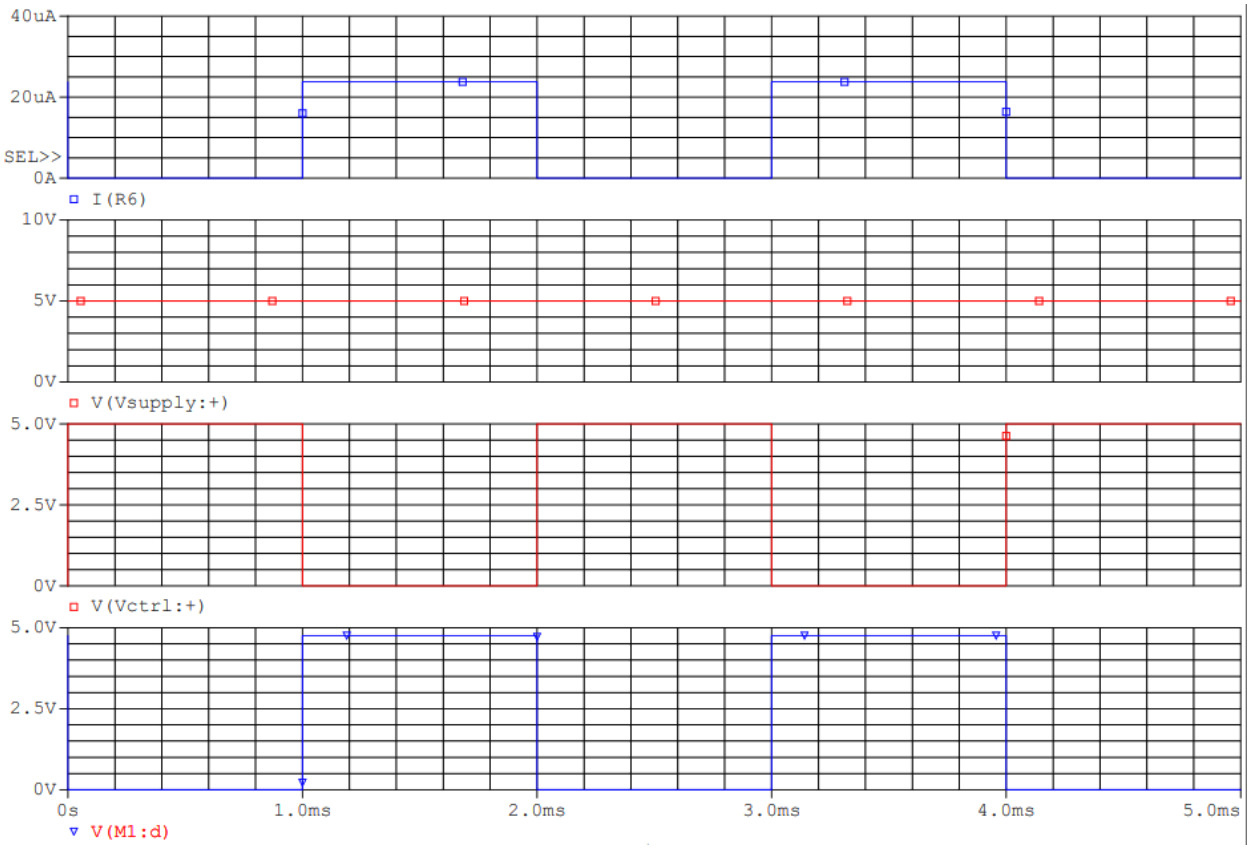

Figure 3: Switch Type 1 Simulation

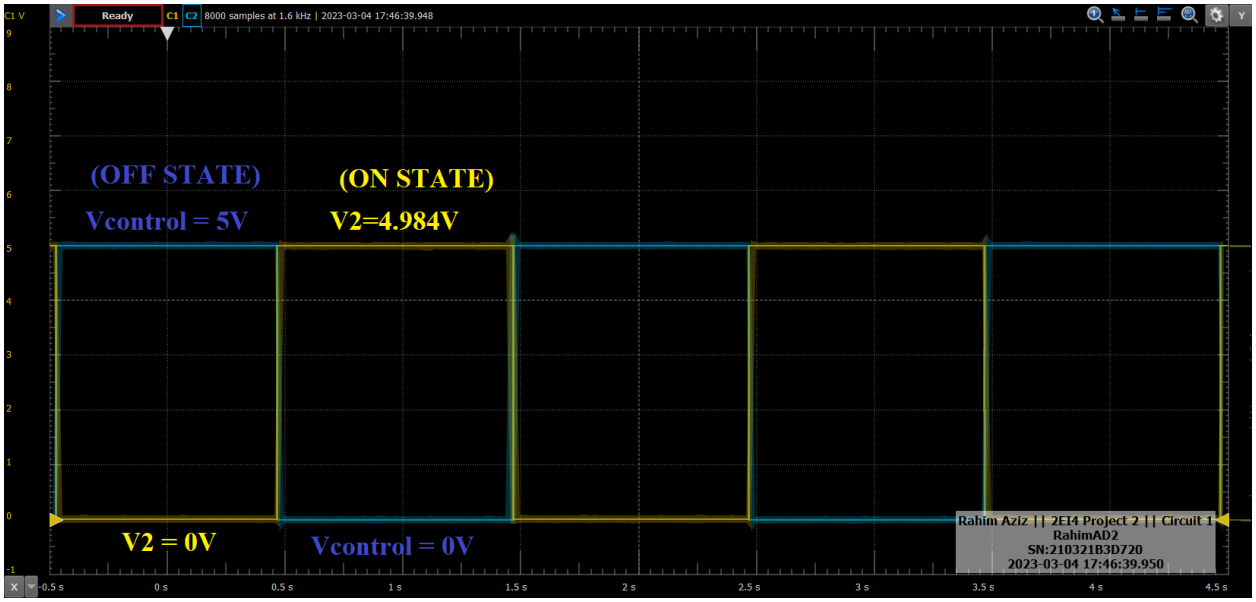

Figure 4: AD2 Measured Vcontrol (Blue) & V2 (Yellow) waveform

Utilizing the documentation in LAB 3, the values for the threshold voltage (V_T) and transconductance parameter (K) was found by plotting the IV characteristics for the CD4007B IC. [3]

PMOS

- $V_{T2} = 1.7V$
- $K = 4.4\mu A/V$

NMOS

- $V_{T1} = 1.75V$
- $K = 7.3\mu A/V$

Voltage drop during (ON STATE/CLOSED)($V_{control} = 0V$)

For the NMOS we know…

$V_{GS1} = 0V$

$V_{GS1} \leq V_{T1}$, therefore the NMOS is in cutoff and the drain current is $I_{DS} = 0mA$

For the PMOS we know…

$V_{SG2} = 5V - 0V \geq - V_{T2}$

$V_{SG2} \geq - V_{T2}$

$5V \geq + 1.7V$, therefore the PMOS is in either saturation or linear mode

Assuming it is in saturation

$I_{DS} = \frac{k}{2}(V_{SG2} + V_{T2})^2$

$I_{DS} = \frac{0.0000044A}{2}(5 - 1.7)^2 = 2.39 \times 10^{-5}A$

Therefore given the current we can calculated $V_2 = V_{D2}$

$V_2 = I_D R_L = (2.39 \times 10^{-5}A)(200,000\Omega) = 4.79V$

Therefore the voltage drop during the ON STATE should be $V_{S2} - V_{D2} = 5V - 4.79V = 0.21V$

Current Leakage (OFF STATE/OPEN)($V_{control} = 5V$)

For the PMOS we know…

$V_{SG} = 5V - 5V \leq V_T$

$V_{SG} \leq V_T$

$0V \leq + 1.7V$, therefore the PMOS is in cutoff and the drain current is $I_{DS} = 0mA$

Therefore there should be no leakage current

Voltage Supply Range (ON STATE/CLOSED)($V_{control} = 0V$)

For this state the PMOS must remain in saturation, therefore $V_{SD2} \geq (V_{SG2} + V_{T2})$

$V_{SD2} \geq (5V - 1.7V)$

$V_{SD2} \geq 3.3V$

Voltage Supply Range (OFF STATE/OPENED)($V_{control} = 5V$)

For this state the PMOS must remain in cutoff, therefore $V_{SG2} \leq - V_T$

$V_{SG2} \leq - V_T$

$V_{SG2} \leq 1.7V$

$V_{S2} - V_{G2} \leq 1.7V$

$V_{S2} \leq 1.7V + 5V \leq 6.2V$

Therefore, in this state our V_{supply} must remain below $6.2V$ however the project specification demands that $V_{supply} \leq 5V$

Figure 5: Theoretical Test Case Calculations

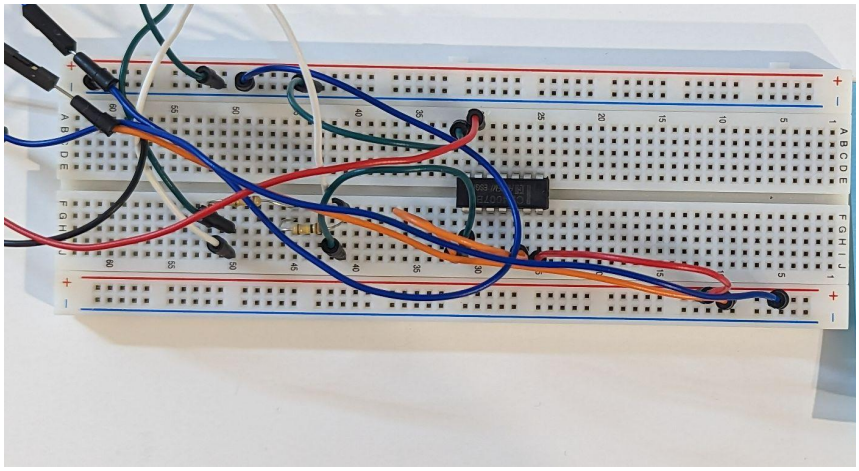

Figure 6: Switch Type 1 Physical Circuit

Experimental Measurements	
Voltage drop during (ON STATE/CLOSED)($V_{control} = 0V$) $V_{12} = V_{SD} = V_S - V_D$	$V_1 = V_S = 5.002V$ $V_2 = V_D = 4.984V$ $V_{SD} = 5.002V - 4.984V = 0.018V$

Current Leakage during (OFF STATE/OPEN)($V_{control} = 5V$) $I_{RL} = \frac{V_2}{R_L} = \frac{V_D}{R_L}$	$I_{RL} = \frac{-10.7mV}{200k\Omega} = 5.35 \times 10^{-8} A$
Voltage Supply Range (ON STATE/CLOSED)($V_{control} = 0V$) $0V \leq V_1, V_{supply} \leq 5V$	See Figure 5 According to the figure the switch operates in this state properly when $1.084V \leq V_{supply} \leq 5V$
Voltage Supply Range (OFF STATE/OPENED)($V_{control} = 5V$) $0V \leq V_1, V_{supply} \leq 5V$	See Figure 6 According to the figure the switch operates in this state properly when $3.506V \leq V_{supply} \leq 5V$

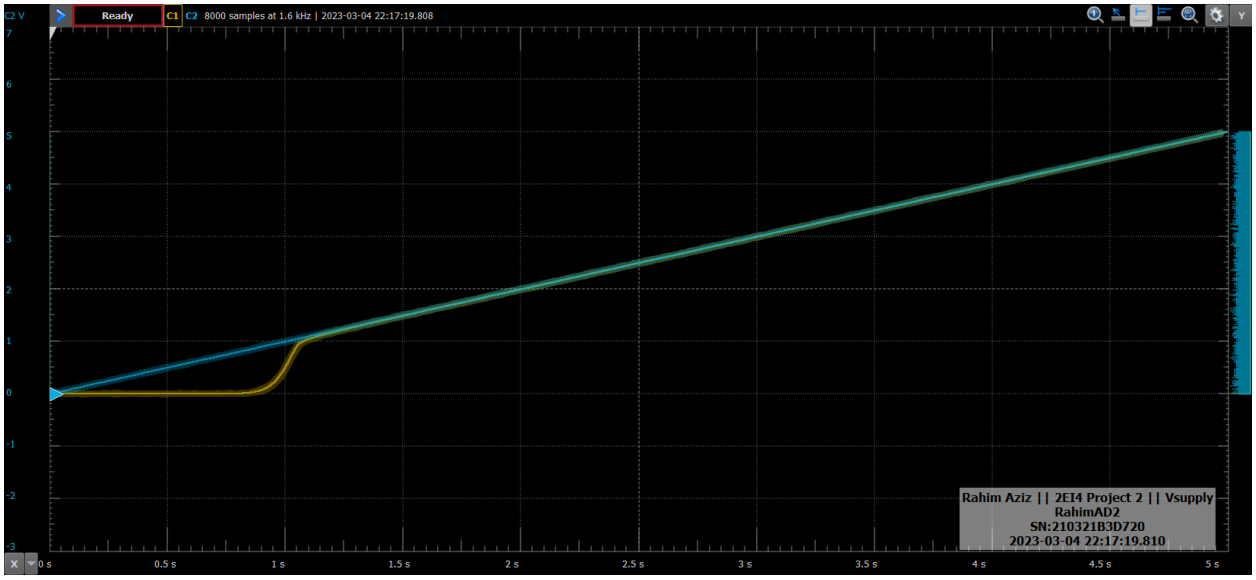

Figure 7: Voltage Supply Operating Range for ON STATE (Vcontrol = 0V)

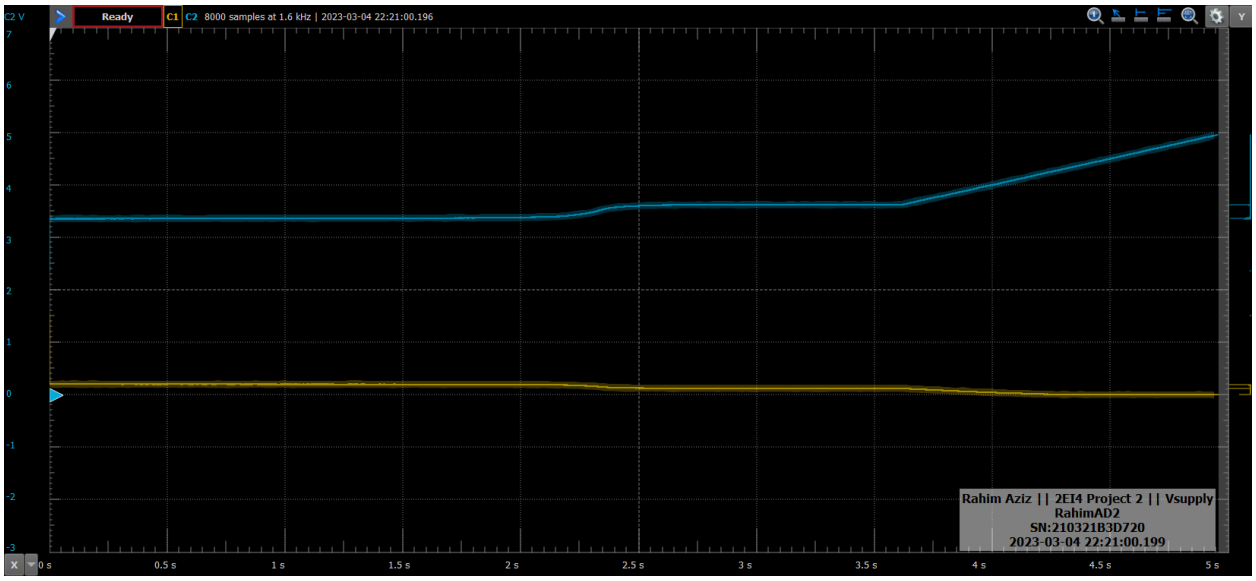

Figure 8: Voltage Supply Operating Range for OFF STATE (Vcontrol = 5V)

Experimental Measurements vs Theoretical Measurements

After testing the physical circuit and design and comparing the test values to the theoretical measurements we can observe various characteristics. First of all, the voltage drop across the switch in the physical circuit was actually smaller than the calculated & simulated value. Therefore, in this aspect the physical circuit was closer to an ideal circuit than the models predicted. The next non-ideality that was tested was the leakage current in the OFF state of the switch. The calculated & simulated model predicted a leakage current of 0mA however the physical design had an extremely small leakage current of $5.7245 \times 10^{-7} A$ proving that the physical switch design isn't an ideal switch. The final non-ideality was the operating supply voltage range of the switch in both ON and OFF states. The predicted voltage supply range for the ON state was $V_{SD_2} \geq 3.3V$ and the supply range for the OFF state was $V_{S2} \leq 6.2V$. The physical measurements for the supply range showed vastly different results. The voltage supply range for the ON state was measured to be $1.084V \leq V_{supply} \leq 5V$. Throughout this range, the voltage V_2 (Yellow on the graph) closely followed the input voltage V_1 (Blue on the graph). This is precisely the behavior we would expect because in the ON state the switch is expected to conduct such that $V_1 = V_2$. The supply range for the OFF state was $3.506V \leq V_{supply} \leq 5V$. Throughout this range, the voltage V_2 (Yellow on the graph) closely hovered around 184mA indicating a leakage current. This is behavior began to disappear and approach $0mA$ above when the supply voltage climbed above $3.506V$.

Design Tradeoffs

This design is relatively simple, requiring only two resistors, two enhancement type MOSFETS, and a single voltage supply. Additionally, the small operating supply range contributes to the simplicity of the circuit. Additionally the lack of components results in a cheaper and more economic circuit. The resistors cost $0.06 per part and the CD4007B MOSFET IC costs around 0.65$ per chip.

Switch Type 2

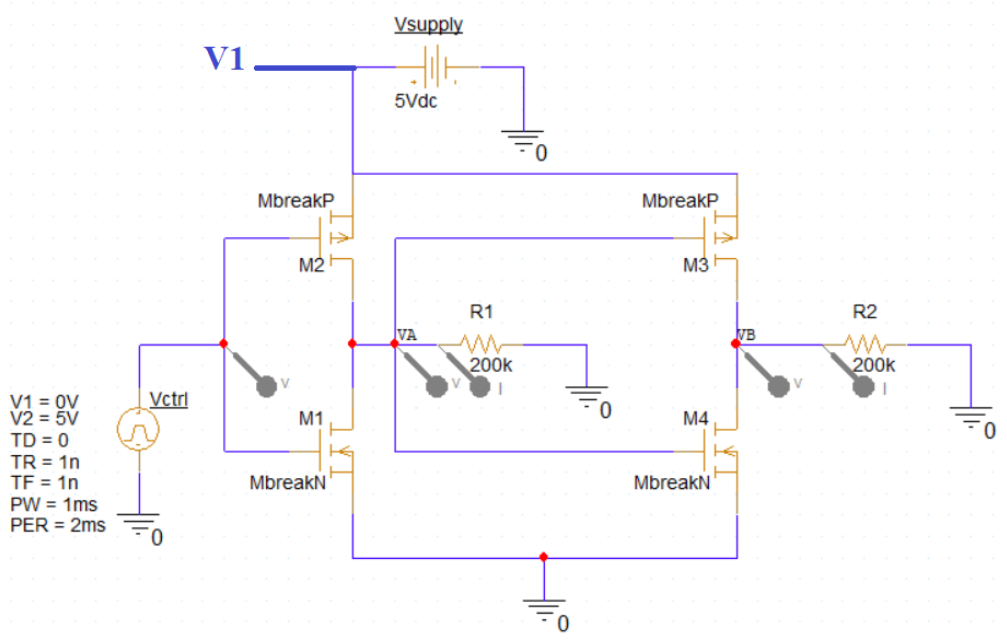

Figure 9: Switch Type 2; PSpice Schematic

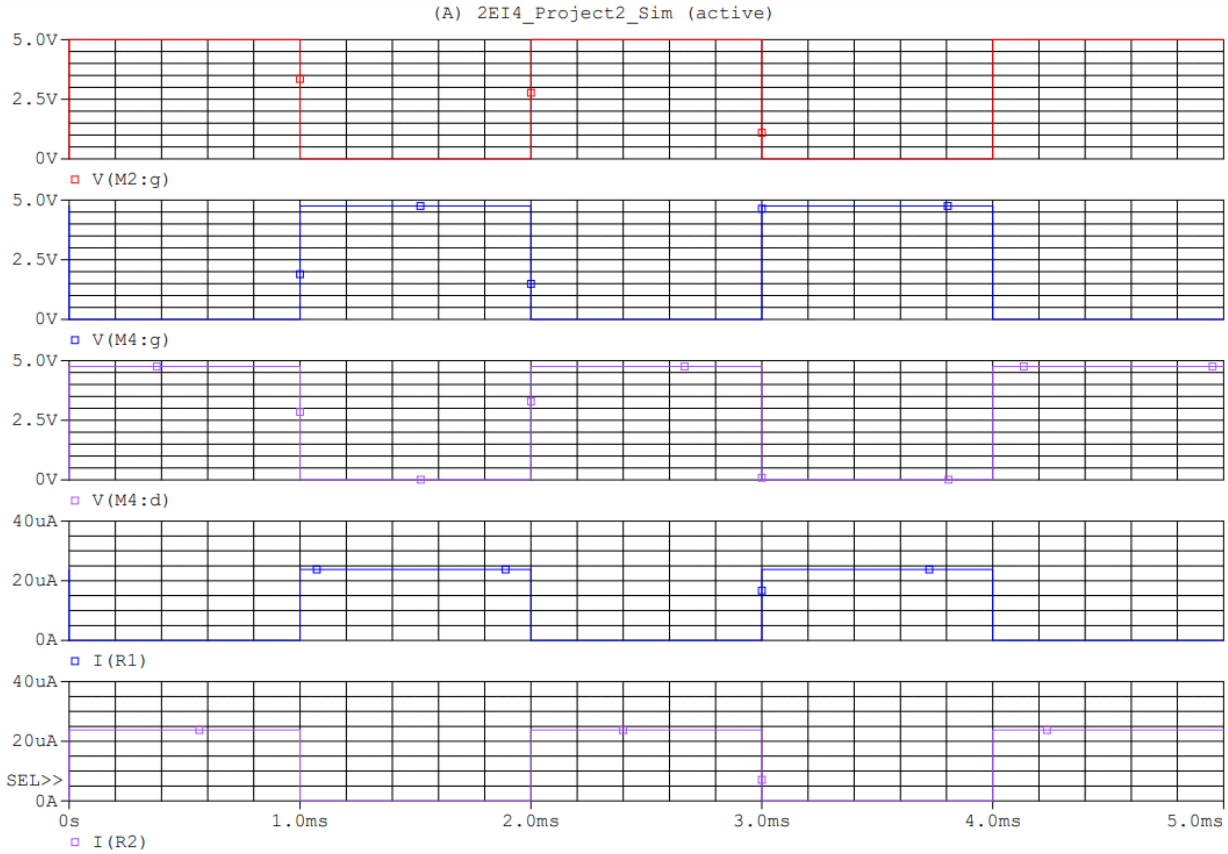

Figure 10: Switch Type 2 Simulation

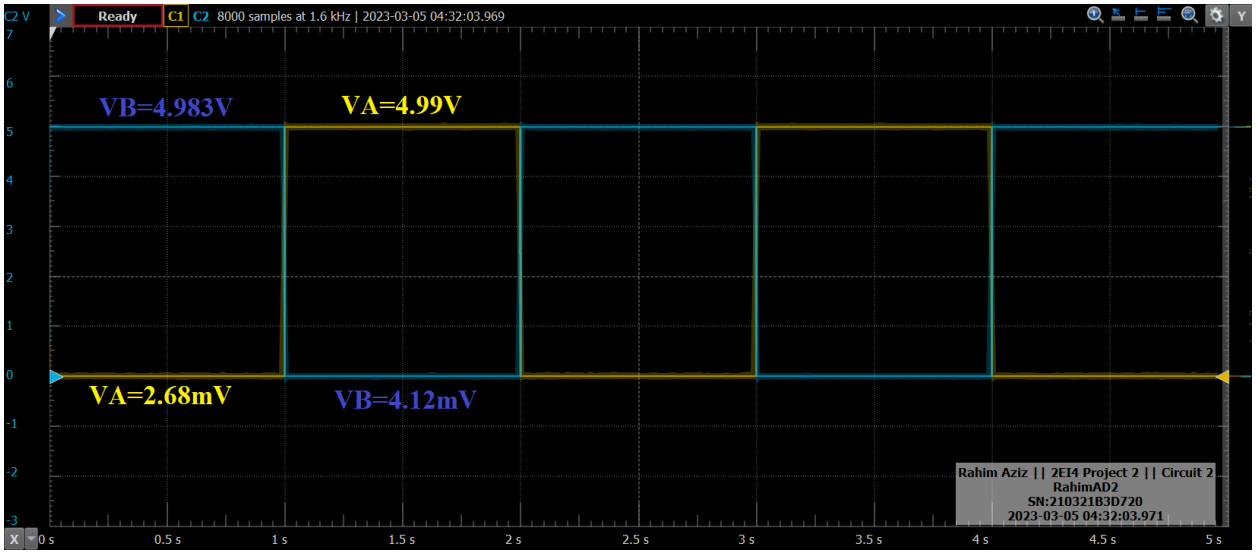

Figure 11: AD2 Measured VA(Blue) & VB (Yellow) waveform

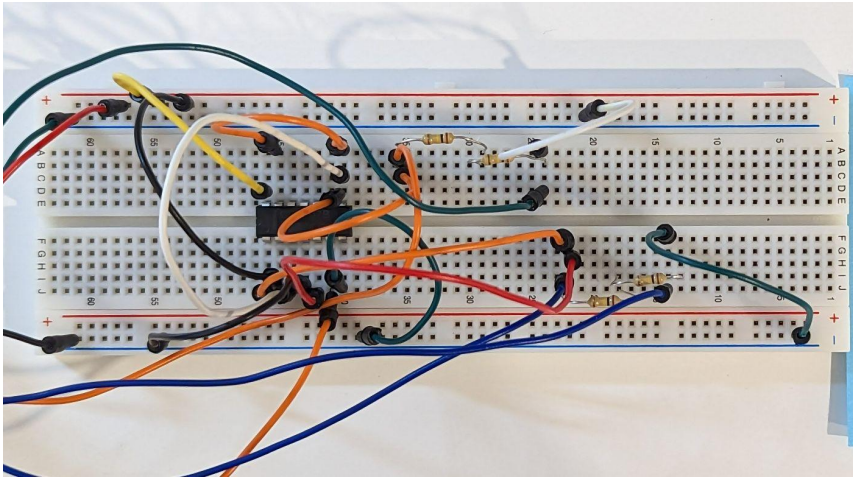

Figure 12: Switch Type 2 Physical Circuit

Experimental Measurements	
Voltage drop during (VA Conducts)($V_{control} = 0V$) $V_{12} = V_{SD} = V_S - V_D$	$V_1 = V_S = 5.002V$ $V_2 = V_D = 4.982V$ $V_{SD} = 5.002V - 4.982V = 0.020V$
Voltage drop during (VA Conducts)($V_{control} = 0V$) (Across second pair of MOSFETS) $V_{12} = V_{SD} = V_S - V_D$	$V_1 = V_S = 5.002V$ $V_2 = V_D = 4.983V$ $V_{SD} = 5.002V - 4.983V = 0.019V$

Current Leakage during (VB Conducts)($V_{control} = 5V$)(Across first pair of MOSFETS) $I_{RL} = \frac{V_2}{R_L} = \frac{V_D}{R_L}$	$I_{RL} = \frac{-11.96mV}{200k\Omega} = 5.98 \times 10^{-8} A$
Current Leakage during (VA Conducts)($V_{control} = 5V$)(Across second pair of MOSFETS) $I_{RL} = \frac{V_2}{R_L} = \frac{V_D}{R_L}$	$I_{RL} = \frac{-3.227mV}{200k\Omega} = 1.61 \times 10^{-8} mA$
Voltage Supply Range (VA Conducts)($V_{control} = 0V$) $0V \leq V_1, V_{supply} \leq 5V$	See Figure 13 According to the figure the switch operates in this state properly when $896.1mV \leq V_{supply} \leq 5V$
Voltage Supply Range (VB Conducts)($V_{control} = 5V$) $0V \leq V_1, V_{supply} \leq 5V$	See Figure 14 According to the figure the switch operates in this state properly when $3.91V \leq V_{supply} \leq 5V$

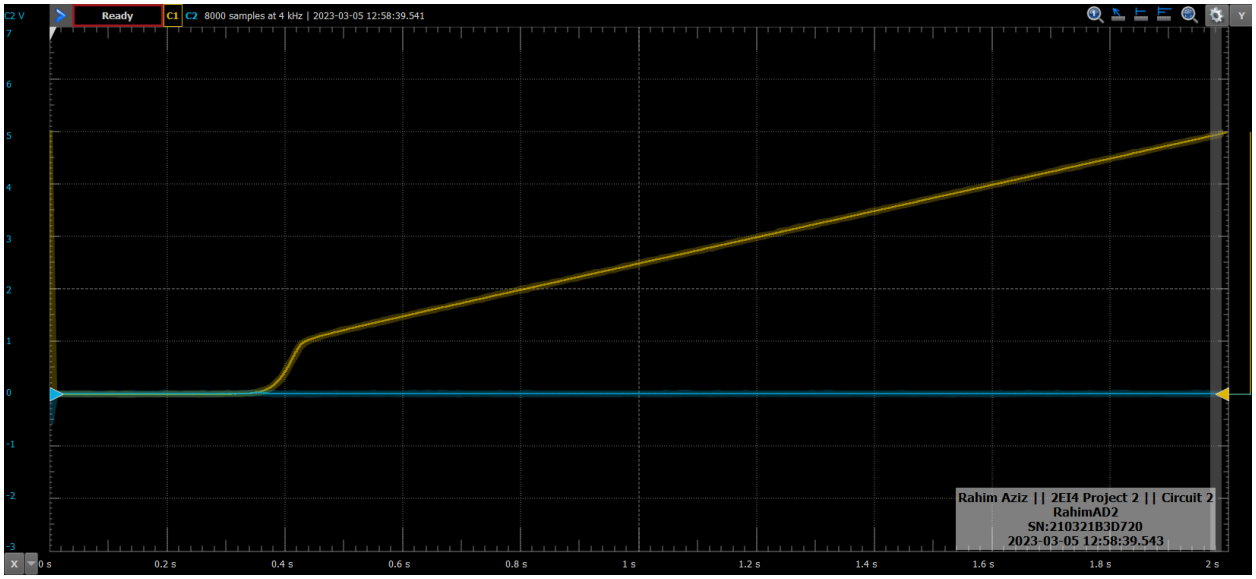

Figure 13: Voltage Supply Operating Range for VA conducting (Vcontrol = 0V)

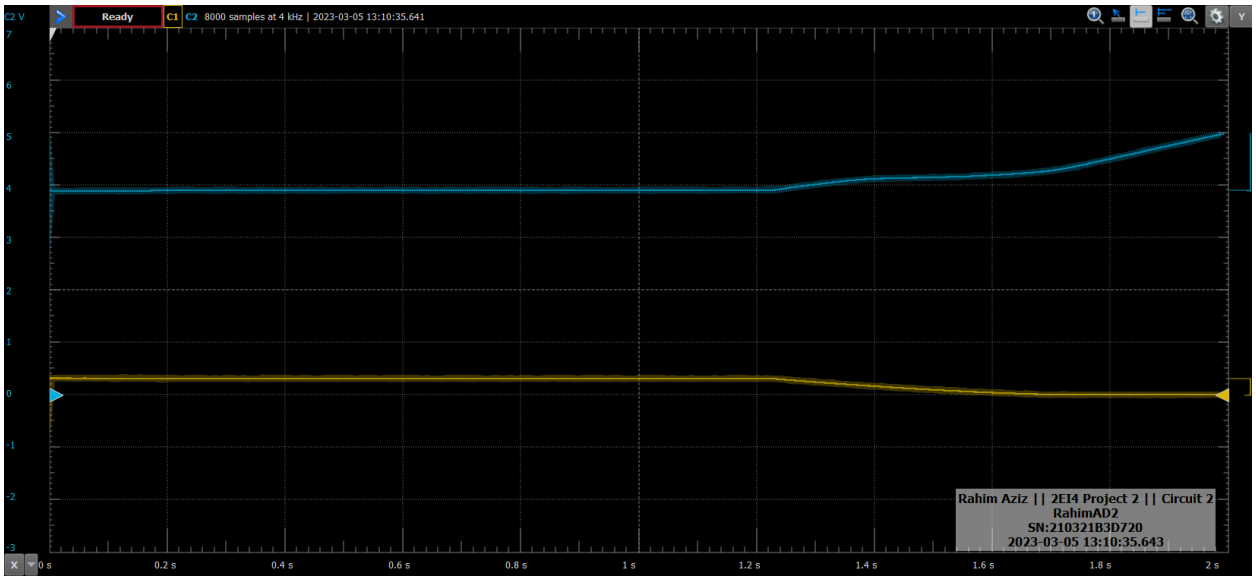

Figure 14: Voltage Supply Operating Range for VB conducting (Vcontrol = 5V)

Experimental Measurements vs Theoretical Measurements

After testing the physical circuit and design and comparing the test values to the theoretical measurements we can observe various characteristics. First of all, the voltage drop across the switch in the physical circuit was actually smaller than the calculated & simulated value. The theoretical drop according to the simulated model was 0.24V while the experimental drop was around 0.020V for both outputs (V_A & V_B). Therefore, in this aspect the physical circuit was closer to an ideal circuit than the models predicted. The next non-ideality that was tested was the leakage current in the OFF state of the switch. The calculated & simulated model predicted a leakage current of 0mA however the physical design had an extremely small leakage current of $5.98 \times 10^{-8} A$ when V_A is not conducting and $1.61 \times 10^{-8} mA$ when V_B is not conducting. This proves that the physical switch design isn't an ideal switch and therefore the switch does not possess the quality of having infinite resistance. The final non-ideality was the operating supply voltage range of the switch in both V_A conducts and V_B conducts. The predicted voltage supply range for both states were predicted to be very similar to the switch type 1 as this switch utilizes the same structure for each of the switches. The physical measurements for the supply range showed vastly different results. The voltage supply range for the conduction of V_A state was measured to be $896.1mV \leq V_{supply} \leq 5V$. Throughout this range, the voltage V_A (Yellow on the graph) closely followed the input ramp function voltage while V_B (Blue on the graph) remained at zero. This is precisely the behavior we would expect because when V_A conducts the switch should have the qualities that $V_1 \approx V_A$ and $V_B = 0V$. The supply range for the conduction of V_B state was $3.91V \leq V_{supply} \leq 5V$. Throughout this range, the voltage V_A (Yellow on the graph) closely hovered around 306mA indicating a leakage current. This is behavior began to disappear and approach $0mA$ above when the supply voltage climbed above $3.91V$. Concurrently, V_B began approaching 5V when we based this threshold. Despite the operating ranges being vastly different

from the predicted values, they are quite similar to the values found experimentally in the first switch. This proves that this design is reasonably scalable.

Design Tradeoffs

This design is relatively simple but slightly more complicated than the first one, requiring four resistors, four enhancement type MOSFETS, and a single voltage supply. Additionally, the small operating supply range contributes to the simplicity of the circuit. There are a few more components resulting in a slightly more expensive circuit. The resistors cost $0.06 per part and the CD4007B MOSFET IC costs around 0.65$ per chip. An alternative to both previous designs was considered using BJT's as they are cheaper than MOSFETS. After further research, it was determined that MOSFETS were more advantageous for varying applications. Firstly, MOSFETS have a switching frequency that is significantly higher than a BJT's, allowing it to be used in high-frequency applications. Additionally, MOSFETS are known to have a much smaller conduction loss during their ON state as well as a much smaller switching loss. Lastly, MOSFETS are more thermally stable as they have a positive temperature coefficient. This means that during the ON state as the temperature increases, the resistance of the switch increases resulting in a decreasing drain current. This is far more beneficial than the negative temperature coefficient property that BJTS possess. [4]

The final tradeoffs to consider are completely dependent on the application. Given this project has no specification on the application of the switches the following tradeoffs are purely for discussion purposes. This arrangement of switches is commonly used in microcontroller pins and therefore a pull-up/pull-down resistor would be a very practical improvement to the design. This would ensure that during the transient switching state, the microcontroller would not be reading any floating values. [4]

Data Sheet

MC140007UB → LINK

References

[1] A. S. Sedra, K. C. Smith, T. C. Carusone, and V. Gaudet, Microelectronic circuits, 8th ed. New York, NY: Oxford University Press, 2019.

[2] R. Aziz. “Design Project #2 - “Ideal” Voltage Controlled Switches - Deliverable 1”, March 4, 2023

[3] Electronic Devices and Circuits I 2EI4, “Lab 3: Field Effect Transistors”, March 4, 2023

[4] V. M. Srivastava, K. S. Yadav, and G. Singh, ‘Design and performance analysis of double-gate MOSFET over single-gate MOSFET for RF switch’, Microelectronics Journal, vol. 42, no. 3, pp. 527–534, 2011.