Electronic Devices and Circuits I 2EI4
Design Project #3 - Amplifier

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Summary

An electronic amplifier is a circuit that uses an external power supply to generate an output signal that is a larger copy of the input signal. The fundamental components that compose a simple amplifier circuit include; capacitors, resistors, a power supply, and transistors (BJT or MOSFETS). Depending on their arrangement you can end up with one of the three standard amplifier configurations. The three standard amplifier configurations are the common base, common emitter, and common collector amplifier. The primary goal of this project is to design an amplifier that can take an input of $\pm\ 0.5V$ from a source with an internal resistance of 100Ω and deliver it to a 100Ω load with an acceptable linearity and less than 10% attenuation ($A_v = Gain \geq 0.9$). The gain specification required implies that the amplifier being designed is not to amplify the input signal but to act as a buffer within a larger amplifying circuit.

Design

The first essential step in designing this circuit involved selecting the appropriate amplifier topology to suit the specifications. After further investigation of the three common amplifier configurations the common collector topology was chosen based on its core characteristics. By examining the characteristics in the figure below (figure 1), we can determine which is best suited for the project constraints.

11. BJT Single Stage Transistors

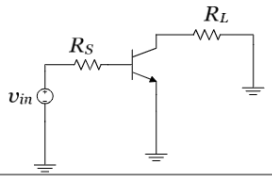
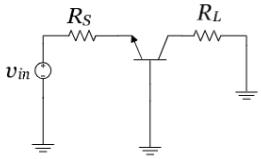
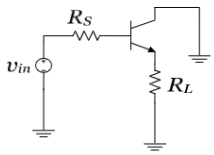
	Common Emitter	Common Base	Common Collector
Circuit			
$A_v = \frac{v_o}{v_{in}}$	$-g_m(R_L \parallel r_o)\frac{r_\pi}{R_S + r_\pi}$	$\frac{+g_m(R_L \parallel r_o)}{1+g_m R_S}$	$\frac{g_m R_L}{1+g_m R_L}\cdot\frac{R_{in}}{R_{in}+R_S} \approx 1$
R_{in} (to the right of R_S)	r_π	$1/g_m$	$r_\pi(1+g_m R_L)$
R_{out} (to the left of R_L)	r_o	$r_o(1+g_m R_S)$	$\frac{\alpha}{g_m}+\frac{R_S}{\beta+1}$
Allowed input signal range	$0.2V_T$	$0.2V_T(1+g_m R_S)$	$0.2V_T(1+g_m R_L)$

Figure 1: Common BJT amplifier configuration characteristics

Firstly, we can start by examining the input resistance. We are ideally looking for a high input resistance which will result in a gain that is close to 1. We can see that both the common emitter and common collector equations for R_{in} will result in a moderate/high input resistance. Therefore we can eliminate the common base/gate topology. Next, since we are designing an amplifier buffer with a desired gain of 1 we can notice that the common collector would be the desired choice given that it has a gain that is roughly equivalent to 1. Lastly, the design specifications of the allowed signal swing is $|0.5V|$ which is considered very large. The common collector caters the best towards a larger input signal swing based on its equation and knowing that our $R_L = 100\Omega$ is considered large. Therefore the ideal choice for an amplifier topology that would operate within the project specifications would be the common collector.

After some extensive research it was decided that the design would utilize the 2N3904 BJT provided in the course kit. A BJT was chosen over a MOSFET for various reasons. First of all, BJT's perform much better in low current applications and are often used in amplifier circuits as very small variations in their input current can cause larger changes in their output current (i.e. Higher Gain). Furthermore, the amplifier stage of a BJT is far more linear than a MOSFET because the gain is independent of the bias voltage. Despite drawing slightly more power the BJT produces an output that is a generally higher fidelity in comparison to its MOSFET counterpart [1]. Additionally, as seen in figure 1-3 below the BJT has a significantly higher g_m than a MOSFET which allows the BJT to satisfy all the constraints of the design project.

The calculations performed for the required component values are as seen below

The first calculation pertains to the calculation of the small signal parameter g_m. Utilizing the gain formula & the project constraints on the gain we can determine the minimum required value for g_m for any topology configuration and any device choice

$A_v = \frac{g_m R_L}{1+g_m R_L} \bullet \frac{R_{in}}{R_t+R_{in}}$

Given we know that the project requires a gain of … $A_v \geq 0.9$ and assuming that for a common collector/drain $\frac{R_{in}}{R_t+R_{in}} \approx 1$ for $R_{in} >> R_t$

$\frac{g_m R_L}{1+g_m R_L} \bullet 1 \geq 0.9$

$g_m \geq 90mS$

Figure 2: Minimum required value for the transconductance parameter g_m

BJT COMMON COLLECTOR TOPOLOGY

Next we can calculate the small signal parameter g_m for a common collector BJT circuit using the constraints of the project

$|v_{in}| = 0.2V_T(1 + g_m R_L) \geq 0.5$

Plugging in the values we know, $v_{in} \geq 0.5V,\ V_T = 25mV,\ and\ R_L = 100\Omega$

$0.2(0.025V)(1 + g_m(0.1k\Omega)) \geq 0.5$

$g_m \geq 990S \geq 0.99mS$

Now calculate the required value for the input resistance for a common collector BJT circuit using the gain constraint

$A_v = \frac{g_m R_L}{1+g_m R_L} \bullet \frac{R_{in}}{R_t+R_{in}}$

$A_v \geq 0.9$

$\frac{g_m R_L}{1+g_m R_L} \bullet \frac{R_{in}}{R_t+R_{in}} \geq 0.9$

Plugging in the values we know, $g_m = 990s,\ R_L = 100\Omega,\ and\ R_t = 100\Omega$

$R_{in} \geq 900\Omega$

$R_{in} \geq 0.9k\Omega$

REQUIRED COMPONENTS VALUES

Next we can solve the values within the internal resistance by utilizing the formula for a common collector amplifier

$R_{in} = R_{eq}||(r_{\pi} \bullet (1 + g_m R_L))$

$r_{\pi} = \frac{B}{g_m} = \frac{100}{0.99S} = 101\Omega$

$R_{in} = R_{eq}||(101\Omega \bullet (1 + (0.99S)(100\Omega))$

$R_{eq} \geq 988\Omega$

From the above circuit we know that R_1 and R_2 are in parallel such that $R_{eq} = R_1||R_2$

$\frac{1}{R_1} + \frac{1}{R_2} \geq \frac{1}{R_{eq}}$

Therefore we can choose any resistor combination of R_1 & R_2 such that their parallel combination is larger than 988Ω. Therefore the arbitrarily chosen values ended up being $R_2 = 2k\Omega$ and $R_3 = 3.3k\Omega$

Therefore we can recalculate the theoretical gain of this circuit taken into account the effect of the bias resistors on R_{in}…

$R_{in} = 2k\Omega||3k\Omega = 1.245k\Omega = 1245\Omega$

$A_v = \frac{g_m R_L}{1+g_m R_L} \bullet \frac{R_{in}}{R_t+R_{in}} = \frac{(990)(100)}{1+(990)(100)} \bullet \frac{1245}{100+1245} = 0.923$

Figure 3: Initial required component calculations of the BJT circuit

MOSFET COMMON DRAIN TOPOLOGY

For the MOSFET circuit given the minimum constraint on the transconductance parameter of $g_m \geq 90$, we can state the following….

$g_m = \sqrt{2kI_D}$

$\sqrt{2kI_D} \geq 90$

$I_D \geq \frac{90}{2 \bullet k}$

From the experiments in lab 3 we know that $k = 4.4\mu A/V^2$ for an NPN MOSFET

$I_D \geq \frac{90^2}{2 \bullet k}$

$I_D \geq \frac{90^2}{2 \bullet 0.044}$

$I_D \geq 92045\ mA$

As seen above for a MOSFET amplifier circuit to achieve the same gain and transconductance parameter as the constraints it would require an enormous amount of current which exceeds the limits of the AD2. As such we can confidently say that a BJT is preferable because the desired g_m parameter is significantly larger than that of a MOSFET

Figure 4: Initial required component calculations of the MOSFET circuit

The last component chosen was the coupling capacitor. The primary goal of a coupling capacitor is to separate the AC voltages from the DC bias voltages. For this design a 100uF capacitor was chosen. A relatively large capacitor was chosen arbitrarily to ensure all incoming AC frequencies were separated from the DC biases.

Simulation

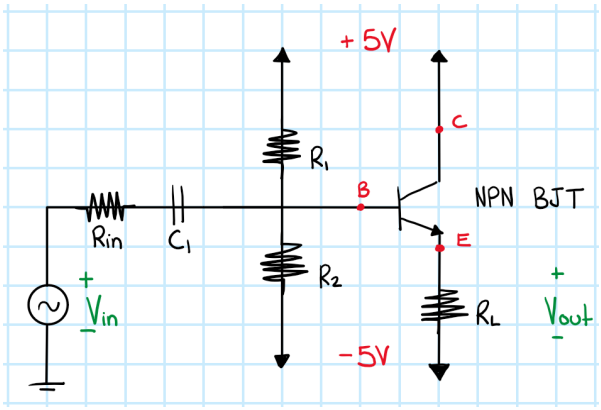


Figure 5: Common Collector Amplifier; Initial Schematic Drawing

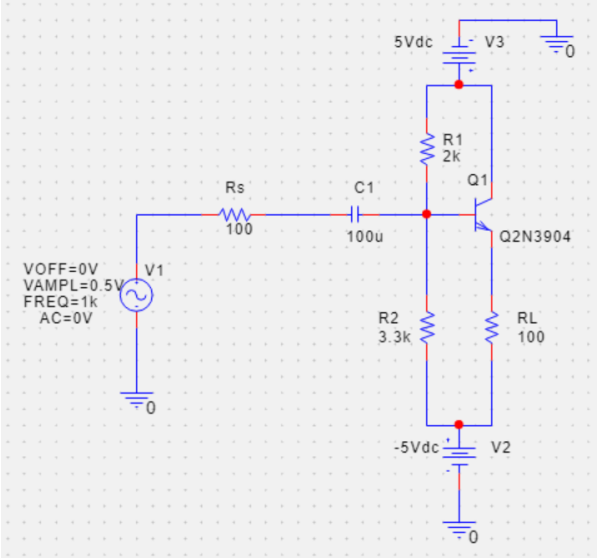


Figure 6: Common Collector Amplifier in PSPice

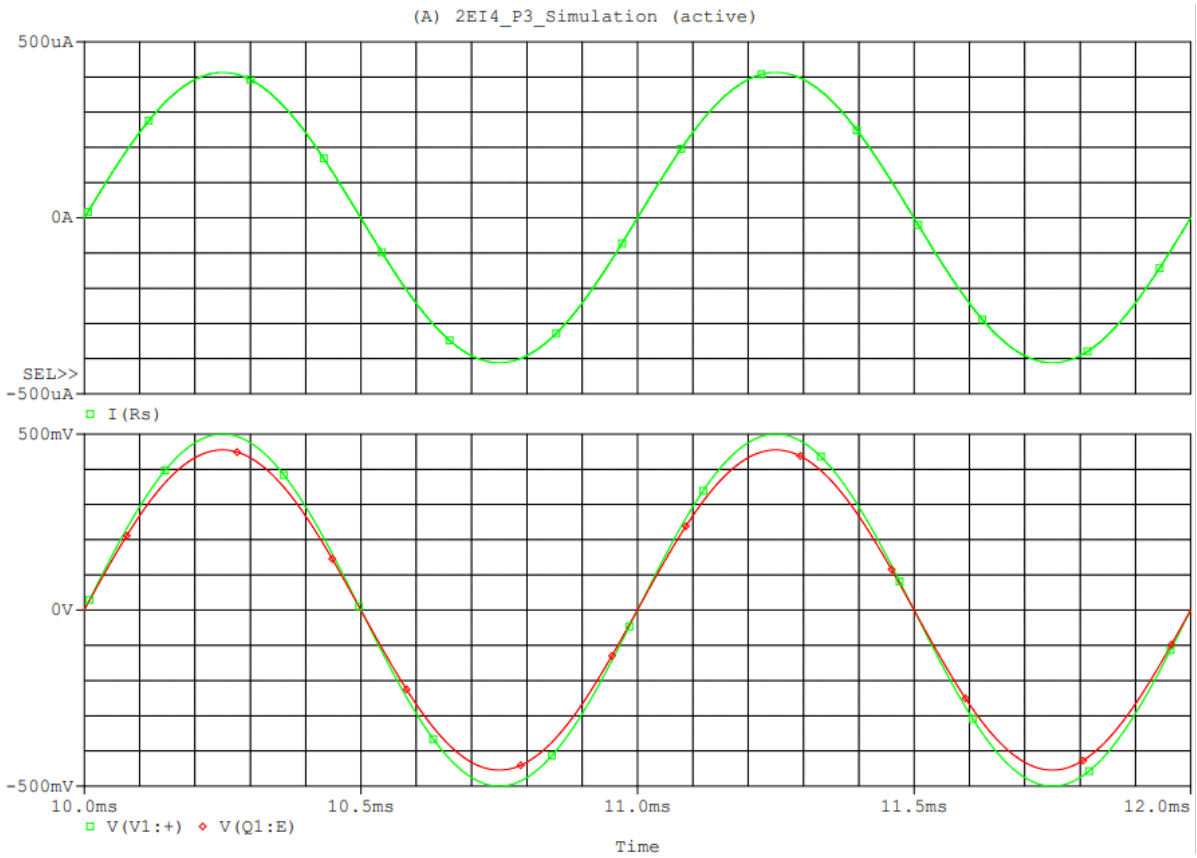


Figure 7: PSpice transient analysis Vin (Green) vs Vout (Red)

The PSpice schematic in figure 6 utilizes the PSpice library model for the 2N3904 NPN BJT. Additionally the PSpice simulation was done using a transient analysis over a time period of 20ms with a maximum step size of 100ns for finer detail. The PSpice simulation plots the sinusoidal input voltage as it oscillates from $-\ 0.5V$ to $+\ 0.5V$ (Frequency of 1kHz) as well as the output voltage across R_L. At the peaks of the input voltage the output voltage was able to achieve a maximum peak of $V_{out} = 0.456V$ (For $V_{in} = 0.5V$) and $V_{out} = -\ 0.456V$ (For $V_{in} = -\ 0.5V$). At these points the attenuation was the largest. Therefore, we can use these values and the equation $A_v = \frac{V_{out}}{V_{in}}$ to determine the maximum attenuation. The attenuation and input resistance were all checked in figure 8 below using the simulated values.

Peak points on the waveforms from both input and output voltages

$V_{in} = 0.5V : V_{out} = 0.456V$

$V_{in} = -0.5V : V_{out} = -0.456V$

Gain calculation

$A_v = \frac{V_{out}}{V_{in}} = \frac{0.456V}{0.5V} = 0.912$

Attenuation calculation

$Attenuation = (1 - gain) * 100 = (1 - 0.912) * 100 = 8.8\%$

Input resistance calculation

$R_{in} = \frac{V_{in}}{I_{in}}$

From the graph in figure 6 we can see that when $V_{in} = 0.5V$, $R_{in} = 412uA$

$R_{in} = \frac{V_{in}}{I_{in}} = \frac{0.5V}{412uA} = 1213.59\ \Omega$

As we can see this number closely resembles the input resistance we calculated all the way back in figure 3.

Figure 8: Checking the simulated gain, attenuation, and input resistance

Physical Circuit

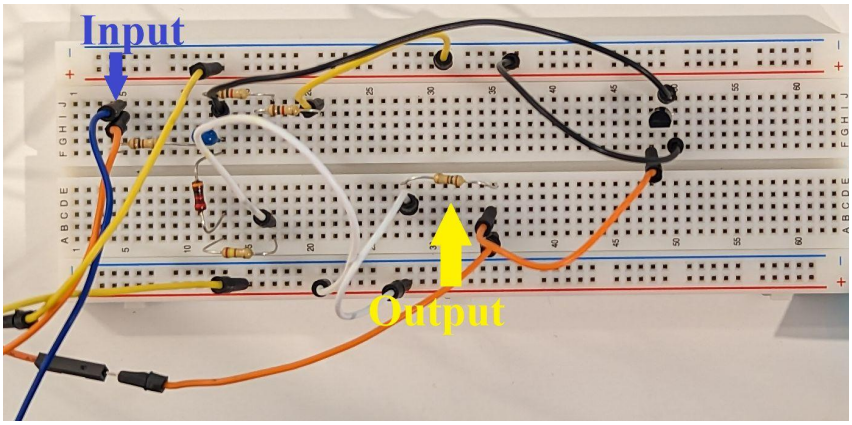


Figure 9: Common collector amplifier physical circuit

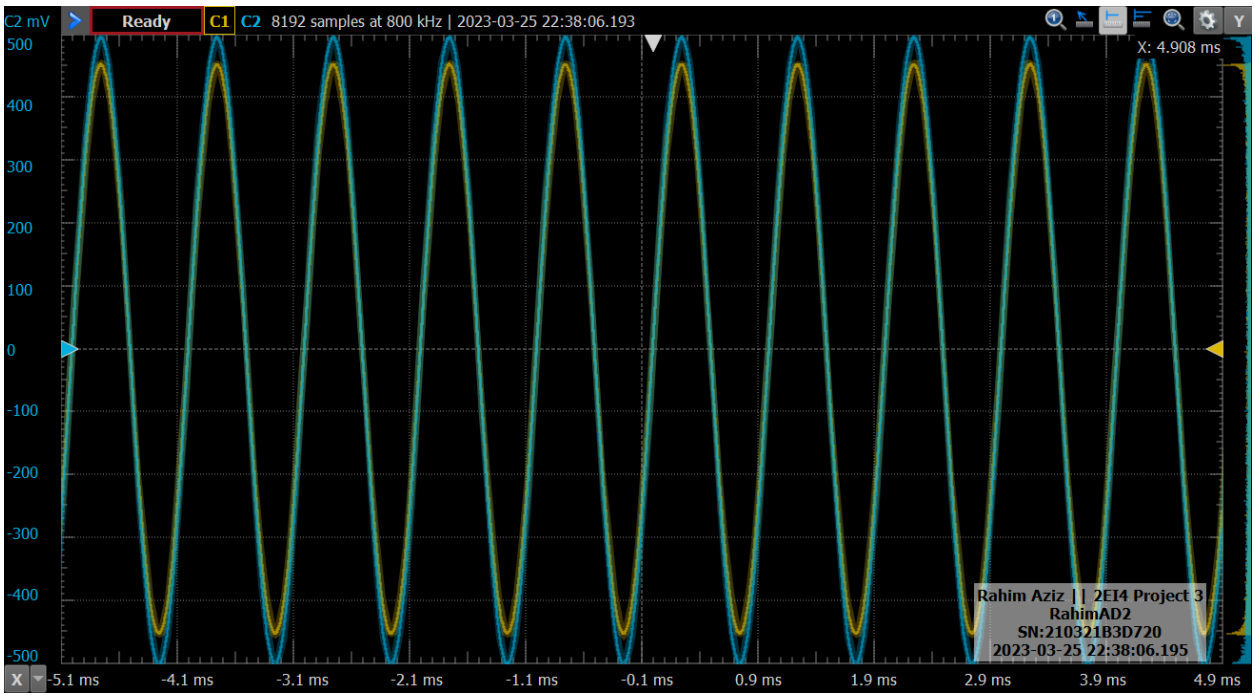


Figure 10: Physical circuit waveforms Vin (Blue) vs Vout (Yellow)

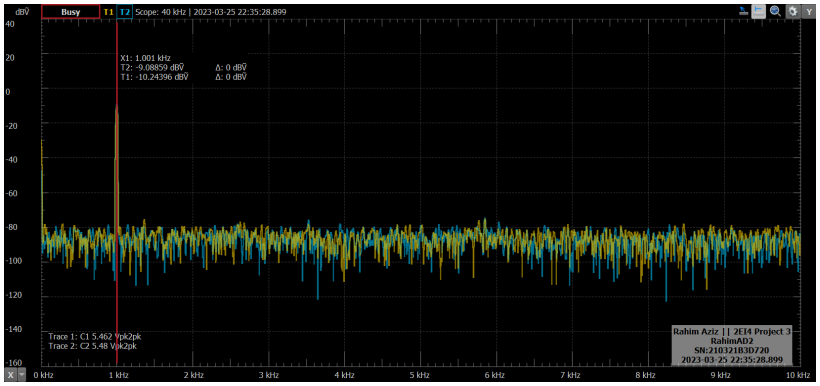


Figure 12: Spectrum analysis

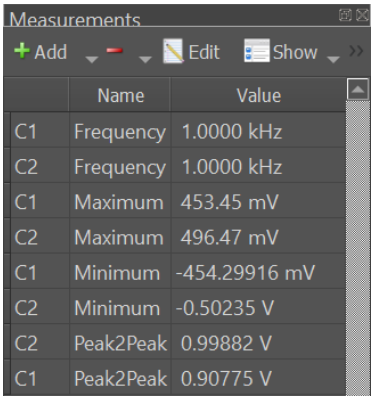


Figure 11: Circuit measurements

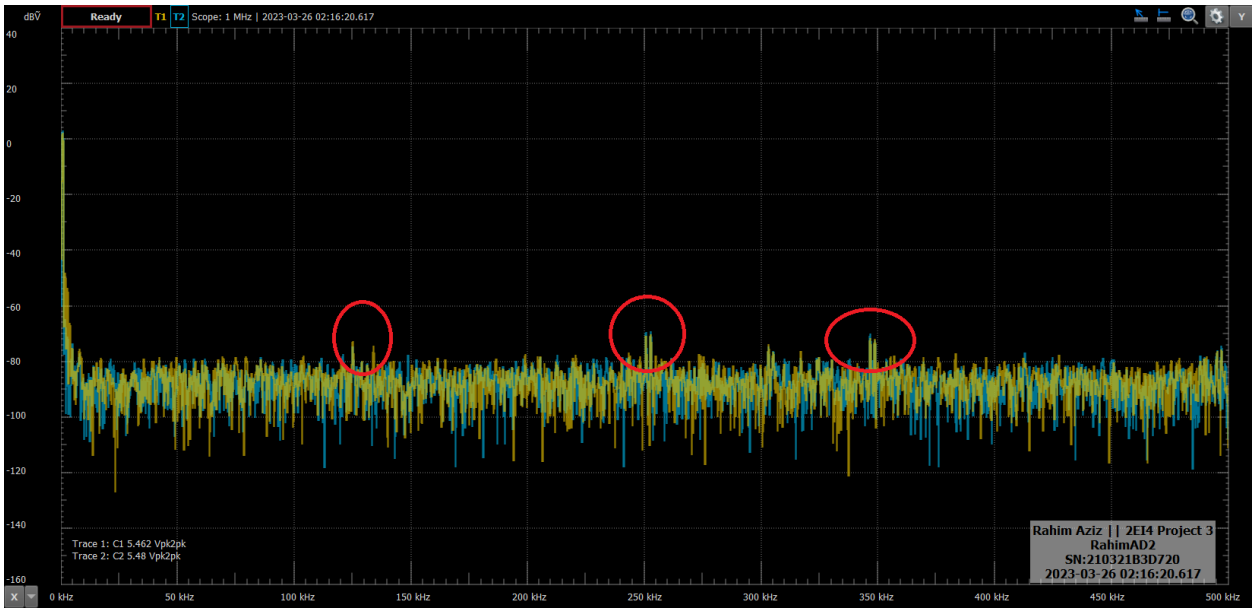


Figure 13: Spectrum Analyzer: Loss of Linearity for $V_{in} > 0.5V$

The physical circuit in figure 9 is composed of; $1 \times$ 2N3904 NPN BJT, $2 \times 100\Omega$ resistor, $1 \times 3k\Omega$ resistor, $2 \times 1k\Omega$, $1 \times 240\Omega$ resistor, and a single CM107 ($100uF$) capacitor. The input of the circuit was placed in series with the source resistance (100Ω) and capacitor. The input was a sinusoidal waveform with an amplitude of $0.5V$ and an frequency of $1kHz$. Additionally the AD2 power supply was used to supply the amplifier with both $+ 5V$ and $- 5V$. The output waveform was output voltage probed across the 100Ω load resistor. In figure 11 we can see that the output waveform achieved a positive peak of 453mV and a negative peak -454mV. Utilizing the gain equation ($A_v = \frac{V_{out}}{V_{in}}$) and the input voltages, we can determine the gain of this amplifier circuit.

$$A_v = \frac{V_{out}}{V_{in}} = \frac{453mV}{496mV} = 0.913$$

Figure 14: Gain calculation of the physical circuit

As seen from the calculation above, the constructed amplifier circuit successfully meets the project requirements of a gain ≥ 0.9 and an input voltage $v_{in} = |0.5V|$. Lastly, to prove the linearity capabilities of this amplifier the input and output voltages were plotted on a spectrum analyzer. On the spectrum analyzer we can see both waveforms are identical which is an indication of linearity. Additionally, in the spectrum analyzer graph we can see a spikes at $1kHz$ with a value of -6dBV which corresponds to our input of $0.5V$. Lastly, we can observe the linearity characteristics of the amplifier as we increase the input voltage past the project specifications. Figure 14 represents the spectrum analyzer for both input and output voltages when the input voltage is 1V. In this figure, there are visible spikes which represent noise and the lack of linearity in the amplifier when the amplifier leaves the region of amplification. This is due to the fact that the above amplifier circuit was designed with the specification that the input voltage would be $V_{in} \leq |0.5V|$

Data Sheet

2N3904→ LINK

References

[1] A. S. Sedra, K. C. Smith, T. C. Carusone, and V. Gaudet, Microelectronic circuits, 8th ed. New York, NY: Oxford University Press, 2019.