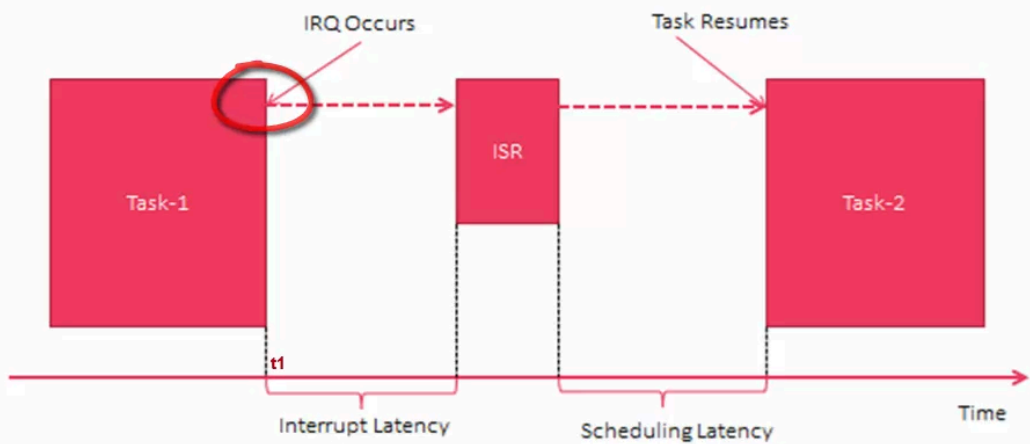




RTOS vs GPOS: Interrupt Latency



Udemy

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JS

Patch for cm7

21 [↑](#) [⋮](#)

[Jason](#) · [Lecture 36](#) · 2 years ago

My dev board has m7 core, will I need a different patch file? If I can use the provided patch, is there anything that needs to be modified?

12 replies

Follow replies



[Shishir](#) — Teaching Assistant

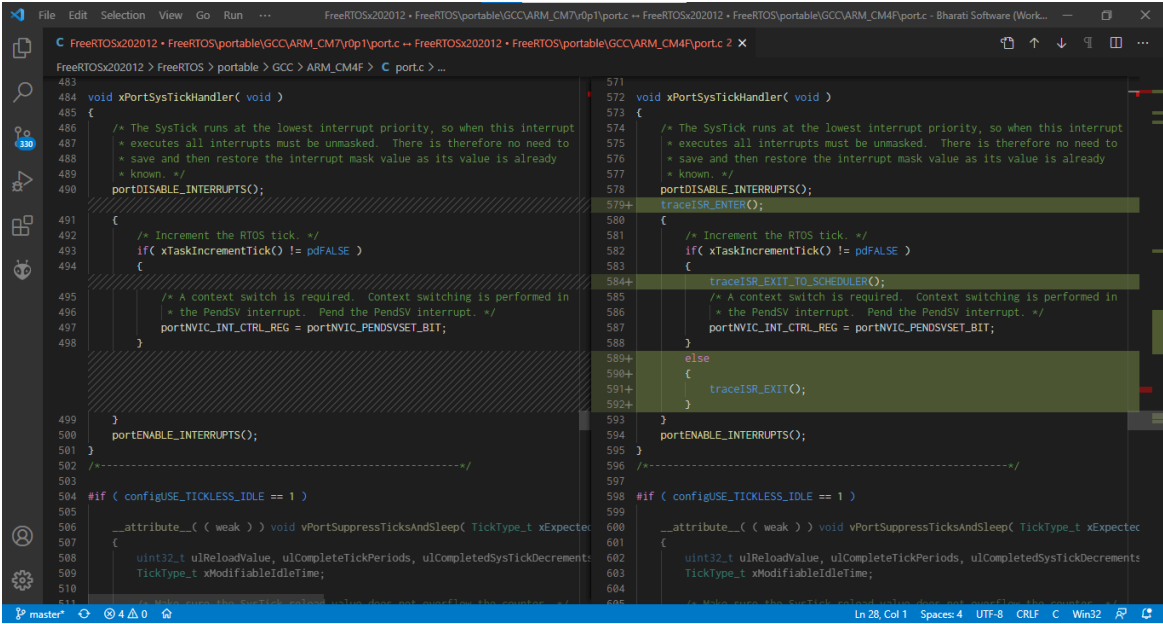
6 [↑](#) [⋮](#)

2 years ago

Jason,

The same patch might not work as the paths are different.

As *Section 4.7.5.1* of the [SEGGER SystemView User Guide](#) mentions, you can manually add the SystemView APIs.



Feel free to revert if you face issues.

Martynas

0 0

2 years ago

Jason, have you been able to modify patch for m7? Or manually add SystemView APIs, as Shishir suggested?

Jason

0 0

2 years ago

Thanks Shishir.

Jason

11 0

2 years ago

Hi Martynas,

Yes I ended up just changing the paths in the patch and it worked.

line 1 FreeRTOS/portable/GCC/ARM_CM7/r0p1/port.c

line 116 FreeRTOS/portable/GCC/ARM_CM7/r0p1/portmacro.h

You also have to add the following defines to port.c

```
/* Constants used to detect a Cortex-M7 r0p1 core, which should use the ARM_CM7
r0p1 port. */
```

```
#define portCPUID ( * ( ( volatile uint32_t *) 0xE000ED00 ) )
```

```
#define portCORTEX_M7_r0p1_ID ( 0x410C271 )
```

```
#define portCORTEX_M7_r0p0_ID ( 0x410C270 )
```

After doing that I couldn't get the timestamps working in SystemView even though I enabled the DWT_CTRL. I found that to have access to the DWT CYCCNT you need to add code below in main.c to enable the DWT (place after SystemClock_Config()) You need to unlock registers to gain access to them.

```
// Enable the CYCCNT counter
```

```
CoreDebug->DEMCR |= CoreDebug_DEMCR_TRCENA_Msk;
```

```
DWT->LAR = 0xC5ACCE55;
```

```
DWT->CYCCNT = 0;
```

```
DWT->CTRL |= DWT_CTRL_CYCCNTENA_Msk;
```

Here's the link where I got the code:
https://github.com/stm32duino/Arduino_Core_STM32/issues/371

Hope that helps.

MJ

[Martynas](#)

2 years ago

This helps a lot.
I changed paths to ARM_CM3 port files, added the defines and it worked.
Timestamps also seem to work, no additional unlocking of registers was required.

0

:

I owe you a beer.

JS

[Jason](#)

2 years ago

No Problem, happy to hear it helped.

0

:

DR

[Darien Savio](#)

2 years ago

Thanks a lot Jason. Worked like a charm

0

:

JS

[Jason](#)

2 years ago

No problem, good to hear Darien.

0

:

CR

[Christian](#)

2 years ago

Thank you Jason for your very valuable comments. It works fine with my NUCLEO-STM32F7

0

:

KA

[Kamil](#) Answer

2 years ago

At the moment when I'm writing this SEGGER company already has published patch for latest LTS version: FreeRTOS 202112.03-LTS. It works well with STM32F7 family. There is no need to integrate it manually. Just search for "FreeRTOSV10.4.zip" on SEGGER Wiki page (I cant paste direct link).

0

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SM

[Sourabh](#)

7 months ago

@Jason , this definition worked for me

#define portCORTEX_M7_r0p1_ID (0x410FC271)
#define portCORTEX_M7_r0p0_ID (0x410FC270)

0

:

RD

Rene

3 months ago

Hi, guys! I'm using an STM Nucleo board with a Cortex M0 and I've realized that the M0 doesn't have DWT. Do you know if it's possible to use SEGGER Viewer with the M0?

0

↑

⋮

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RA

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