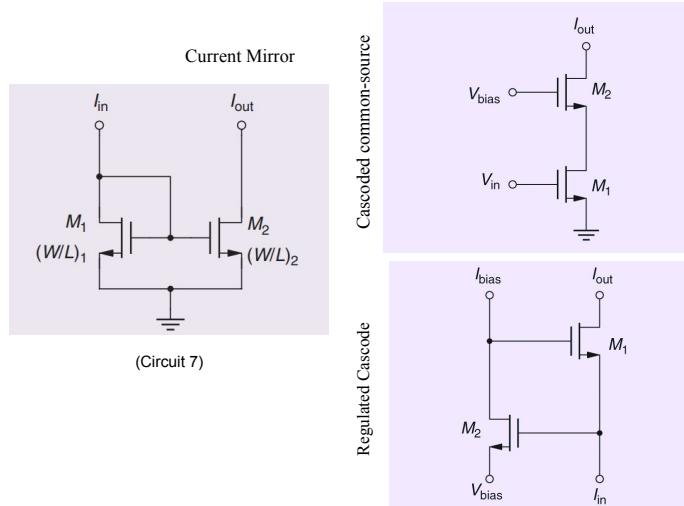


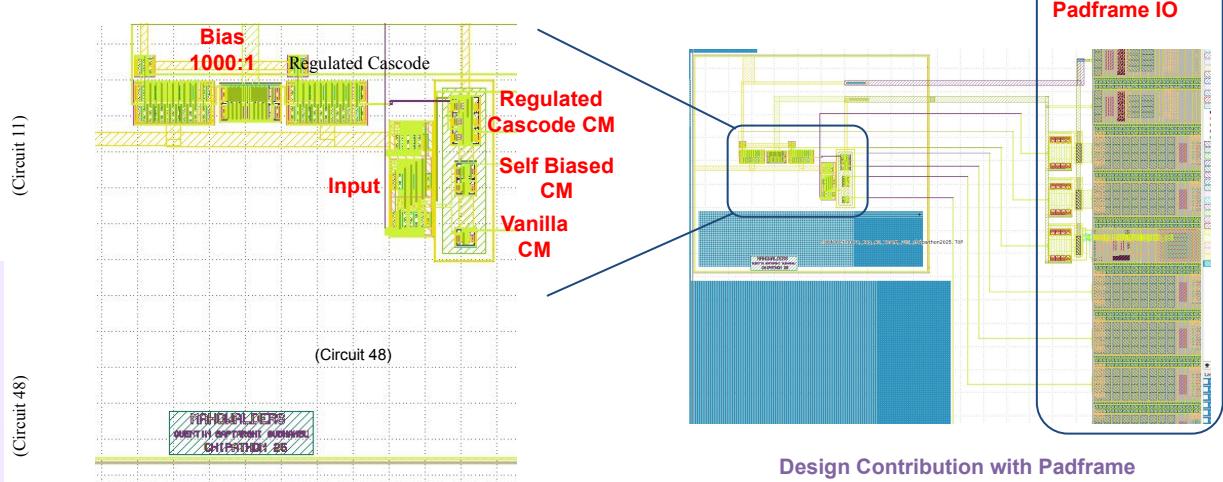
IEEE SSCS Chipathon 2025-24 : Team A3 – Mahowalders

Team M contributed the automated design and layout of a high-impedance current mirror block, parametrically instantiated via gLayout, enabling on-demand python2GDS automated layout generation. We tapped out three current mirror architectures:

- **Vanilla Current Mirror (VCM)**, as a reference
- **Self-Biased Common-Source CM (SB-CM)**, with improved impedance, moderate complexity
- **Regulated Cascode CM (RC-CM)**, with high output impedance, better stability, but requires auxiliary bias



Regulated Cascoded and other Current Mirrors



Status: DRC/LVS (w/o padframe) clean, Pre-PEX simulated, Taped-out in GF180

Lessons Learned and Best Practices

→ Lessons Learned:

- ◆ Design and Layout of mixed signal circuits with Open-source tools
- ◆ Utilization of the Python2GDS workflow in mixed signal design
- ◆ Progress Tracker is a must for collaborative and time-constrained projects
- ◆ Tapeout process (connecting the design to padring + generation of the Padring) after completion of layout can take as much time as the design/layout of the proposed circuit itself.

→ Things that Worked:

- ◆ Tutorials for various tools
- ◆ Setup for the development environment with IIC-OSIC Docker

→ Things that needs improvement:

- ◆ LVS Test with padring and other components like ESD Cells is must.
- ◆ Post Layout verification and Testing should be allocated more time
- ◆ Open-source DRC Decks and FAB DFM tests can have huge gaps. This possibility should be taken into consideration into Planning stage.
- ◆ Documentation for Open-source Tools

Feedback

- Favourite Part:
 - ◆ Weekly mentoring and interaction allows a unique look into expert perspectives that went into the art of design.
 - ◆ Different approaches to design
 - ◆ Collaboration with like-minded people from around the world.
- LLM/AI based Help: Interpreting the DRC/LVS errors in context of intended and physical designs
- Suggestions for Next year:
 - ◆ Synchronised Open-source DRC decks with actual Fab rules
 - ◆ Separate track-based optional meeting
 - ◆ Physical workshops for meeting with Chipathon collaborators
 - ◆ More clarity early-on the roadmap for the projects, padrings, allocated areas, floor planning etc.
 - ◆ More TAs for helping from previous chipathons