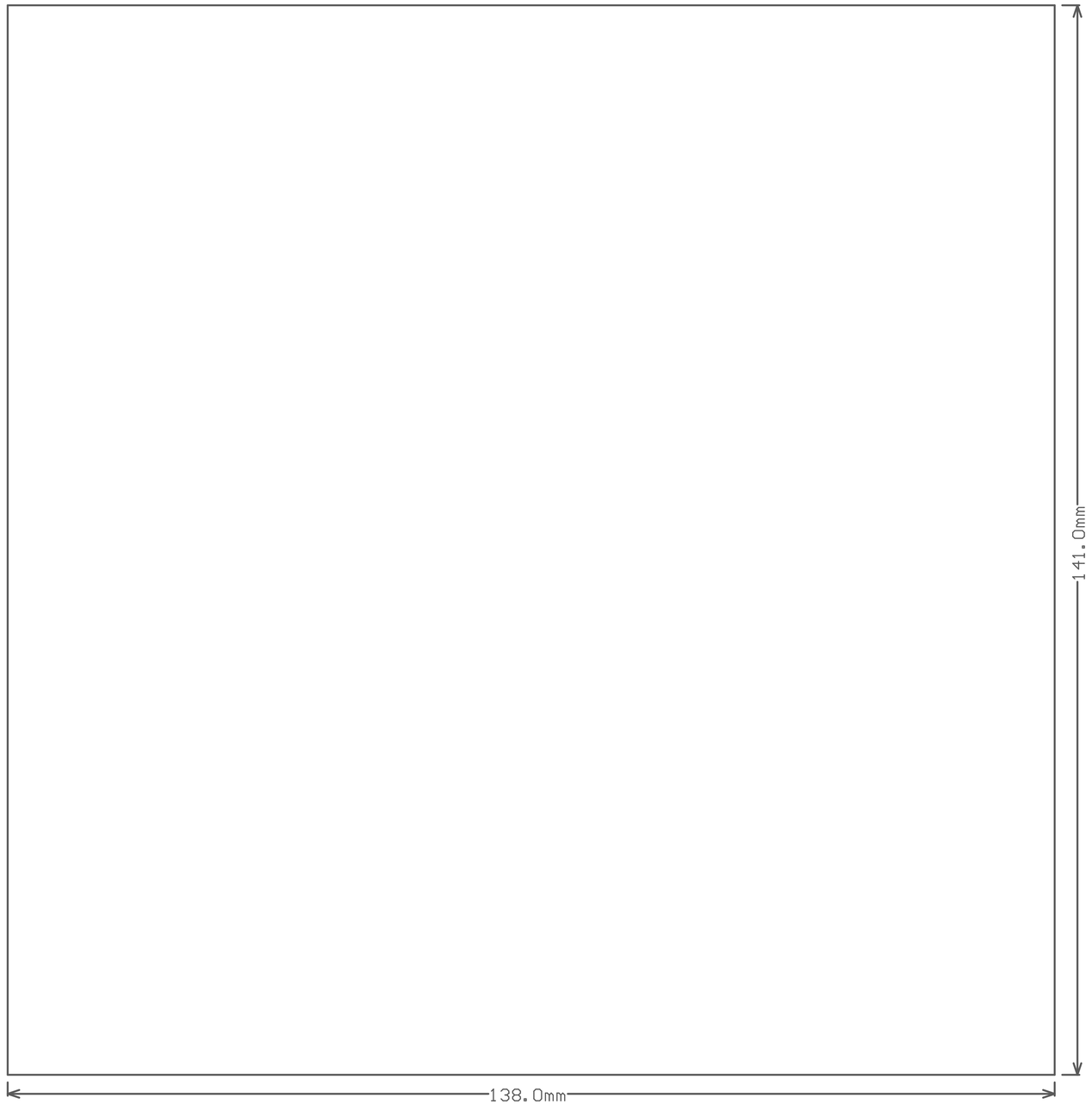

UW-IPMC TEST BOARD (revA)

Specifications:

1. Dielectric material is Tetrafunctional FR-4 with Tg > 170 C
2. Overall thickness is 1.6mm +/- 0.16mm
3. Controlled impedance: 50 ohm single-ended traces on all 8mil traces
4. All layers use 1/2 oz. copper (before plating)
5. Holes:
   a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
   b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
   c. All holes are exposed
   d. Drill locations are partioned into 3 separate drill files:
      * Plated-through holes
      * Non-Plated-through holes
      * Plated slots
6. Finish: immersion gold
7. Minimum observed signal layer clearances is 6 mils on layers 1 and 2
8. Solder Mask (SMOBC) to be applied to both top and bottom sides.
   Mask shall be photoimagable, with maximum thickness of 3 mils
9. Layers 2 and 3 are power planes and are INVERTED
10. Silkscreen to be applied to top side ONLY. Silkscreen shall be white ink
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
12. Combination of bow and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Testing:
   a. All layers to undergo optical inspection (machine-based) of all layers before lamination
   b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
      DC resistance shall be 10 ohms or less
   c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
   d. Impedance testing is NOT required
15. Locations in IPC-D-356A file are given in 2.4 English units

Layer Stackup

-- Layer 1 (Top, Signal)
-- Layer 2 (Power, GND)
-- Layer 3 (Power, 3.3V)
-- Layer 4 (Bottom, Signal)

Univ. of Wisconsin–Madison Madison, WI 53706	ENGINEER: Marcelo Vicente	TITLE: ZYNQ–IPMC and MMC test board	
	PCB DESIGNER: Marcelo Vicente		
	DATE: 24/03/2017	PART NO.:	REV: revA1
	FILE NAME: IPMC_TestBoard_PCB	DWG NO:	SCALE: 1:1