May 2019, datasheet revision B

ZYNQ-IPMC

Hardware Specification and General Information

1 DESCRIPTION

ZYNQ-IPMC is a high versatile open-source self-contained Intelligent Platform Management Controller (IPMC) in a miniDIMM-244 mezzanine form factor with extended monitoring features targeted for Advance Telecommunications Computing Architecture (ATCA) applications in accordance with the PICMG 3.x standard.

2 FEATURES

- Self-contained IPMI compliant platform for ATCA applications:
  - Field-replaceable unit (FRU) information
  - Fault detection and reporting
  - MMC support via IPMB
- Extended monitoring and features:
  - Sub-millisecond fault response
  - Parallel sensor reading
  - Standard protocol support on GPIOs
  - Hardware accelerated feedback
- Single 3.3V supply and interfaces
- Open-source and NDA-free HW/FW/SW

3 HARDWARE

- Powered by Xilinx Zynq-7020 or Z014S System-on-Chip (SoC)
  - Single-core or Dual-core ARM Cortex-A9 (667 MHz)
  - 256Mbytes of DDR3-1066 memory
  - 64Mbytes of QSPI flash storage
- 256Kbit EEPROM storage w/ unique MAC
- 1Gb ethernet w/ on-board transformers
- 109 fully configurable GPIOs
- 16 ADC inputs w/ 16-bit @ 10kSPS channel
- Master JTAG and UART interfaces

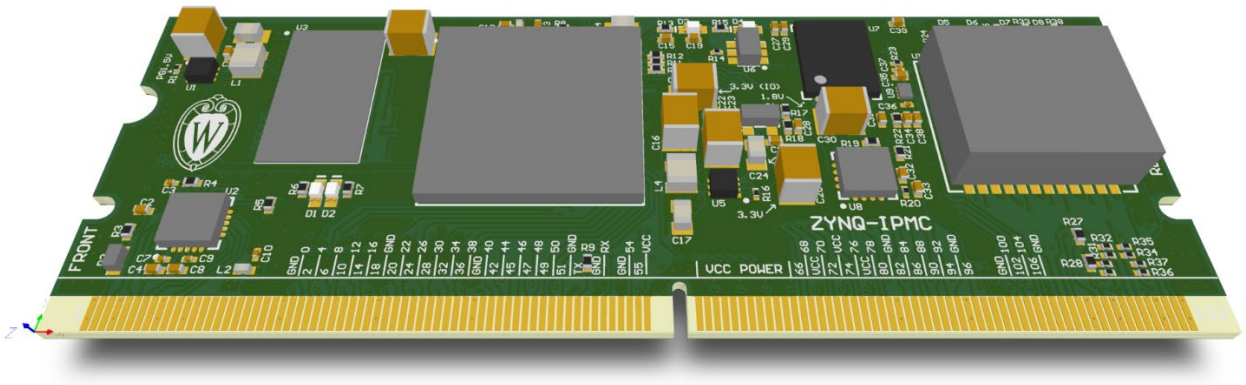

Figure 3.1 ZYNQ-IPMC (revB) rendering

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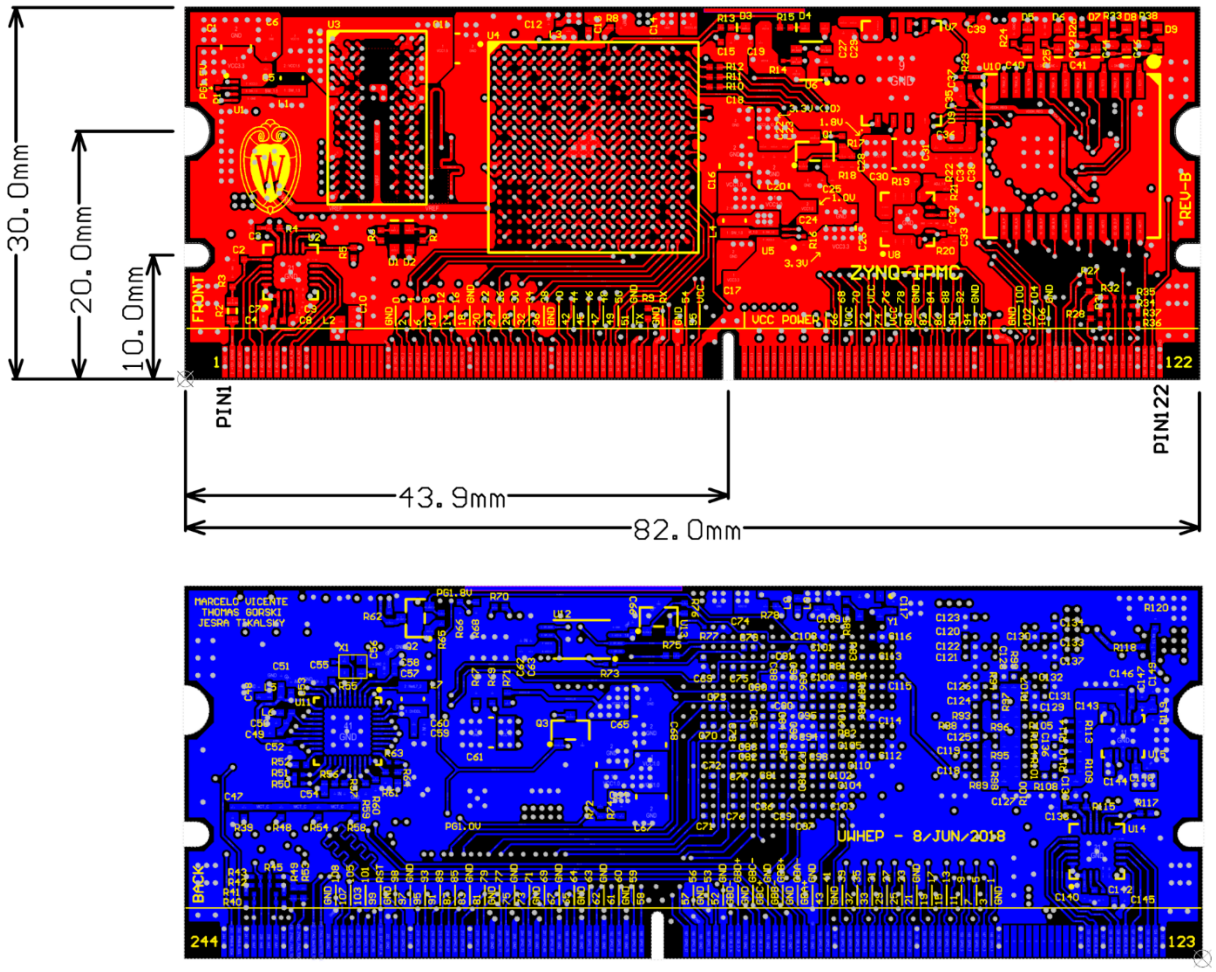
5 REVISION HISTORY

Revision B (May 2019):

- Adds measurements for power consumption for both Z7020 and Z7014S variants.
- Removes ‘DRAFT’ watermark, document no longer preliminary.

6 PIN CONFIGURATION AND FUNCTION

The following illustration is a representation of the ZYNQ-IPMC, as seen from the top (red) and bottom (blue) view.



6.1 PINS BY FUNCTION

Table 6.1 Pin type symbol definitions

SYMBOL	PIN TYPE	DESCRIPTION
A	Analog input	Analog input for sensing variable voltage levels
DIFF	Differential	Differential signal pair
I	Input	Input signal
I-PU	Input w/ pull-up	Input signal with on-board pull-up
I-PD	Input w/ pull-down	Input signal with on-board pull-down
O	Output	Output signal
I/O	Bidirectional	Bidirectional input or output signal

Table 6.2 Pins by Function

GROUP	NAME	PIN NUMBER(S)	TYPE	LEVEL	DESCRIPTION
Power	VCC	65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 80, 83, 86	-	3.3V	Main 3.3V supply
	GND	1, 4, 9, 12, 23, 34, 45, 55, 59, 62, 89, 97, 102, 107, 111, 114, 119, 122, 123, 126, 131, 134, 145, 156, 167, 170, 173, 176, 179, 182, 185, 190, 193, 196, 199, 202, 205, 208, 211, 219, 222, 230, 233, 236, 241, 244	-	-	Logic ground
Analog	12V_SENSE	2	A	12.0V	+12V sensing
	ADC-A_IN[1-7]	3, 5, 6, 7, 8, 10, 11	A	2.5V	Bank A analog sensing
	ADC-B_IN[0-7]	124, 125, 127, 128, 129, 130, 132, 133	A	2.5V	Bank B analog sensing
GPIO	GPIO_[0-108]	24, 146, 25, 147, 26, 148, 27, 149, 28, 150, 29, 151, 30, 152, 31, 153, 32, 154, 33, 155, 35, 157, 36, 158, 37, 159, 38, 160, 39, 161, 40, 162, 41, 163, 42, 164, 43, 165, 44, 166, 46, 168, 47, 169, 48, 49, 50, 51, 52, 53, 54, 55,183, 184, 54, 55, 186, 187, 188, 189, 191, 192, 194, 195, 197, 198, 78 , 200, 79, 201, 81, 203, 82, 204, 84, 206, 85, 207, 87, 209, 88, 210, 90, 212, 91, 213, 92, 214, 93, 215, 94, 216, 95, 217, 96, 218, 98, 220, 221, 224, 103, 225, 104, 226, 105, 227, 106, 228, 229	I/O	3.3V	General purpose input-outputs that can be configured to any standard or custom protocol
Ethernet	GB_A_[P,N]	171, 172	DIFF	2.5V	4-pair 1000BASE-T 1Gb ethernet after magnetics
	GB_B_[P,N]	174, 175	DIFF		
	GB_C_[P,N]	177, 178	DIFF		
	GB_D_[P,N]	180, 181	DIFF		
UART	UART_TX	57	O	3.3V	Serial console
	UART_RX	60	I		
Reset	EXT_RST_N	223	I-PU	3.3V	External reset, asserted low
Master JTAG	M-JTAG_TRST	108	O	3.3V	Master JTAG interface, drives a JTAG chain
	M-JTAG_TDO	109	I		
	M-JTAG_TMS	110	O		
	M-JTAG_TCK	231	O		
	M-JTAG_TDI	232	O		
ZYNQ JTAG	Z-JTAG_TDO	112	O	3.3V	Slave JTAG interface for Zynq firmware debugging and GDB access
	Z-JTAG_TMS	113	I-PU		
	Z-JTAG_TCK	234	I-PU		
	Z-JTAG_TDI	235	I-PU		

Address	HA[0-7] (1)	115, 237, 116, 238, 117, 239, 118, 240	I-PU	1.8V	ATCA hardware address interface
IPMI Bus	IPMB-A_SCL	120	I/O	3.3V	IPMI bus interface, channel A
	IPMB-A_SDA	121	I/O		
	IPMB-B_SCL	242	I/O		IPMI bus interface, channel B
	IPMB-B_SDA	243	I/O		
-	NC	13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 58, 61, 99, 100, 101, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144	-	-	No connection

7 SPECIFICATIONS

7.1 ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range

Table 7.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	3.6	V
V_{IN}	Logic pin input voltage range (GPIO, UART, IPMI, etc.)	-0.4	V_{CC}+0.55	V
V_{ADC}	Analog sense input range	-0.1	2.6	V

7.2 RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range

Table 7.2 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		-0.2	3.3	3.45	V
V_{IN}	Logic pin input voltage as LVCMOS33	Logic LOW	-0.3	-	0.8	V
		Logic HIGH	2.0	-	3.45	V
V_{OUT}	Logic pin output voltage as LVCMOS33	Logic LOW	-	-	0.4	V
		Logic HIGH	V_{CC}-0.4	-	V_{CC}	V
I_{OUT}	Maximum logic pin output current		-	-	16.0	mA
I_{IN}	Maximum current in a logic pin when forward biasing the clamp diode		-	-	10.0	mA
V_{ADC}	Standard analog sensing pins voltage range		0.0	-	2.5	V
$V_{ADC-12V}$	+12V sensing pin voltage range		0.0		14.1	V
F_{ADC}	Analog sensing sampling frequency				10	kHz
P_{IN}	Total power consumption[2]	Z7020	-	2.15	-	W
		Z7014S	-	1.95	-	W

[1] Hardware Address pins should not be driven, instead they should be left floating or connected to GND.
[2] Obtained from real measurements using an IPMC testboard.

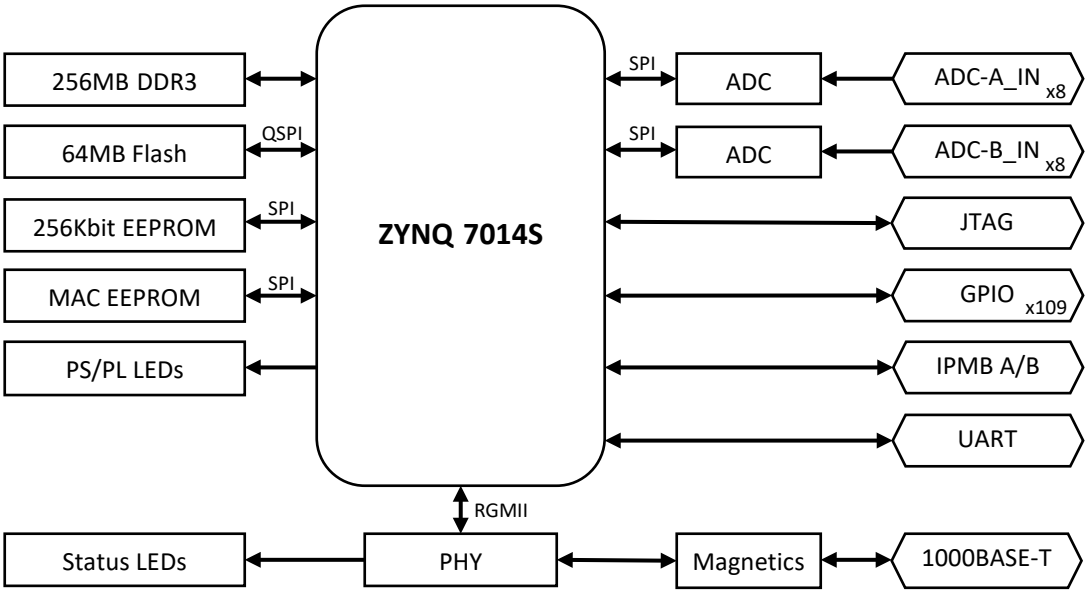
7.3 TIMING CHARACTERISTICS

based on PCB routing

Table 7.3 Timing Characteristics

			TYP	UNIT
$t_{\Delta ETH-DIFF}$	Propagation delay between ethernet differential P and N signals	Pair A	1.8	ps
		Pair B	0.6	ps
		Pair C	-5.8	ps
		Pair D	-5.5	ps
$t_{\Delta ETH-PAIRS}$	Maximum propagation delay between ethernet pairs	B to D	40.1	ps
f_{ADC}	Maximum analog sensing sampling frequency		10.0	kHz

8 ARCHITECTURE



8.1 PROGRAMABLE AND STATUS LEDS

A total of 9 LEDs are present on-board as seen in Figure 8.1. Table 8.1 as a brief description.

Table 8.1 On-board LED description

LED #	NAME	COLOR	DRIVER	DESCRIPTION
1	PS_LED_RED	Red	Zynq PS	Programmable from the Zynq Processing System (PS)
2	PS_LED_YELLOW	Yellow	Zynq PS	
3	POWER_ON	Green	Power Supply	Indicates the card has power
4	POWER_GOOD	Green	Power Supply	Indicates a good power sequencing
5	ETH_10_100	Yellow	Ethernet Phy	100M link when active, 10M otherwise

6	ETH_1000	Green	Ethernet Phy	1000M when active, ETH_10_100 off
7	ETH_ACT	Red	Ethernet Phy	Active link when on, activity when blinking
8	PL_LED_RED	Red	Zynq PL	Usable from the Zynq Programable Logic (PL)
9	PL_LED_YELLOW	Yellow	Zynq PL	

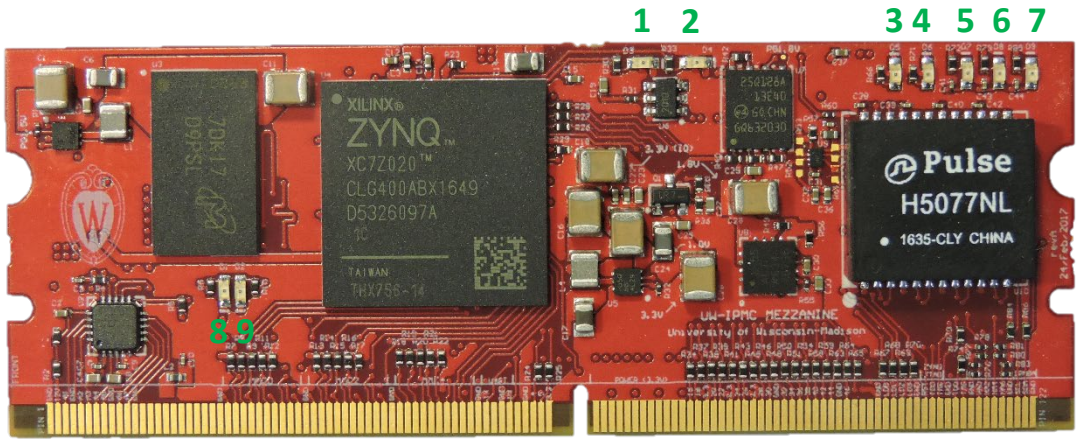


Figure 8.1 On-board LED locations

9 ATCA REQUIREMENTS

9.1 MICROSWITCH

A handle switch can be used to turn on and off the blade payload as shown in section D.1.1 of PICMG 3.0. Any available GPIO can be used to interface with microswitch being used. An external pull-up of 1kΩ or less is recommended to assert the signal when the switch is open as seen in Figure 9.1.

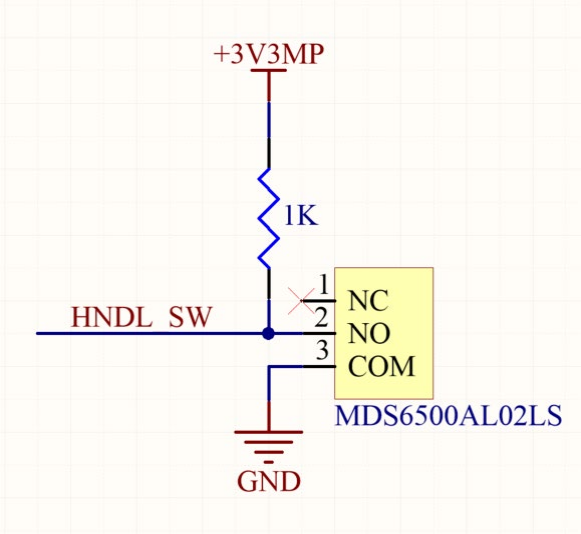


Figure 9.1 Microswitch Interface

9.2 HARDWARE ADDRESS

The hardware address is set in accordance with PICMG 3.0 REQ 3.37: “Each IPM Controller in the Shelf shall be assigned a seven (7) bit Hardware Address and a corresponding odd parity bit that are “hardwired” at each FRU location on the Backplane or elsewhere in the Shelf. The FRU location shall indicate a logic one by leaving the address pin floating. A logic zero shall be indicated by connecting the address pin to the Logic Ground.”

Hardware Address pins are to be connected directly to the ATCA blade Zone-1 hardware address pins.

9.3 IPMB A/B

IPMB A and B channels are available in accordance with PICMG 3.0 REQ 3.543: “IPM Controllers shall implement connections to IPMB-A and IPMB-B”.

IPMB interfaces are to be connected directly to the ATCA blade Zone-1 IPMB A/B pins.

9.4 LEDS

Face Plate indications are described in section 3.2.5 of PICMG 3.0. These correspond to LED interfaces and should be connected to any available GPIO since assignment and configuration takes places in firmware.

These LEDs are recommended to be powered by the 3.3V management power (MP) source while being biased by 332Ω resistors as seen in Figure 9.2.

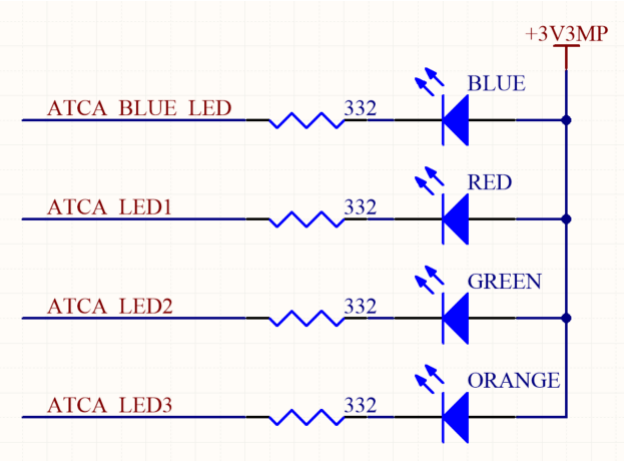


Figure 9.2 ATCA LED Interface

10 DESIGN CONSIDERATIONS

10.1 ANALOG INPUTS

Analog sensing connections need to be dimensioned by having two factors in consideration: the maximum allowed voltage of 2.5V on analog sensing pins and the Nyquist frequency of 5kHz based on the sampling rate of 10kHz. In most cases a voltage divider is required between the analog pin and the and the signal, as shown in Figure 10.1.

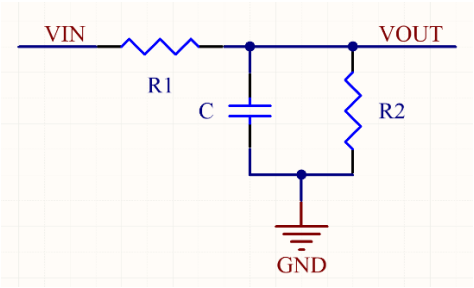


Figure 10.1 Voltage divider

$$V_{OUT} = V_{IN} \cdot \frac{R2}{R1+R2} \qquad f_C = \frac{1}{2\pi \cdot R1 \cdot C}$$

Table 10.1 Example divider circuit values

INPUT VOLTAGE (V)	R1 (Ω)	R2 (Ω)	C (uF)	DIVIDER FACTOR	NOM. OUTPUT VOLTAGE (V)	MAX. INPUT VOLTAGE (V)	CUTOFF FREQ (Hz)
5.00	4640	3320	0.1	0.417	2.09	5.99	343
3.30	2740	4640	0.22	0.629	2.08	3.98	264
2.50	1000	4640	1.0	0.823	2.06	3.04	159
1.20	100	-	10.0	1.000	1.20	2.50	159

10.2 ETHERNET

Four differential pairs provide a 1000BASE-T ethernet connectivity. On-board magnetics are present on the IPMC and therefore these are not required externally. Each pair should be length matched and routed with 100Ω differential traces.

10.3 GENERAL PURPOSE I/O (GPIO)

All 109 available GPIOs are connected to Zynq's Programming Logic (PL) which allows for easy implementation of most standard protocols (SPI, I2C, UART, etc) as well as other custom interfaces. Individual GPIOs can be internally configured to be pulled-up, pulled-down and be internally terminated while supporting TTL and LVCMOS logic levels.

GPIOs are divided into 3 majors banks, highlighted in green, orange and blue in Figure 13.1, Table 13.1 and Table 13.2.

Table 10.2 GPIOs Banking

BANK COLOR	BANK NUMBER	GPIO COUNT	GPIO NUMBER
Green	13	15	0, 2, 4, 6, 8, 10, 12, 14, 16, 18, 41, 43, 52-54
Orange	34	49	1, 3, 5, 7, 9, 11, 13, 15, 17, 19-40, 42, 44-51, 55-63
Blue	35	45	64-108

It is recommended that for moderate speed protocols the same bank is used to define the interface since this will facilitate internal FPGA routing, simplify clocking and improve signal quality. For protocols that require clock reception it is recommended to use a clock capable GPIO as indicated in Table 13.2**.**

10.4 Master JTAG

Dedicated pins provide a JTAG Master interface that can drive other JTAG capable devices. The IPMC will support Xilinx Virtual Cable (XVC) through TCP/IP.

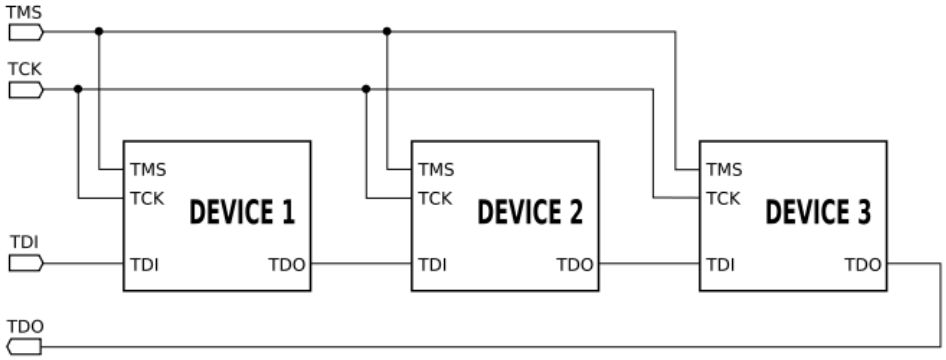


Figure 10.2 Example JTAG chain implementation (from Wikipedia)

10.5 Debugging JTAG

A standard Xilinx JTAG header is recommended to be present and connected to these pins, or any other alternative approach. JTAG access greatly facilitates debugging and development of custom IPMC builds.

No pull-ups are required externally on input lines.

10.6 IPMC Reset

An external reset of the IPMC can be issued by pulling down EXT_RST_N to ground. It is recommended to leave this pin floating or connect it to a push bottom that sets the logic state to logic ground when pressed.

11 Mechanical and Mating

A miniDIMM DDR3 surface mount socket with 22.5 degrees insertion angle is recommended due to height restrictions imposed by PICMG 3.0 REQ 2.19: “Including tolerance accumulations, the maximum

height of components (other than Component Side 1 covers or components under those Component Side 1 covers) in a single-Slot Front Board shall be 21.33 mm.". This will assure that the IPMC won't exceed the ATCA height envelope. Two Molex connectors are recommended:

- Molex 87783-0301 (IPMC front facing up)
- Molex 78035-0301 (IPMC front facing down)

Components are allowed under the IPMC but their height should be taken into consideration.

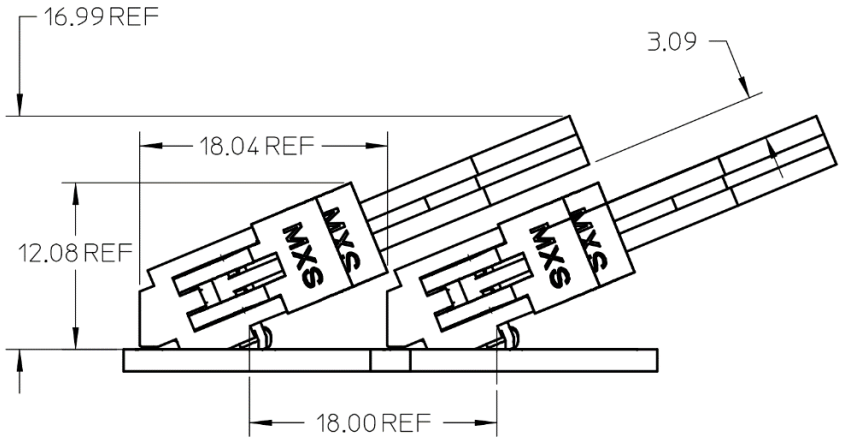


Figure 11.1 Molex 87783-0301 side view

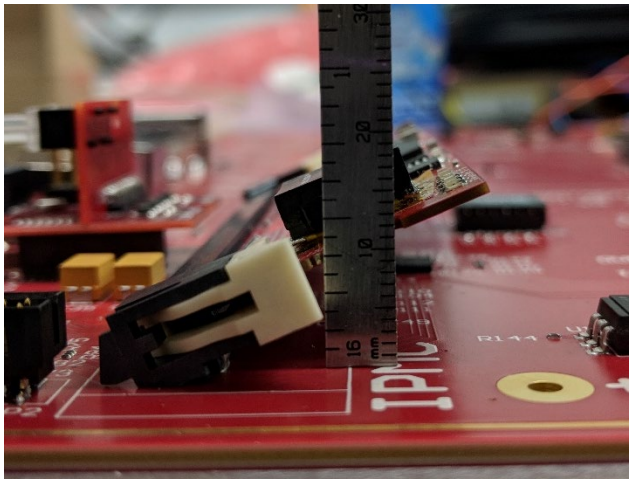


Figure 11.2 IPMC height measurement

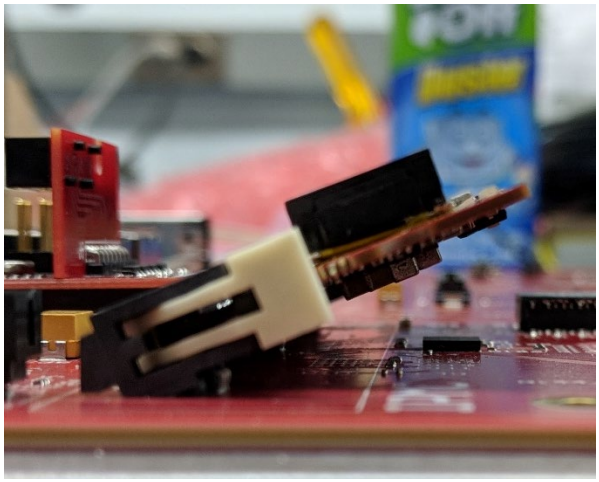


Figure 11.3 Observable clearance from IPMC to main board

12 FUTURE TOPICS

Items planned to be added in a later revision of this document:

- Detailed architecture description (Ethernet PHY, ADCs, power sequencing, etc.)

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- Operation Conditions -> Power consumption
- ATCA Interfaces -> MMC

13 APPENDIX

13.1 SCHEMATIC SYMBOL

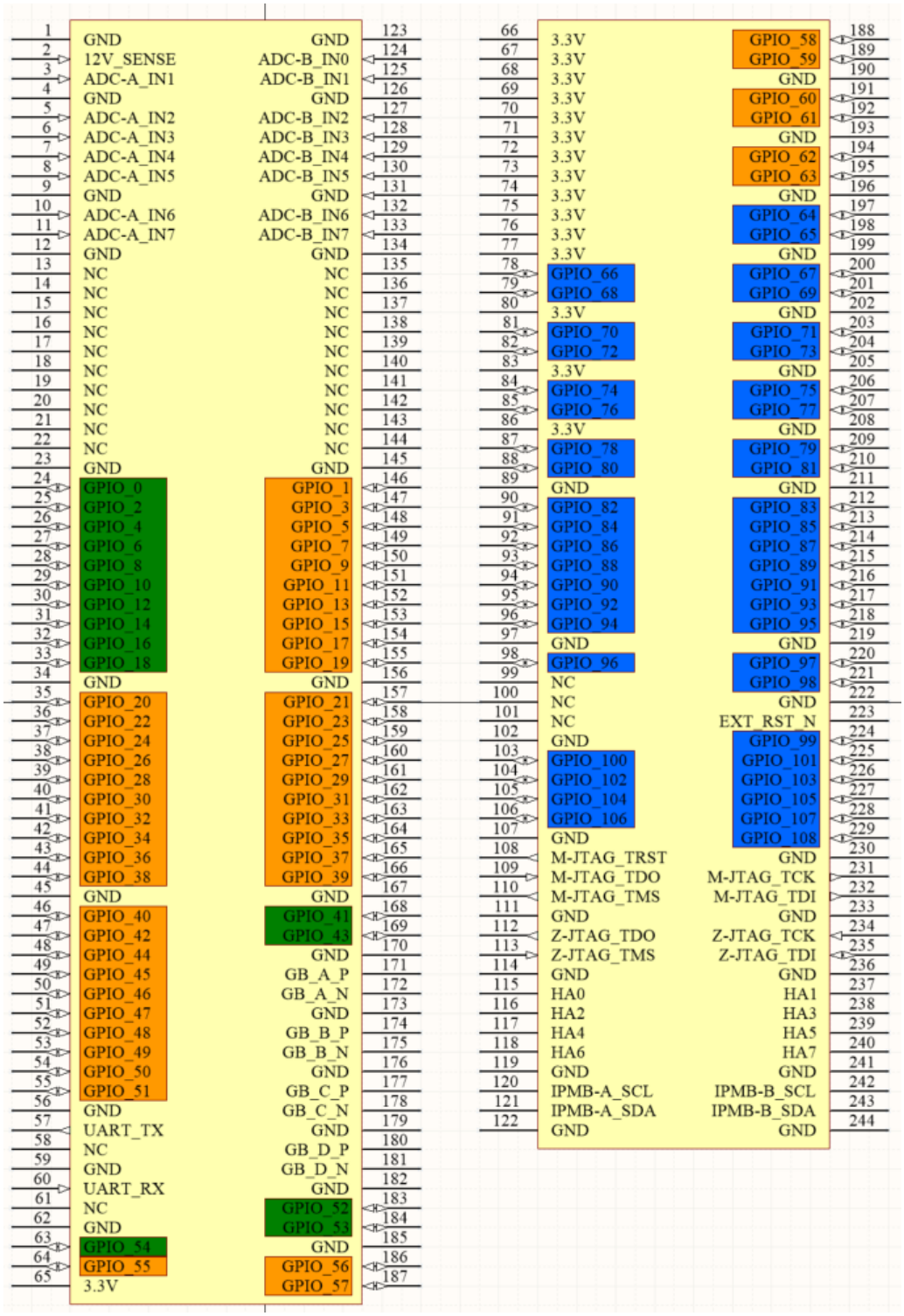

Figure 13.1 Altium Schematic Symbol

13.2 Pin Assignment by Location

Table 13.1 Pin assignment by Location

NAME	PIN	PIN	NAME
GND	1	123	GND
+12V_SENSE	2	124	ADC-B_IN0
ADC-A_IN1	3	125	ADC-B_IN1
GND	4	126	GND
ADC-A_IN2	5	127	ADC-B_IN2
ADC-A_IN3	6	128	ADC-B_IN3
ADC-A_IN4	7	129	ADC-B_IN4
ADC-A_IN5	8	130	ADC-B_IN5
GND	9	131	GND
ADC-A_IN6	10	132	ADC-B_IN6
ADC-A_IN7	11	133	ADC-B_IN7
GND	12	134	GND
NC	13	135	NC
NC	14	136	NC
NC	15	137	NC
NC	16	138	NC
NC	17	139	NC
NC	18	140	NC
NC	19	141	NC
NC	20	142	NC
NC	21	143	NC
NC	22	144	NC
GND	23	145	GND
GPIO_0	24	146	GPIO_1
GPIO_2	25	147	GPIO_3
GPIO_4	26	148	GPIO_5
GPIO_6	27	149	GPIO_7
GPIO_8	28	150	GPIO_9
GPIO_10	29	151	GPIO_11
GPIO_12	30	152	GPIO_13
GPIO_14	31	153	GPIO_15
GPIO_16	32	154	GPIO_17
GPIO_18	33	155	GPIO_19
GND	34	156	GND
GPIO_20	35	157	GPIO_21
GPIO_22	36	158	GPIO_23
GPIO_24	37	159	GPIO_25
GPIO_26	38	160	GPIO_27
GPIO_28	39	161	GPIO_29
GPIO_30	40	162	GPIO_31

NAME	PIN	PIN	NAME
VCC3.3	66	188	GPIO_58
VCC3.3	67	189	GPIO_59
VCC3.3	68	190	GND
VCC3.3	69	191	GPIO_60
VCC3.3	70	192	GPIO_61
VCC3.3	71	193	GND
VCC3.3	72	194	GPIO_62
VCC3.3	73	195	GPIO_63
VCC3.3	74	196	GND
VCC3.3	75	197	GPIO_64
VCC3.3	76	198	GPIO_65
VCC3.3	77	199	GND
GPIO_66	78	200	GPIO_67
GPIO_68	79	201	GPIO_69
VCC3.3	80	202	GND
GPIO_70	81	203	GPIO_71
GPIO_72	82	204	GPIO_73
VCC3.3	83	205	GND
GPIO_74	84	206	GPIO_75
GPIO_76	85	207	GPIO_77
VCC3.3	86	208	GND
GPIO_78	87	209	GPIO_79
GPIO_80	88	210	GPIO_81
GND	89	211	GND
GPIO_82	90	212	GPIO_83
GPIO_84	91	213	GPIO_85
GPIO_86	92	214	GPIO_87
GPIO_88	93	215	GPIO_89
GPIO_90	94	216	GPIO_91
GPIO_92	95	217	GPIO_93
GPIO_94	96	218	GPIO_95
GND	97	219	GND
GPIO_96	98	220	GPIO_97
NC	99	221	GPIO_98
NC	100	222	GND
NC	101	223	EXT_RST_N
GND	102	224	GPIO_99
GPIO_100	103	225	GPIO_101
GPIO_102	104	226	GPIO_103
GPIO_104	105	227	GPIO_105

GPIO_32	**41**	**163**	GPIO_33
GPIO_34	**42**	**164**	GPIO_35
GPIO_36	**43**	**165**	GPIO_37
GPIO_38	**44**	**166**	GPIO_39
GND	**45**	**167**	GND
GPIO_40	**46**	**168**	GPIO_41
GPIO_42	**47**	**169**	GPIO_43
GPIO_44	**48**	**170**	GND
GPIO_45	**49**	**171**	GB_A_P
GPIO_46	**50**	**172**	GB_A_N
GPIO_47	**51**	**173**	GND
GPIO_48	**52**	**174**	GB_B_P
GPIO_49	**53**	**175**	GB_B_N
GPIO_50	**54**	**176**	GND
GPIO_51	**55**	**177**	GB_C_P
GND	**56**	**178**	GB_C_N
UART_TX	**57**	**179**	GND
NC	**58**	**180**	GB_D_P
GND	**59**	**181**	GB_D_N
UART_RX	**60**	**182**	GND
NC	**61**	**183**	GPIO_52
GND	**62**	**184**	GPIO_53
GPIO_54	**63**	**185**	GND
GPIO_55	**64**	**186**	GPIO_56
VCC3.3	**65**	**187**	GPIO_57

GPIO_106	**106**	**228**	GPIO_107
GND	**107**	**229**	GPIO_108
M-JTAG_TRST	**108**	**230**	GND
M-JTAG_TDO	**109**	**231**	M-JTAG_TCK
M-JTAG_TMS	**110**	**232**	M-JTAG_TDI
GND	**111**	**233**	GND
Z-JTAG_TDO	**112**	**234**	Z-JTAG_TCK
Z-JTAG_TMS	**113**	**235**	Z-JTAG_TDI
GND	**114**	**236**	GND
HA0	**115**	**237**	HA1
HA2	**116**	**238**	HA3
HA4	**117**	**239**	HA5
HA6	**118**	**240**	HA7
GND	**119**	**241**	GND
IPMB-A_SCL	**120**	**242**	IPMB-B_SCL
IPMB-A_SDA	**121**	**243**	IPMB-B_SDA
GND	**122**	**244**	GND

13.3 GPIO BANKING AND ASSIGNMENT

Table 13.2 GPIO-Zynq assignment

GPIO	IPMI PIN	BANK	ZYNQ PIN	CLOCK INPUT?
0	24	13	U5	-
1	146	34	P14	-
2	25	13	T5	-
3	147	34	T10	-
4	26	13	U8	-
5	148	34	T11	-
6	27	13	U9	-
7	149	34	T12	-
8	28	13	W8	-
9	150	34	T14	-
10	29	13	W9	-
11	151	34	U12	-
12	30	13	W10	-

GPIO	IPMI PIN	BANK	ZYNQ PIN	CLOCK INPUT?
55	64	34	R16	-
56	186	34	R17	-
57	187	34	R18	-
58	188	34	N17	-
59	189	34	P18	-
60	191	34	P15	-
61	192	34	P16	-
62	194	34	T19	-
63	195	34	R19	-
64	197	35	N15	-
65	198	35	N16	-
66	78	35	M14	-
67	200	35	M15	-

13	152	34	T15	-
14	31	13	W11	-
15	153	34	V12	-
16	32	13	Y11	-
17	154	34	W13	-
18	33	13	Y12	-
19	155	34	V13	-
20	35	34	R14	-
21	157	34	W18	-
22	36	34	W15	-
23	158	34	V16	-
24	37	34	T16	-
25	159	34	T17	-
26	38	34	U17	-
27	160	34	Y18	-
28	39	34	Y14	-
29	161	34	W16	-
30	40	34	W14	-
31	162	34	V17	-
32	41	34	U14	Limited
33	163	34	W19	-
34	42	34	Y16	-
35	164	34	Y19	-
36	43	34	V15	-
37	165	34	V18	-
38	44	34	Y17	-
39	166	34	W20	-
40	46	34	U15	Limited
41	168	13	W6	-
42	47	34	U18	Yes
43	169	13	V6	-
44	48	34	P19	Yes
45	49	34	N18	Yes
46	50	34	N20	Limited
47	51	34	U19	Yes
48	52	34	P20	Limited
49	53	34	V20	-
50	54	34	U20	-
51	55	34	T20	-
52	183	13	V10	-
53	184	13	V11	-
54	63	13	Y13	-

68	79	35	M17	-
69	201	35	M18	-
70	81	35	M19	-
71	203	35	M20	-
72	82	35	L14	-
73	204	35	L15	-
74	84	35	L16	Limited
75	206	35	L17	Limited
76	85	35	L20	-
77	207	35	L19	-
78	87	35	K14	-
79	209	35	J14	-
80	88	35	K17	Yes
81	210	35	K16	-
82	90	35	K18	Yes
83	212	35	G14	-
84	91	35	J19	-
85	213	35	K19	-
86	92	35	J16	-
87	214	35	J15	-
88	93	35	J20	-
89	215	35	H20	-
90	94	35	J18	-
91	216	35	H18	-
92	95	35	H17	Yes
93	217	35	H16	Yes
94	96	35	H15	-
95	218	35	G15	-
96	98	35	G17	-
97	220	35	G18	-
98	221	35	G19	-
99	224	35	G20	-
100	103	35	F16	-
101	225	35	F20	-
102	104	35	F17	-
103	226	35	E18	-
104	105	35	D18	-
105	227	35	E19	-
106	106	35	D19	-
107	228	35	F19	-
108	229	35	D20	-