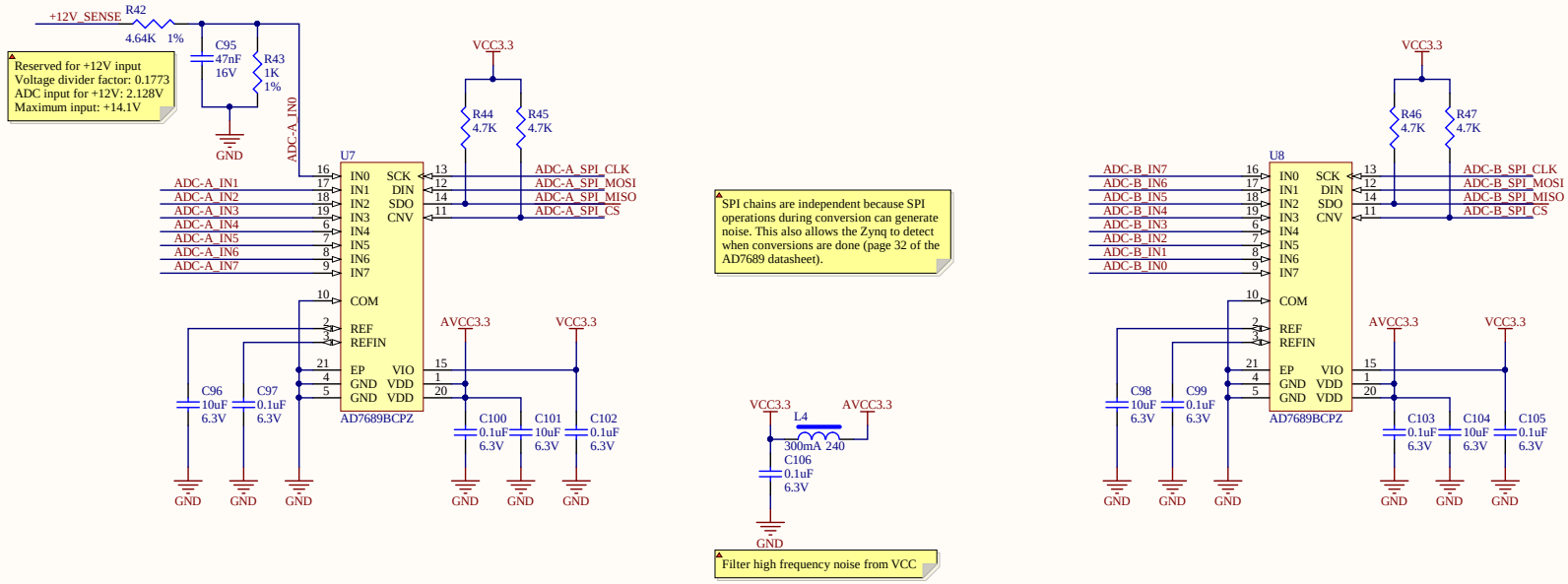
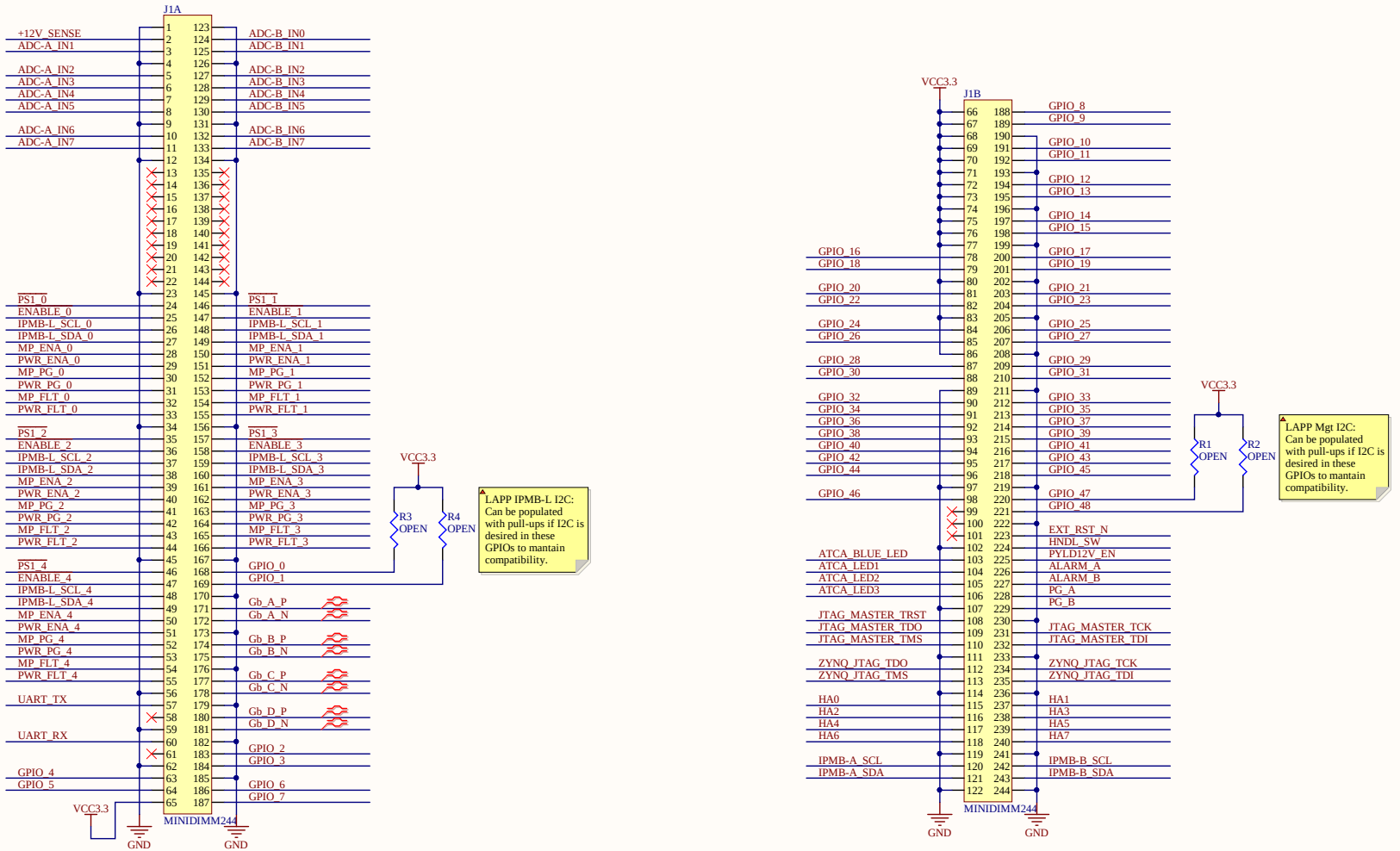
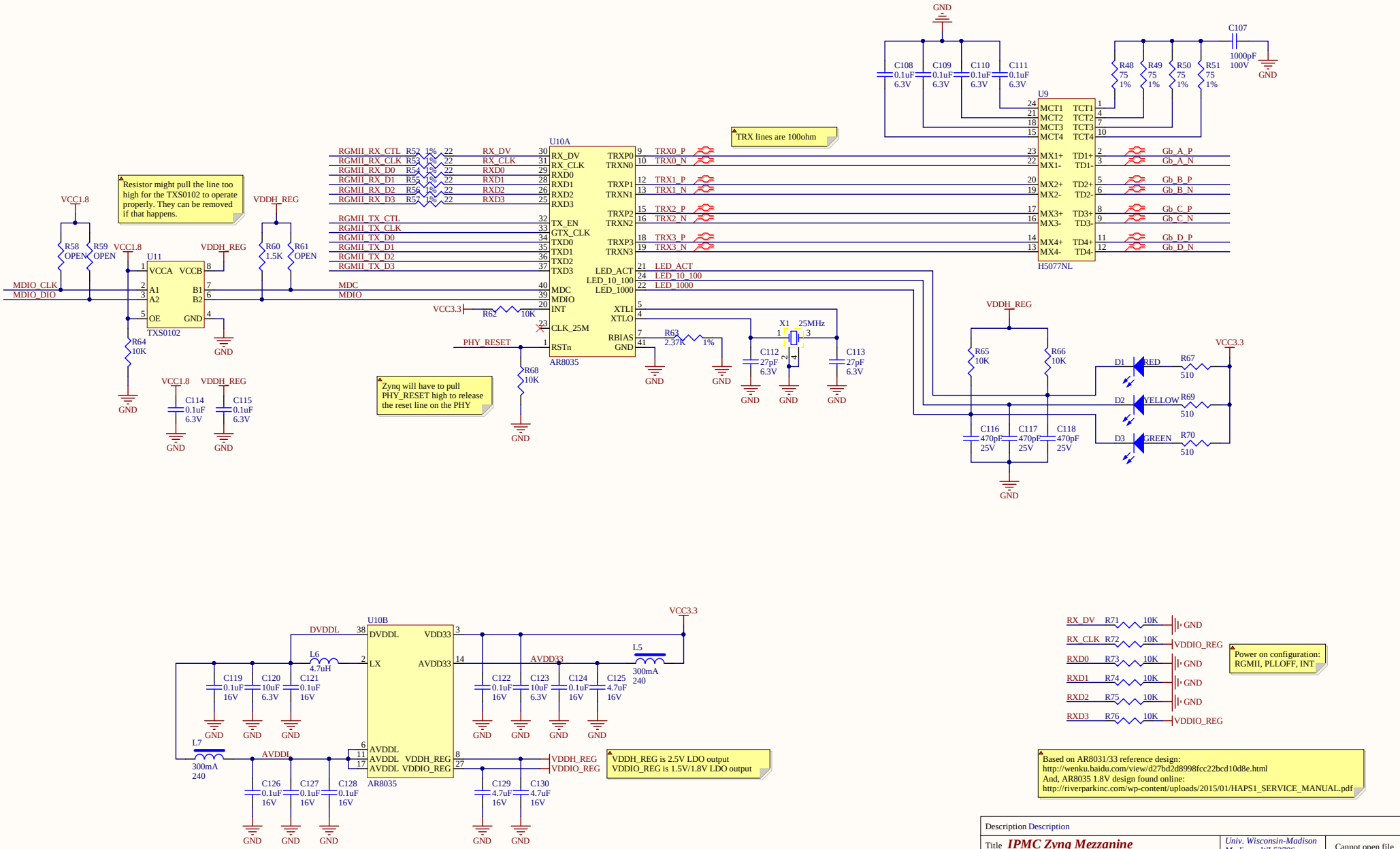
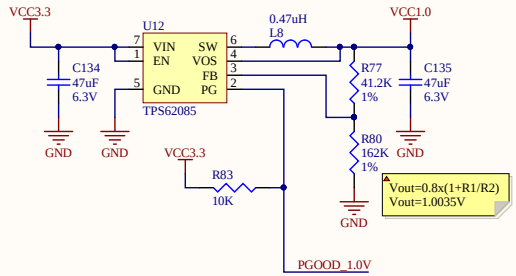


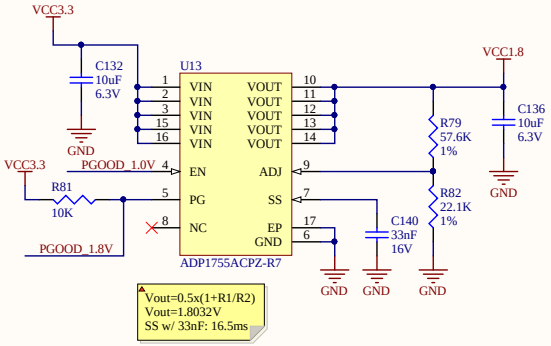
Description Description			
Title *IPMC Zynq Mezzanine*			*Univ. Wisconsin-Madison Madison, WI 53706*
Size: A3	Number:*	Revision:revA	Cannot open file \\cern.ch\dfs\Users\mpv\Desktop\Uw-ma
Date: 05/01/2017	Time: 16:05:28	Sheet * of *	
File: AnalogSense.SchDoc			Author: Vicente, M., Gorski., T., Tikalsky, J.

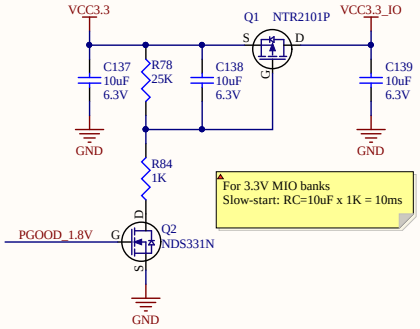


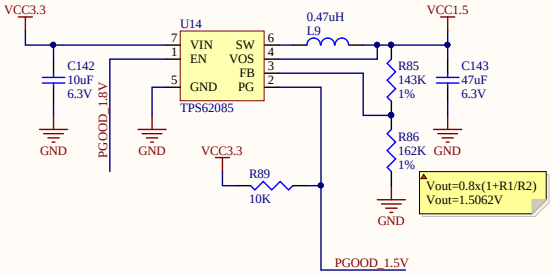
Description Description			
Title *IPMC Zynq Mezzanine*			*Univ. Wisconsin-Madison Madison, WI 53706*
Size: A3	Number:*	Revision:revA	Cannot open file \\cern.ch\dfs\Users\mpv\Desktop\Uw-ma
Date: 05/01/2017	Time: 16:05:28	Sheet * of *	
File: BoardConnector.SchDoc			Author: Vicente, M., Gorski., T., Tikalsky, J.

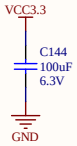

Resistor might pull the line too high for the TXS0102 to operate properly. They can be removed if that happens.
TRX lines are 100ohm
Zynq will have to pull PHY_RESET high to release the reset line on the PHY
VDDH_REG is 2.5V LDO output
VDDIO_REG is 1.5V/1.8V LDO output
Power on configuration: RGMII, PLLOFF, INT
Based on AR8031/33 reference design:
http://wenku.baidu.com/view/d27bd2d8998fcc22bcd10d8e.html
And, AR8035 1.8V design found online:
http://riverparkinc.com/wp-content/uploads/2015/01/HAPS1_SERVICE_MANUAL.pdf
U10A
AR8035
U10B
AR8035
U9
H5077NL
U11
TXS0102
X1 25MHz
VCC1.8
VDDH_REG
VCC3.3
GND
MDIO_CLK
MDIO_DIO
MDC
MDIO
PHY_RESET
RGMII_RX_CTL
RGMII_RX_CLK
RGMII_RX_D0
RGMII_RX_D1
RGMII_RX_D2
RGMII_RX_D3
RGMII_TX_CTL
RGMII_TX_CLK
RGMII_TX_D0
RGMII_TX_D1
RGMII_TX_D2
RGMII_TX_D3
RX_DV
RX_CLK
RXD0
RXD1
RXD2
RXD3
TX_EN
GTX_CLK
TXD0
TXD1
TXD2
TXD3
INT
CLK_25M
RSTn
LED_ACT
LED_10_100
LED_1000
XTLI
XTLO
RBIAS
TRXP0
TRXN0
TRXP1
TRXN1
TRXP2
TRXN2
TRXP3
TRXN3
TRX0_P
TRX0_N
TRX1_P
TRX1_N
TRX2_P
TRX2_N
TRX3_P
TRX3_N
Gb_A_P
Gb_A_N
Gb_B_P
Gb_B_N
Gb_C_P
Gb_C_N
Gb_D_P
Gb_D_N
DVDDL
AVDDL
AVDD33
VDD33
VDDH_REG
VDDIO_REG
RED
YELLOW
GREEN
Description Description
Title IPMC Zynq Mezzanine
Size: A3
Number:*
Revision:revA
Date: 05/01/2017
Time: 16:05:28
Sheet * of *
File: Ethernet.SchDoc
Univ. Wisconsin-Madison
Madison, WI 53706
Cannot open file \\cern.ch\dfs\Users\mmpv\Desktop\Uw-ma
Author: Vicente, M., Gorski., T., Tikalsky, J.

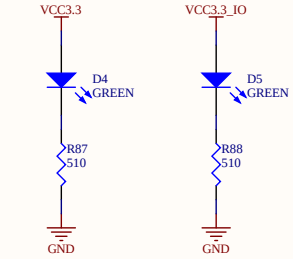




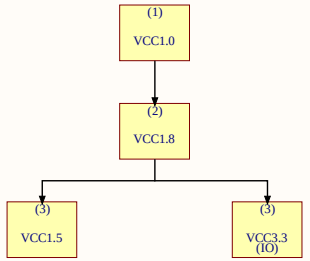








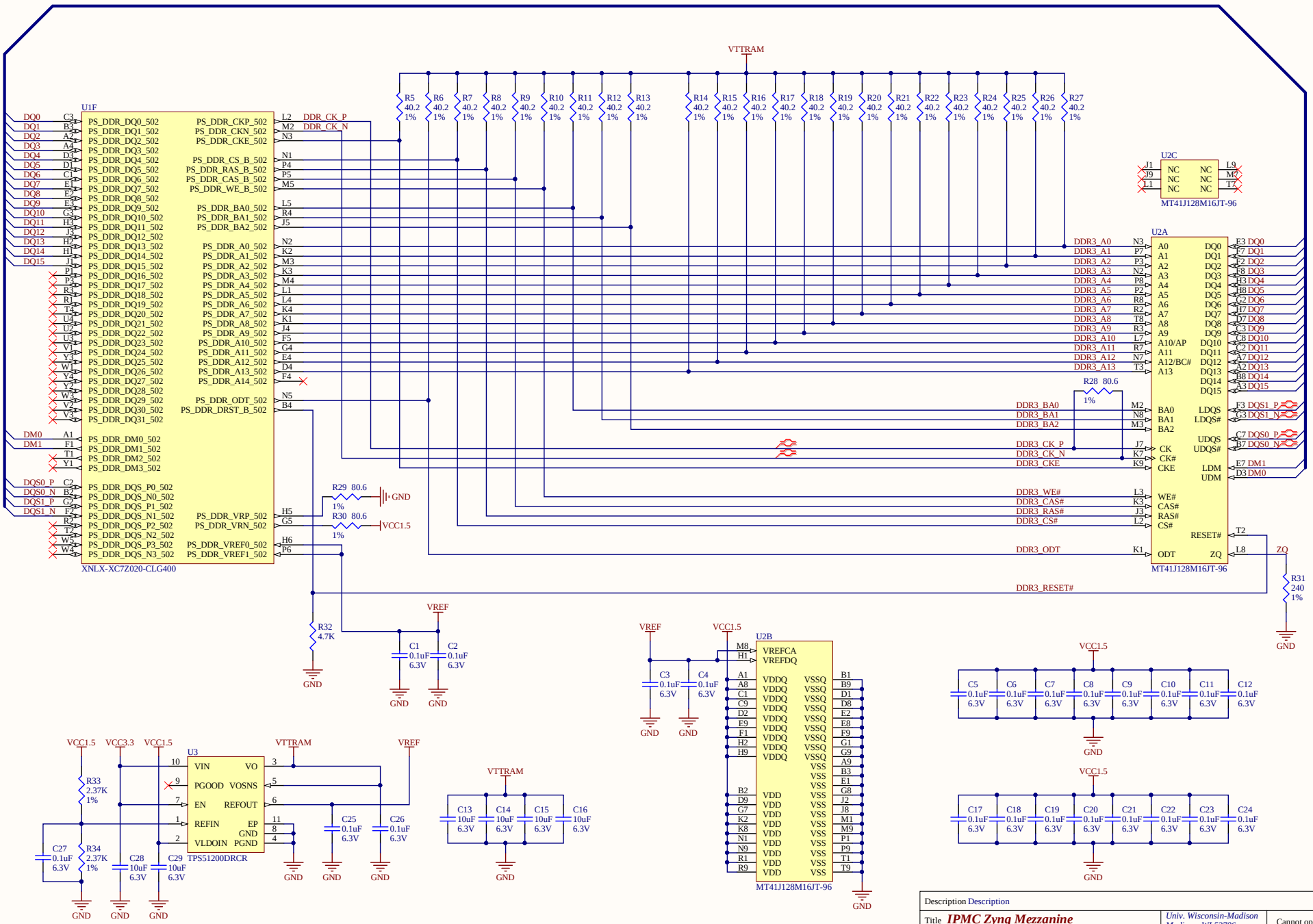
Power sequence for Zynq

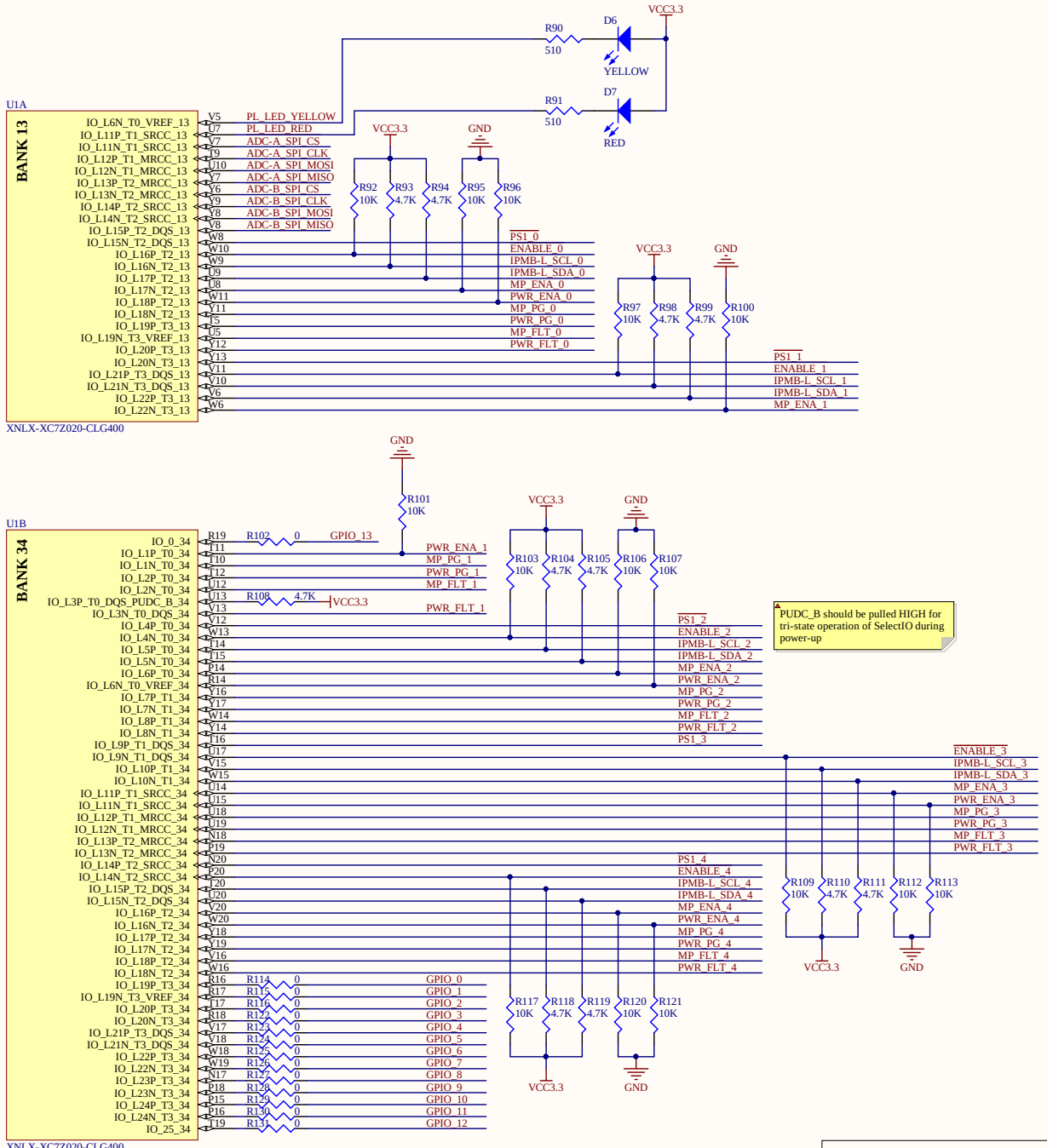


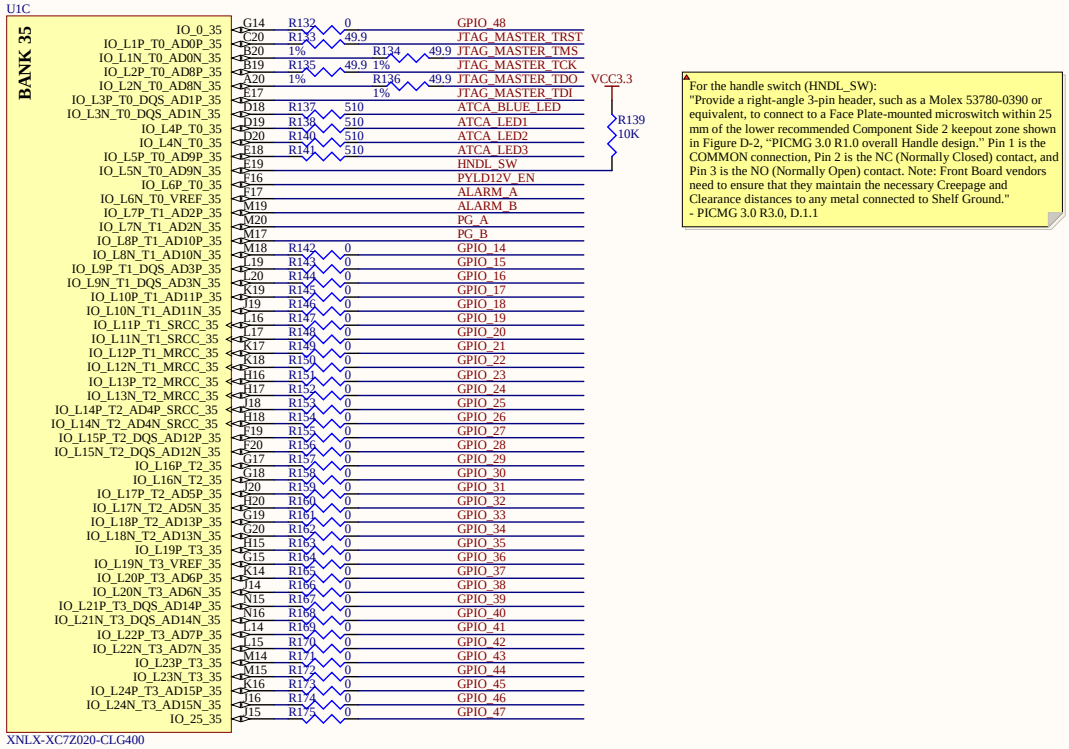
LDO converters are interchangable with the following components:
ADP1753 (0.8A) and ADP1741 (2.0A)

Potentially, a cheaper and small option is also available: LD39050 (0.5A, no soft-start) or LD39100 (1.0A, no soft-start)

Description Description			
Title *IPMC Zynq Mezzanine*			Univ. Wisconsin-Madison Madison, WI 53706
Size: A3	Number:*	Revision:revA	Cannot open file \\cern.ch\dfs\Users\mpv\Desktop\Uw-ma
Date: 05/01/2017	Time: 16:05:28	Sheet * of *	
File: PowerSequence.SchDoc			Author: Vicente, M., Gorski., T., Tikalsky, J.

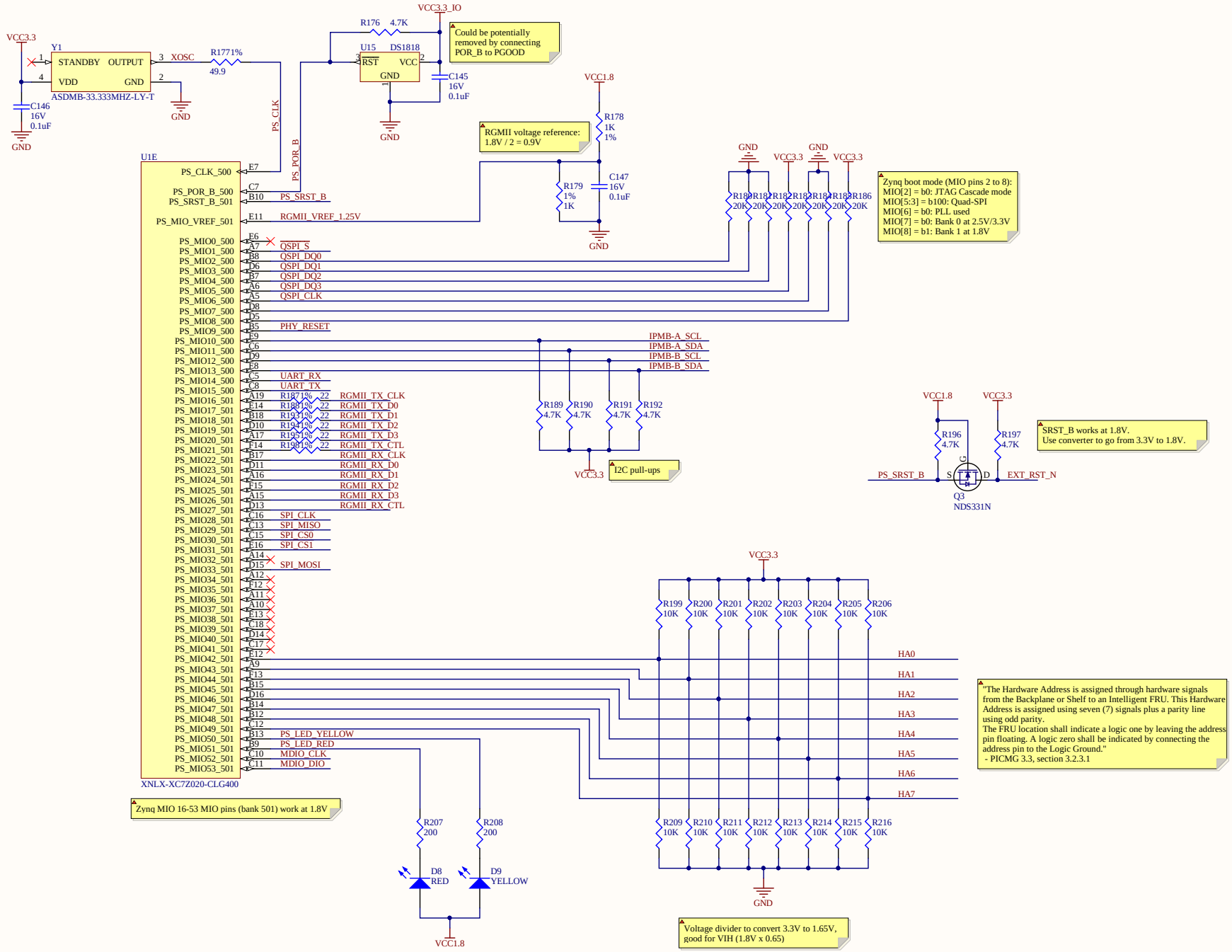

VTTRAM
U1F
XNLX-XC7Z020-CLG400
U2A
U2C
MT41J128M16JT-96
U2B
MT41J128M16JT-96
U3
TPS51200DRCR
VREF
VCC1.5
VCC3.3
GND
DDR_CK_P
DDR_CK_N
DDR3_RESET#
DDR3_ODT
R28 80.6 1%
R29 80.6 1%
R30 80.6 1%
R31 240 1%
R32 4.7K
R33 2.37K 1%
R34 2.37K 1%
Description Description
Title IPMC Zynq Mezzanine
Size: A3
Number:*
Revision: revA
Date: 05/01/2017
Time: 16:05:28
Sheet * of *
File: ZynqDDR.SchDoc
Univ. Wisconsin-Madison
Madison, WI 53706
Cannot open file \\cern.ch\dfs\Users\mpv\Desktop\Uw-ma
Author: Vicente, M., Gorski., T., Tikalsky, J.

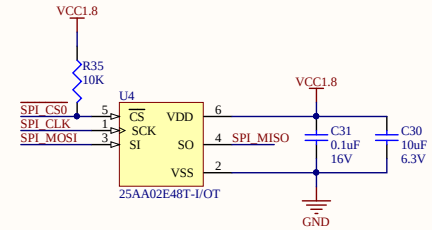

U1A
BANK 13
IO_L6N_T0_VREF_13
IO_L11P_T1_SRCC_13
IO_L11N_T1_SRCC_13
IO_L12P_T1_MRCC_13
IO_L12N_T1_MRCC_13
IO_L13P_T2_MRCC_13
IO_L13N_T2_MRCC_13
IO_L14P_T2_SRCC_13
IO_L14N_T2_SRCC_13
IO_L15P_T2_DQS_13
IO_L15N_T2_DQS_13
IO_L16P_T2_13
IO_L16N_T2_13
IO_L17P_T2_13
IO_L17N_T2_13
IO_L18P_T2_13
IO_L18N_T2_13
IO_L19P_T3_13
IO_L19N_T3_VREF_13
IO_L20P_T3_13
IO_L20N_T3_13
IO_L21P_T3_DQS_13
IO_L21N_T3_DQS_13
IO_L22P_T3_13
IO_L22N_T3_13
V5 PL_LED_YELLOW
U7 PL_LED_RED
V7 ADC-A_SPI_CS
T9 ADC-A_SPI_CLK
U10 ADC-A_SPI_MOSI
Y7 ADC-A_SPI_MISO
Y6 ADC-B_SPI_CS
Y9 ADC-B_SPI_CLK
Y8 ADC-B_SPI_MOSI
V8 ADC-B_SPI_MISO
W8
W10 PS1_0
W9 ENABLE_0
U9 IPMB-L_SCL_0
U8 IPMB-L_SDA_0
W11 MP_ENA_0
Y11 PWR_ENA_0
T5 MP_PG_0
U5 PWR_PG_0
Y12 MP_FLT_0
V13 PWR_FLT_0
V11 PS1_1
V10 ENABLE_1
V6 IPMB-L_SCL_1
W6 IPMB-L_SDA_1
MP_ENA_1
XNLX-XC7Z020-CLG400
R90 510
D6
YELLOW
VCC3.3
R91 510
D7
RED
R92 10K
R93 4.7K
R94 4.7K
R95 10K
R96 10K
GND
R97 10K
R98 4.7K
R99 4.7K
R100 10K
U1B
BANK 34
IO_0_34
IO_L1P_T0_34
IO_L1N_T0_34
IO_L2P_T0_34
IO_L2N_T0_34
IO_L3P_T0_DQS_PUDC_B_34
IO_L3N_T0_DQS_34
IO_L4P_T0_34
IO_L4N_T0_34
IO_L5P_T0_34
IO_L5N_T0_34
IO_L6P_T0_34
IO_L6N_T0_VREF_34
IO_L7P_T1_34
IO_L7N_T1_34
IO_L8P_T1_34
IO_L8N_T1_34
IO_L9P_T1_DQS_34
IO_L9N_T1_DQS_34
IO_L10P_T1_34
IO_L10N_T1_34
IO_L11P_T1_SRCC_34
IO_L11N_T1_SRCC_34
IO_L12P_T1_MRCC_34
IO_L12N_T1_MRCC_34
IO_L13P_T2_MRCC_34
IO_L13N_T2_MRCC_34
IO_L14P_T2_SRCC_34
IO_L14N_T2_SRCC_34
IO_L15P_T2_DQS_34
IO_L15N_T2_DQS_34
IO_L16P_T2_34
IO_L16N_T2_34
IO_L17P_T2_34
IO_L17N_T2_34
IO_L18P_T2_34
IO_L18N_T2_34
IO_L19P_T3_34
IO_L19N_T3_VREF_34
IO_L20P_T3_34
IO_L20N_T3_34
IO_L21P_T3_DQS_34
IO_L21N_T3_DQS_34
IO_L22P_T3_34
IO_L22N_T3_34
IO_L23P_T3_34
IO_L23N_T3_34
IO_L24P_T3_34
IO_L24N_T3_34
IO_25_34
R19 R102 0 GPIO_13
T11 PWR_ENA_1
T10 MP_PG_1
T12 PWR_PG_1
U12 MP_FLT_1
U13 R108 4.7K VCC3.3
V13 PWR_FLT_1
V12 PS1_2
W13 ENABLE_2
T14 IPMB-L_SCL_2
T15 IPMB-L_SDA_2
P14 MP_ENA_2
R14 PWR_ENA_2
Y16 MP_PG_2
Y17 PWR_PG_2
W14 MP_FLT_2
Y14 PWR_FLT_2
PS1_3
U17 ENABLE_3
V15 IPMB-L_SCL_3
W15 IPMB-L_SDA_3
U14 MP_ENA_3
U15 PWR_ENA_3
U18 MP_PG_3
U19 PWR_PG_3
N18 MP_FLT_3
P19 PWR_FLT_3
V20 PS1_4
P20 ENABLE_4
T20 IPMB-L_SCL_4
U20 IPMB-L_SDA_4
V20 MP_ENA_4
W20 PWR_ENA_4
Y18 MP_PG_4
Y19 PWR_PG_4
V16 MP_FLT_4
W16 PWR_FLT_4
R16 R114 0 GPIO_0
R17 R115 0 GPIO_1
T17 R116 0 GPIO_2
R18 R122 0 GPIO_3
V17 R123 0 GPIO_4
T18 R124 0 GPIO_5
W18 R125 0 GPIO_6
W19 R126 0 GPIO_7
N17 R127 0 GPIO_8
P18 R128 0 GPIO_9
P15 R129 0 GPIO_10
P16 R130 0 GPIO_11
T19 R131 0 GPIO_12
XNLX-XC7Z020-CLG400
R101 10K
R103 10K
R104 4.7K
R105 4.7K
R106 10K
R107 10K
R109 10K
R110 4.7K
R111 4.7K
R112 10K
R113 10K
R117 10K
R118 4.7K
R119 4.7K
R120 10K
R121 10K
PUDC_B should be pulled HIGH for tri-state operation of SelectIO during power-up
Description Description
Title IPMC Zynq Mezzanine
Size: A3
Number:*
Revision:revA
Date: 05/01/2017
Time: 16:05:29
Sheet * of *
File: ZynqEMIO.SchDoc
Univ. Wisconsin-Madison
Madison, WI 53706
Cannot open file \\cern.ch\dfs\Users\mpv\Desktop\Uw-ma
Author: Vicente, M., Gorski., T., Tikalsky, J.



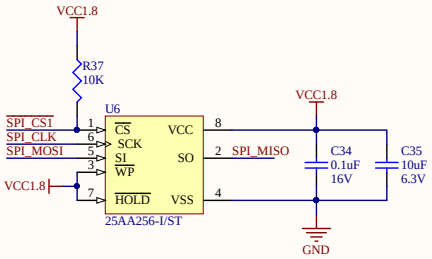
For the handle switch (HNDL_SW):
"Provide a right-angle 3-pin header, such as a Molex 53780-0390 or equivalent, to connect to a Face Plate-mounted microswitch within 25 mm of the lower recommended Component Side 2 keepout zone shown in Figure D-2, "PICMG 3.0 R1.0 overall Handle design." Pin 1 is the COMMON connection, Pin 2 is the NC (Normally Closed) contact, and Pin 3 is the NO (Normally Open) contact. Note: Front Board vendors need to ensure that they maintain the necessary Creepage and Clearance distances to any metal connected to Shelf Ground."
- PICMG 3.0 R3.0, D.1.1

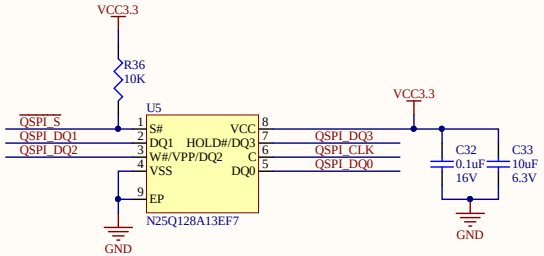
Description Description			
Title *IPMC Zynq Mezzanine*			Univ. Wisconsin-Madison Madison, WI 53706
Size: A3	Number:*	Revision:revA	Cannot open file \\cern.ch\dfs\Users\mpv\Desktop\Uw-ma
Date: 05/01/2017 Time: 16:05:29		Sheet * of *	
File: ZynqEMIO_2.SchDoc			Author: Vicente, M., Gorski., T., Tikalsky, J.


VCC3.3
Y1
STANDBY
OUTPUT
VDD
GND
ASDMB-33.333MHZ-LY-T
C146
16V
0.1uF
XOSC
R1771%
49.9
PS_CLK
VCC3.3_IO
R176 4.7K
U15 DS1818
RST
VCC
C145
16V
0.1uF
Could be potentially removed by connecting POR_B to PGOOD
VCC1.8
R178
1K
1%
RGMII voltage reference:
1.8V / 2 = 0.9V
R179
1%
1K
C147
16V
0.1uF
U1E
PS_CLK_500
PS_POR_B_500
PS_SRST_B_501
PS_MIO_VREF_501
RGMII_VREF_1.25V
PS_SRST_B
PS_POR_B
R180 R181 R182 R183 R184 R185 R186
20K
Zynq boot mode (MIO pins 2 to 8):
MIO[2] = b0: JTAG Cascade mode
MIO[5:3] = b100: Quad-SPI
MIO[6] = b0: PLL used
MIO[7] = b0: Bank 0 at 2.5V/3.3V
MIO[8] = b1: Bank 1 at 1.8V
QSPI_S
QSPI_DQ0
QSPI_DQ1
QSPI_DQ2
QSPI_DQ3
QSPI_CLK
PHY_RESET
IPMB-A_SCL
IPMB-A_SDA
IPMB-B_SCL
IPMB-B_SDA
R189 R190 R191 R192
4.7K
I2C pull-ups
UART_RX
UART_TX
RGMII_TX_CLK
RGMII_TX_D0
RGMII_TX_D1
RGMII_TX_D2
RGMII_TX_D3
RGMII_TX_CTL
RGMII_RX_CLK
RGMII_RX_D0
RGMII_RX_D1
RGMII_RX_D2
RGMII_RX_D3
RGMII_RX_CTL
SPI_CLK
SPI_MISO
SPI_CS0
SPI_CS1
SPI_MOSI
PS_LED_YELLOW
PS_LED_RED
MDIO_CLK
MDIO_DIO
XNLX-XC7Z020-CLG400
Zynq MIO 16-53 MIO pins (bank 501) work at 1.8V
R196 R197
4.7K
SRST_B works at 1.8V.
Use converter to go from 3.3V to 1.8V.
PS_SRST_B
EXT_RST_N
Q3
NDS331N
R199 R200 R201 R202 R203 R204 R205 R206
10K
HA0
HA1
HA2
HA3
HA4
HA5
HA6
HA7
"The Hardware Address is assigned through hardware signals from the Backplane or Shelf to an Intelligent FRU. This Hardware Address is assigned using seven (7) signals plus a parity line using odd parity.
The FRU location shall indicate a logic one by leaving the address pin floating. A logic zero shall be indicated by connecting the address pin to the Logic Ground."
- PICMG 3.3, section 3.2.3.1
R209 R210 R211 R212 R213 R214 R215 R216
10K
R207 R208
200
D8
RED
D9
YELLOW
Voltage divider to convert 3.3V to 1.65V, good for VIH (1.8V x 0.65)
Description Description
Title IPMC Zynq Mezzanine
Size: A3
Number:*
Revision:revA
Date: 05/01/2017
Time: 16:05:29
Sheet * of *
File: ZynqMIO.SchDoc
Univ. Wisconsin-Madison
Madison, WI 53706
Author: Vicente, M., Gorski., T., Tikalsky, J.
Cannot open file
\\cern.ch\dfs\Users\m
mpv\Desktop\Uw-ma



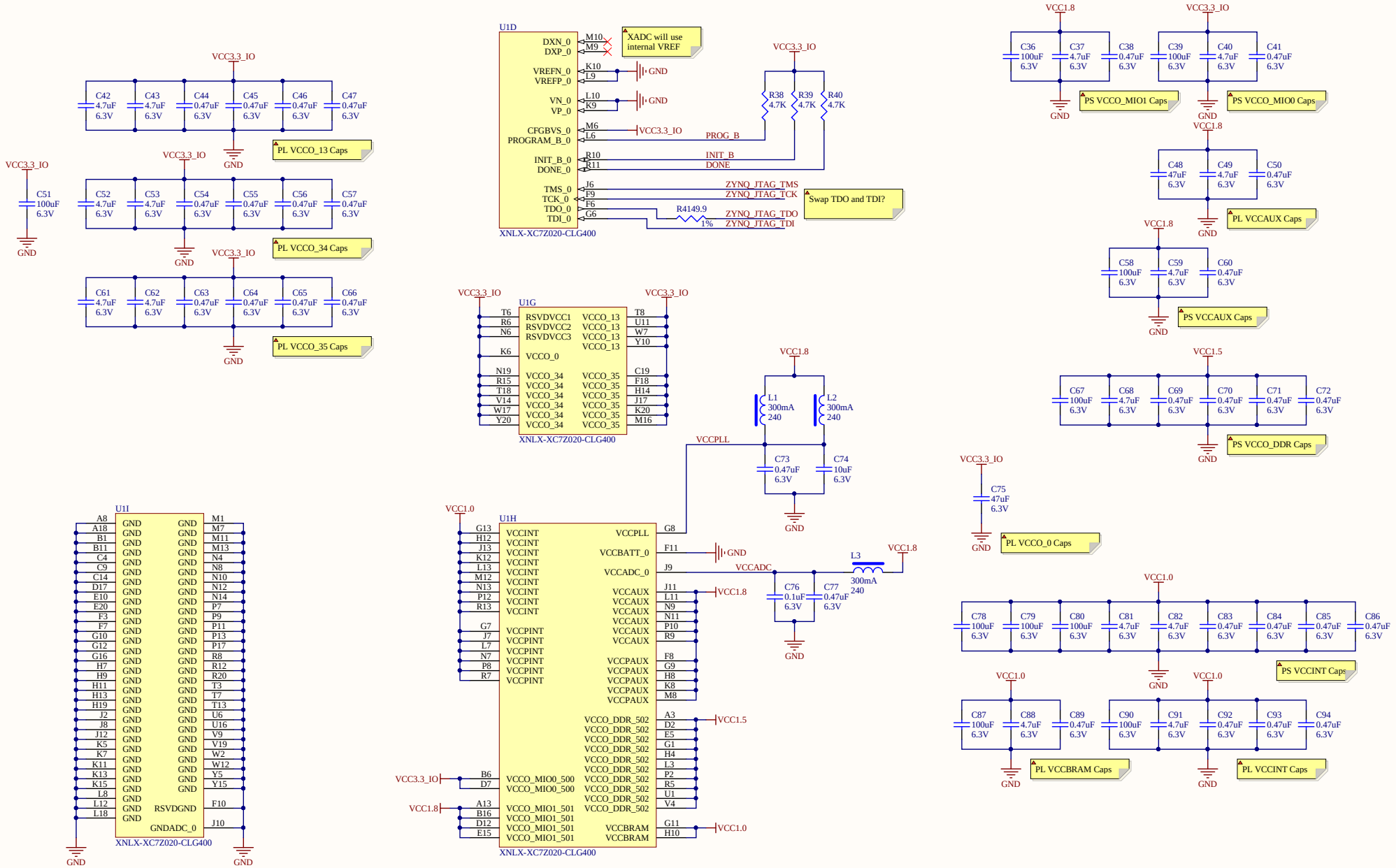
CS pins can be swapped if it improves layout





QSPI has 16MBytes
Needs 50ohm lines
C should be pulled LOW, but there is already the Zynq strap-pins

Description Description			
Title *IPMC Zynq Mezzanine*			*Univ. Wisconsin-Madison Madison, WI 53706*
Size: A3	Number:*	Revision:revA	Cannot open file \\cern.ch\dfs\Users\mpv\Desktop\Uw-ma
Date: 05/01/2017	Time: 16:05:29	Sheet * of *	
File: ZynqPeripherals.SchDoc			Author: Vicente, M., Gorski., T., Tikalsky, J.


VCC3.3_IO
C42 4.7uF 6.3V
C43 4.7uF 6.3V
C44 0.47uF 6.3V
C45 0.47uF 6.3V
C46 0.47uF 6.3V
C47 0.47uF 6.3V
GND
PL VCCO_13 Caps
C51 100uF 6.3V
C52 4.7uF 6.3V
C53 4.7uF 6.3V
C54 0.47uF 6.3V
C55 0.47uF 6.3V
C56 0.47uF 6.3V
C57 0.47uF 6.3V
PL VCCO_34 Caps
C61 4.7uF 6.3V
C62 4.7uF 6.3V
C63 0.47uF 6.3V
C64 0.47uF 6.3V
C65 0.47uF 6.3V
C66 0.47uF 6.3V
PL VCCO_35 Caps
U1D
DXN_0
DXP_0
VREFN_0
VREFP_0
VN_0
VP_0
CFGBVS_0
PROGRAM_B_0
INIT_B_0
DONE_0
TMS_0
TCK_0
TDO_0
TDI_0
XADC will use internal VREF
R38 4.7K
R39 4.7K
R40 4.7K
PROG_B
INIT_B
DONE
ZYNQ_JTAG_TMS
ZYNQ_JTAG_TCK
ZYNQ_JTAG_TDO
ZYNQ_JTAG_TDI
R4149.9 1%
Swap TDO and TDI?
XNLX-XC7Z020-CLG400
U1G
RSVDVCC1
RSVDVCC2
RSVDVCC3
VCCO_0
VCCO_34
VCCO_35
VCCO_13
U1I
GND
RSVDGND
GNDADC_0
U1H
VCCINT
VCCPINT
VCCPLL
VCCBATT_0
VCCADC_0
VCCAUX
VCCPAUX
VCCO_DDR_502
VCCO_MIO0_500
VCCO_MIO1_501
VCCBRAM
L1 300mA 240
L2 300mA 240
L3 300mA 240
C73 0.47uF 6.3V
C74 10uF 6.3V
C75 47uF 6.3V
C76 0.1uF 6.3V
C77 0.47uF 6.3V
PL VCCO_0 Caps
C36 100uF 6.3V
C37 4.7uF 6.3V
C38 0.47uF 6.3V
C39 100uF 6.3V
C40 4.7uF 6.3V
C41 0.47uF 6.3V
PS VCCO_MIO1 Caps
PS VCCO_MIO0 Caps
C48 47uF 6.3V
C49 4.7uF 6.3V
C50 0.47uF 6.3V
PL VCCAUX Caps
C58 100uF 6.3V
C59 4.7uF 6.3V
C60 0.47uF 6.3V
PS VCCAUX Caps
C67 100uF 6.3V
C68 4.7uF 6.3V
C69 0.47uF 6.3V
C70 0.47uF 6.3V
C71 0.47uF 6.3V
C72 0.47uF 6.3V
PS VCCO_DDR Caps
C78 100uF 6.3V
C79 100uF 6.3V
C80 100uF 6.3V
C81 4.7uF 6.3V
C82 4.7uF 6.3V
C83 0.47uF 6.3V
C84 0.47uF 6.3V
C85 0.47uF 6.3V
C86 0.47uF 6.3V
PS VCCINT Caps
C87 100uF 6.3V
C88 4.7uF 6.3V
C89 0.47uF 6.3V
C90 100uF 6.3V
C91 4.7uF 6.3V
C92 0.47uF 6.3V
C93 0.47uF 6.3V
C94 0.47uF 6.3V
PL VCCBRAM Caps
PL VCCINT Caps
Description Description
Title IPMC Zynq Mezzanine
Univ. Wisconsin-Madison
Madison, WI 53706
Size: A3
Number:*
Revision:revA
Date: 05/01/2017
Time: 16:05:29
Sheet * of *
File: ZynqPower.SchDoc
Author: Vicente, M., Gorski., T., Tikalsky, J.
Cannot open file \\cern.ch\dfs\Users\mpv\Desktop\Uw-ma

Comment	Description	Designator	Footprint	LibRef	Qua ntity	Rat ed Cur rent	Rati ng	Tole ranc e	Valu e
?	Capacitor	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27	C0201_IPC_H	Cap	23		6.3V		0.1u F
?	Capacitor	C13, C14, C15, C16, C28, C29, C30, C33, C35, C74, C96, C98, C101, C104, C120, C123, C132, C136, C137, C138, C139, C142	C0402_IPC_H	Cap	22		6.3V		10u F
	Capacitor	C31, C32, C34, C119, C121, C122, C134, C135, C127, C129, C145, C146, C147	C0402	Cap	13		16V		0.1u F
Murata GRM32ER61C107ME20L	Capacitor	C36, C39, C58, C67, C78, C79, C80, C87, C90	C1210_IPC_H	Cap	9		6.3V		100 uF
?	Capacitor	C37, C40, C43, C53, C61, C62	C0402_IPC_H	Cap	6		6.3V		4.7u F
Murata GRM155R60J474KE19D	Capacitor	C38, C41, C50, C60, C65, C66, C69, C70, C71, C72, C73, C77, C83, C84, C85, C86, C89, C92, C93, C94	C0402_IPC_H	Cap	20		6.3V		0.47 uF
Murata GRM155R60J474KE19D	Capacitor	C42, C49, C52, C59, C68, C82, C88, C91	C0402_IPC_H	Cap	8		6.3V		4.7u F
?	Capacitor	C44, C45, C46, C47, C54, C55, C56, C57, C63, C64	C0402_IPC_H	Cap	10		6.3V		0.47 uF
Murata GRM155R60J474KE19D	Capacitor	C48	C0805_M	Cap	1		6.3V		47u F
?	Capacitor	C51, C144	C1210_IPC_H	Cap	2		6.3V		100 uF
?	Capacitor	C75, C134, C135, C143	C0805_M	Cap	4		6.3V		47u F
?	Capacitor	C76, C97, C99, C100, C102, C103, C105, C106, C108, C109, C110, C111, C114, C115	C0201	Cap	14		6.3V		0.1u F
	Capacitor	C81	C0402_IPC_H	Cap	1		6.3V		4.7u F
?	Capacitor	C95	C0402	Cap	1		16V		47n F
?	Capacitor	C107	C0402	Cap	1		100 V		100 0pF
?	Capacitor	C112, C113	C0201	Cap	2		6.3V		270 pF
?	Capacitor	C116, C117, C118	C0201	Cap	3		25V		470 pF
?	Capacitor	C125, C129, C130	C0402	Cap	3		16V		4.7u F
?	Capacitor	C140	C0402	Cap	1		16V		33n F
?	Light Emitting Diode	D1, D7, D8	LED0603_M	LED	3				RED
?	Light Emitting Diode	D2, D6, D9	LED0603_M	LED	3				YELLOW
?	Light Emitting Diode	D3, D4, D5	LED0603_M	LED	3				GREEN
MINIDIMM-244	244-pin miniDIMM pads	J1	miniDIMM244	MINIDIMM244	1				
9K1005HM241-T	Bead Inductor	L3, L2, L3, L4, L5, L7	L0402_H	Bead	6	300 mA			240
Wurth 74438323047	Inductor	L6	L2520_H	ind	1			20%	4.7u H
DR252012-R47M-HF	Inductor	L8, L9	L2520_H	ind	2			20%	0.47 uH
NTR2101P	Small Signal MOSFET, −8.0V, −3.7 A, Single P−Channel,	Q1	SOT23-H	NTR2101P	1				
NDS331N	N-Channel Logic Level Enhancement Mode Field Effect Transistor	Q2, Q3	SSOT-3_H	NDS331N	2				
?	Resistor	R1, R2, R3, R4, R58, R59, R61	R0402_IPC_H	Res	7			5%	OPEN
?	Resistor	R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27	R0201_IPC_H	Res	23			1%	40.2
?	Resistor	R28, R29, R30	R0402_IPC_H	Res	3			1%	80.6
?	Resistor	R31	R0402_IPC_H	Res	1			1%	240
?	Resistor	R32, R38, R39, R40, R44, R45, R46, R47, R93, R94, R98, R99, R104, R105, R108, R110, R111, R118, R119, R176, R189, R190, R191, R192, R196, R197	R0402_IPC_H	Res	26			5%	4.7k
?	Resistor	R33, R34, R62	R0402_IPC_H	Res	3			1%	2.37 k
Yageo AC0201JR-071DKL	Resistor	R35, R36, R37, R62, R64, R65, R66, R68, R71, R72, R73, R74, R75, R76, R81, R83, R89, R139, R199, R200, R201, R202, R203, R204, R205, R206, R209, R210, R211, R212, R213, R214, R215, R216	R0201	Res	34			5%	10K
?	Resistor	R41	R0201	Res	1			1%	49.9
?	Resistor	R42	R0603	Res	1			1%	4.64 k
?	Resistor	R43, R178, R179	R0603	Res	3			1%	1K
?	Resistor	R48, R49, R50, R51	R0402_IPC_H	Res	4			1%	75
?	Resistor	R52, R53, R54, R55, R56, R57, R187, R188, R193, R194, R195, R198	R0201	Res	12			1%	22
?	Resistor	R60	R0402_IPC_H	Res	1			5%	1.5K
?	Resistor	R67, R69, R70, R87, R88, R90, R91, R137, R138, R140, R141	R0402_IPC_H	Res	11			5%	510
?	Resistor	R77	R0603	Res	1			1%	41.2 k
?	Resistor	R78	R0402_IPC_H	Res	1			5%	255
?	Resistor	R79	R0603	Res	1			1%	57.6 k
?	Resistor	R80, R86	R0603	Res	2			1%	100 k
?	Resistor	R82	R0603	Res	1			1%	221 k
?	Resistor	R84	R0402_IPC_H	Res	1			5%	1K
?	Resistor	R85	R0603	Res	1			1%	140 k
?	Resistor	R92, R95, R96, R97, R100, R101, R103, R106, R107, R109, R112, R113, R117, R120, R121	R0402_IPC_H	Res	15			5%	10K
?	Resistor	R102, R114, R115, R116, R122, R123, R124, R125, R126, R127, R128, R129, R130, R131, R132, R142, R143, R144, R145, R146, R147, R148, R149, R150, R151, R152, R153, R154, R155, R156, R157, R158, R159, R160, R161, R162, R163, R164, R165, R166, R167, R168, R169, R170, R171, R172, R173, R174, R175	R0402_IPC_H	Res	49			5%	0
?	Resistor	R133, R134, R135, R136, R177	R0402_IPC_H	Res	5			1%	49.9
?	Resistor	R180, R181, R182, R183, R184, R185, R186	R0201	Res	7			5%	20K
?	Resistor	R207, R208	R0402_IPC_H	Res	2			5%	200
XNLX-XC7Z020-CLG400		U1	CLG400	XILX-XC7Z020-CLG400	1				
MT41J128M16JT-96		U2	MICT-JT-96	MT41J128M16JT-96	1				
TPS51200DRCR	Single Output LDO, 3 A, 2.375 to 3.5 V Input, with DDR Termination, 10-pin SON (DRC), -40 to 85 degC, Green (RoHS & no Sb/Br)	U3	DRC0010J_V	CMP-9395-000664-2	1		Cat alo g		
25AA02E48T-I/OT	2K SPI Bus Serial EEPROM with EUI-48 Node Identity, 6-Pin SOT-23, Industrial Temperature, Tape and Reel	U4	SOT-23-OT6_L	CMP-0165-00270-0	1				
N25Q128A13E7	128Mb, Multiple I/O Serial Flash Memory	U5	V-PDFN-8_H	N25Q128A13E7	1				
25AA256-I/ST	256K SPI Bus Serial EEPROM, 8-Pin TSSOP, Industrial Temperature	U6	TSSOP-ST8_L	CMP-0165-00405-0	1				
AD7689BCPZ	Octal 16-Bit PulSAR Analog-to-Digital Converter with Serial, SPI Interface, 250KSPS, -40 to +85 degC, CP-20-4, Pb-Free, Tube	U7, U8	CP-20-4_N	CMP-0313-00576-2	2				
H5077NL	1000Base-T, Single Port Mini-Magnetics Modules	U9	H5077NL	H5077NL	1				
AR8035	Integrated 10/100/1000 Gigabit Ethernet Transceiver	U10	QFN40_H	AR8035	1				
TXS0102	2-Bit Bidirectional Voltage-Level Translator for Open-Drain and Push-Pull Applications	U11	X2SON-8_H	TXS0102	1				
TPS62085	3-A Step-Down Converter With Hiccup Short-Circuit Protection	U12, U14	VSON-8_L	TPS62085	2				
ADP1755ACP-R7	1.2 A, Low VIN, Low Dropout Linear Regulator, 1.6 to 3.6 V Vin, 0.75 to 3 V Vout, Industrial, 16-pin QFN (CP-16-4), Reel	U13	CP-16-4_L	CMP-0786-00436-1	1				
DS1818	3.3V Econo/Reset with Pushbutton	U15	SOT23-H	DS1818	1				
XRCGB25M000F3M00R0	Standard Crystal Oscillator	X1	XRCGB_F	Crystal Osc	1				25 MHz
ASDMB-33	Plastic Package Clock Oscillator	X1	ABRA-ASDMB-4 V	CMP-07	1				