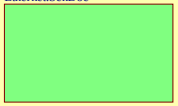
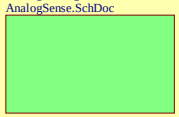
ZYNQ-IPMC MEZZANINE (revB)

Connectivity
(PHY, ADC, Mezzanine IO)

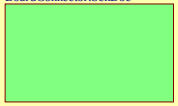
Ethernet PHY
Ethernet.SchDoc



Analog-to-Digital Converters
AnalogSense.SchDoc



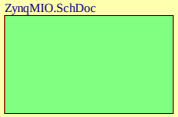
Mezzanine Connector
BoardConnector.SchDoc



ZYNQ-7020/14S

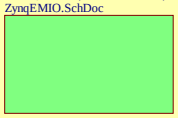
PS:

ZYNQ MIO
ZynqMIO.SchDoc

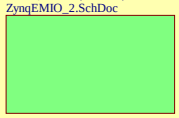


PL:

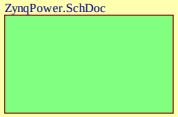
ZYNQ EMIO (banks 13 and 34)
ZynqEMIO.SchDoc



ZYNQ EMIO (bank 35)
ZynqEMIO_2.SchDoc

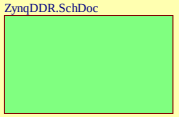


ZYNQ Power
ZynqPower.SchDoc

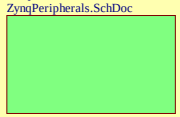


Memory
(DDR3, QSPI, EEPROM)

DDR3
ZynqDDR.SchDoc

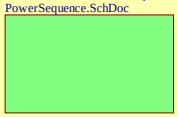


Peripherals
ZynqPeripherals.SchDoc

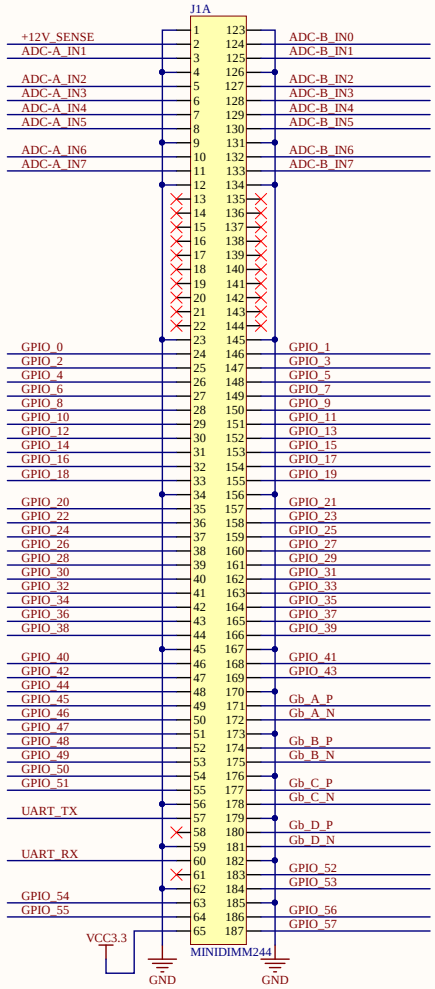


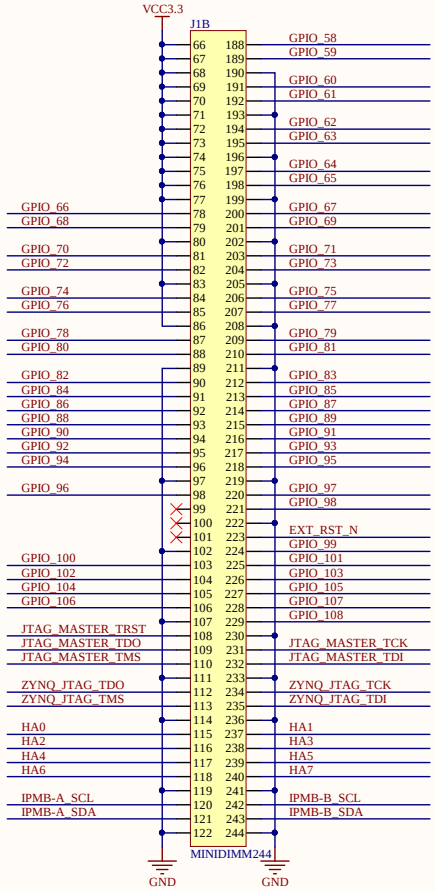
Power

DC/DC Converters and Sequencing
PowerSequence.SchDoc

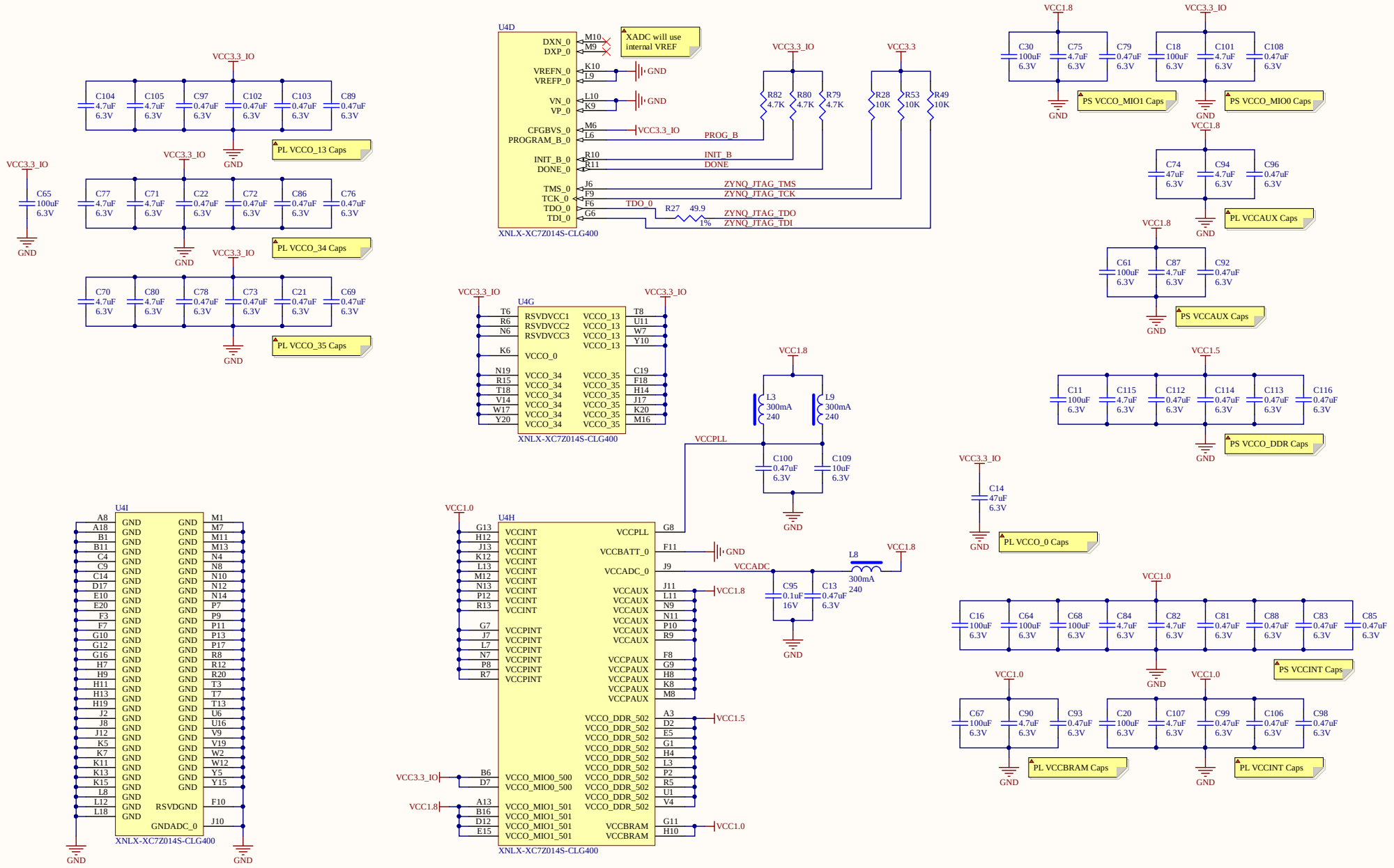


Description	**Project overview**		
Title	***ZYNQ-IPMC***		*Univ. Wisconsin-Madison Madison, WI 53706*
Size: A3	Number: 1	Revision: revB1	
Date: 6/20/2019	Time: 3:03:47 PM	Sheet 1 of 11	
File: IPMC.SchDoc			Author: *Marcelo Vicente*



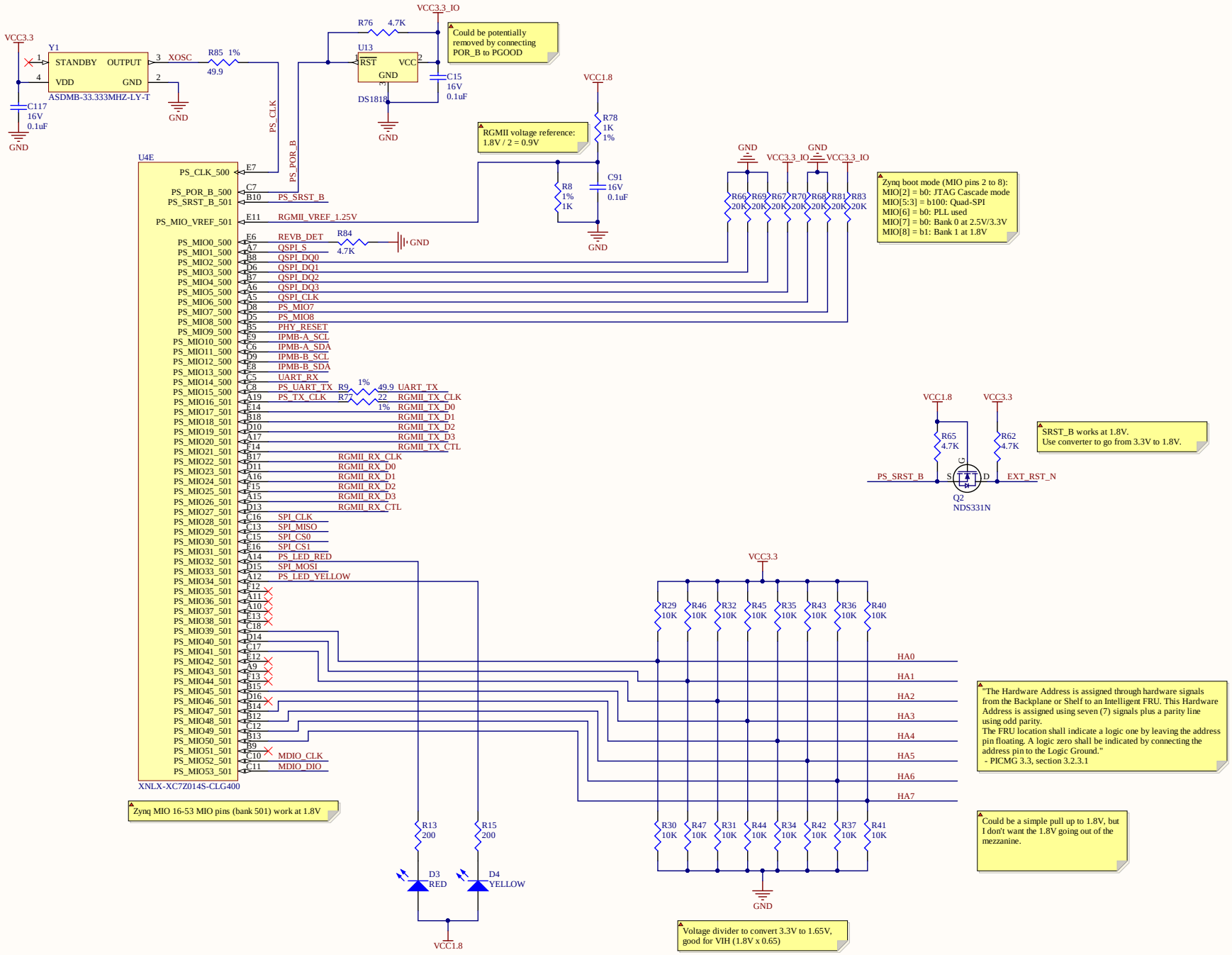


Description	**Mini-DIMM pinout**		
Title	***ZYNQ-IPMC***		*Univ. Wisconsin-Madison Madison, WI 53706*
Size: A3	Number: 2	Revision: revB1	
Date: 6/20/2019	Time: 3:03:48 PM	Sheet 2 of 11	
File: BoardConnector.SchDoc			Author: *Marcelo Vicente*



Description	**ZYNQ power wiring and JTAG**
Title	***ZYNQ-IPMC***
Size: A3	Number: 3 Revision: revB1
Date: 6/20/2019	Time: 3:03:49 PM Sheet 3 of 11
File: ZynqPower.SchDoc	

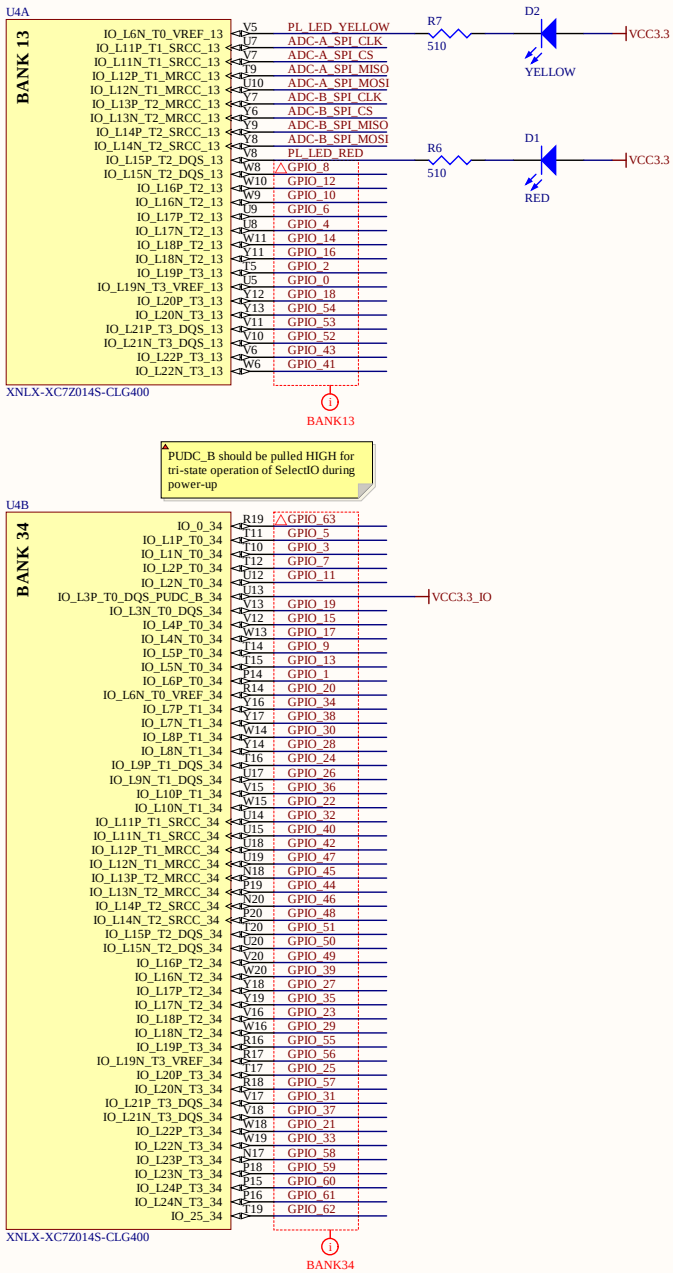
Univ. Wisconsin-Madison
Madison, WI 53706
Author: *Marcelo Vicente*



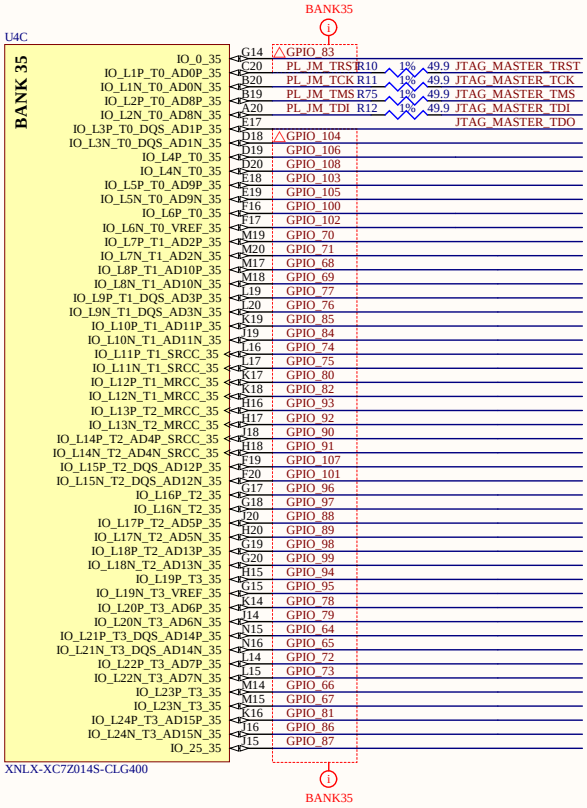
Description	**ZYNQ MIO connectivity**
Title	***ZYNQ-IPMC***
Size: A3	Number: 4 Revision: revB1
Date: 6/20/2019	Time: 3:03:50 PM Sheet 4 of 11
File: ZynqMIO.SchDoc	

Univ. Wisconsin-Madison
Madison, WI 53706

Author: *Marcelo Vicente*

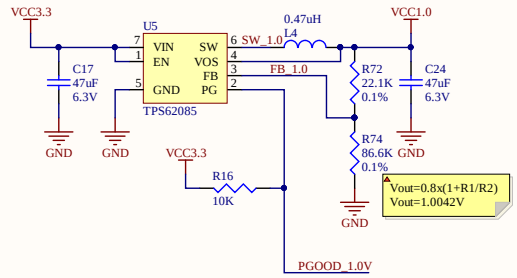


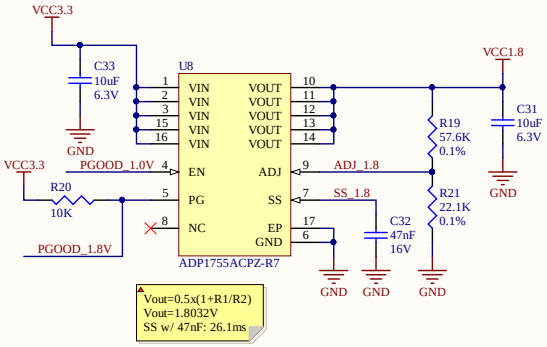
Description	**ZYNQ EMIO connectivity (banks 13 & 34)**		
Title	***ZYNQ-IPMC***		*Univ. Wisconsin-Madison Madison, WI 53706*
Size: A3	Number: 5	Revision: revB1	
Date: 6/20/2019	Time: 3:03:51 PM	Sheet 5 of 11	
File: ZynqEMIO.SchDoc			Author: *Marcelo Vicente*

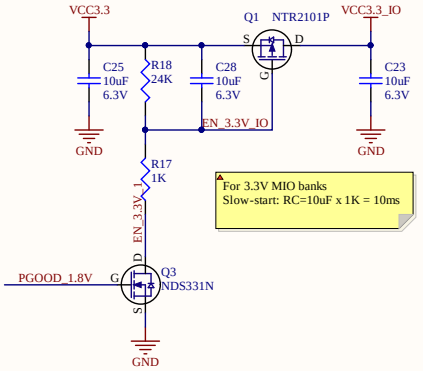


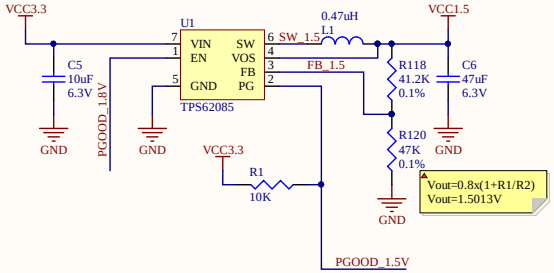
For the handle switch (HNDL_SW):
"Provide a right-angle 3-pin header, such as a Molex 53780-0390 or equivalent, to connect to a Face Plate-mounted microswitch within 25 mm of the lower recommended Component Side 2 keepout zone shown in Figure D-2, "PICMG 3.0 R1.0 overall Handle design." Pin 1 is the COMMON connection, Pin 2 is the NC (Normally Closed) contact, and Pin 3 is the NO (Normally Open) contact. Note: Front Board vendors need to ensure that they maintain the necessary Creepage and Clearance distances to any metal connected to Shelf Ground."
- PICMG 3.0 R3.0, D.1.1

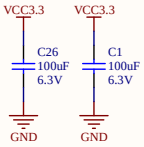
Description	**ZYNQ EMIO connectivity (banks 35)**		
Title	***ZYNQ-IPMC***		*Univ. Wisconsin-Madison Madison, WI 53706*
Size: A3	Number: 6	Revision: revB1	
Date: 6/20/2019	Time: 3:03:55 PM	Sheet 6 of 11	
File: ZynqEMIO_2.SchDoc			Author: *Marcelo Vicente*

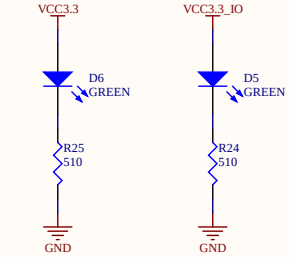




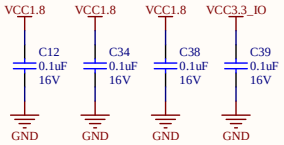




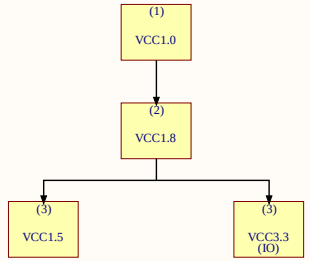




Stitching caps



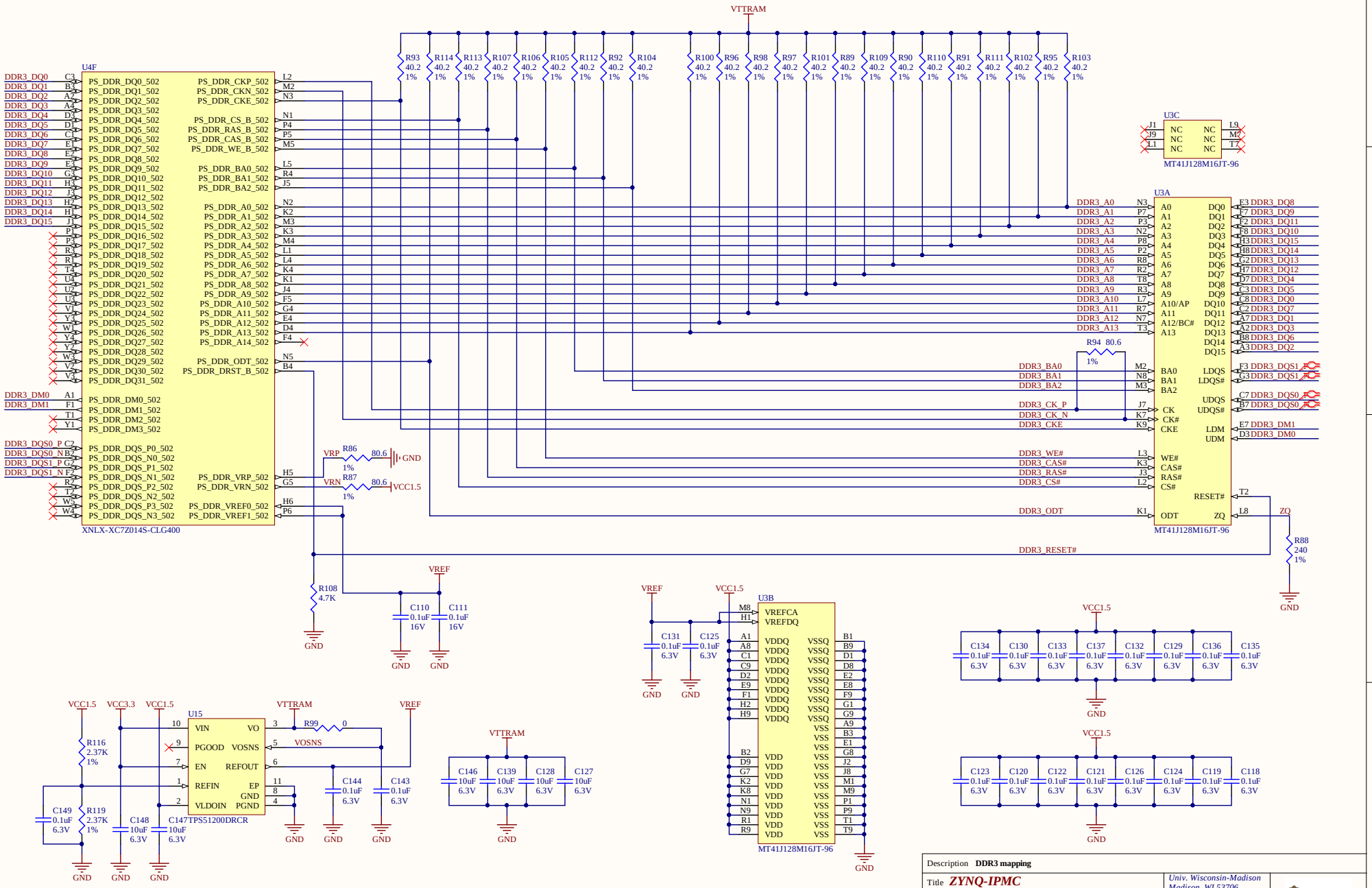
Power sequence for Zynq



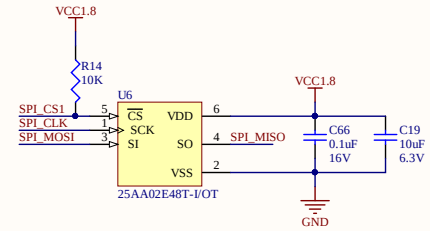
LDO converters are interchangable with the following components:
ADP1753 (0.8A) and ADP1741 (2.0A)

Potentially, a cheaper and small option is also available: LD39050 (0.5A, no soft-start) or LD39100 (1.0A, no soft-start)

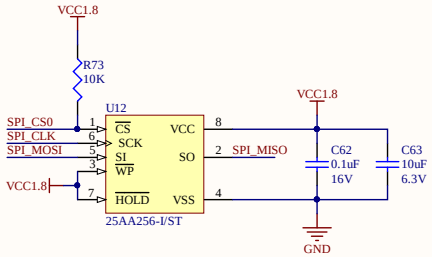
Description	**Power and sequencing**		
Title	***ZYNQ-IPMC***		*Univ. Wisconsin-Madison Madison, WI 53706*
Size: A3	Number: 7	Revision: revB1	
Date: 6/20/2019	Time: 3:04:00 PM	Sheet 7 of 11	
File: PowerSequence.SchDoc			Author: *Marcelo Vicente*

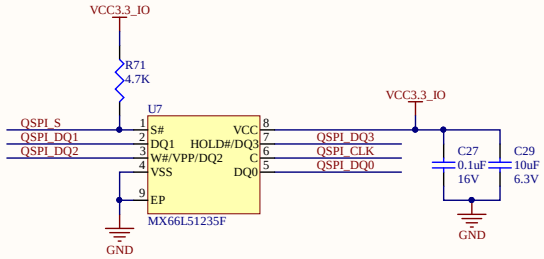


Description	**DDR3 mapping**		
Title	***ZYNQ-IPMC***		*Univ. Wisconsin-Madison* *Madison, WI 53706*
Size: A3	Number: 8	Revision: revB1	
Date: 6/20/2019	Time: 3:04:01 PM	Sheet 8 of 11	
File: ZynqDDR.SchDoc			Author: *Marcelo Vicente*



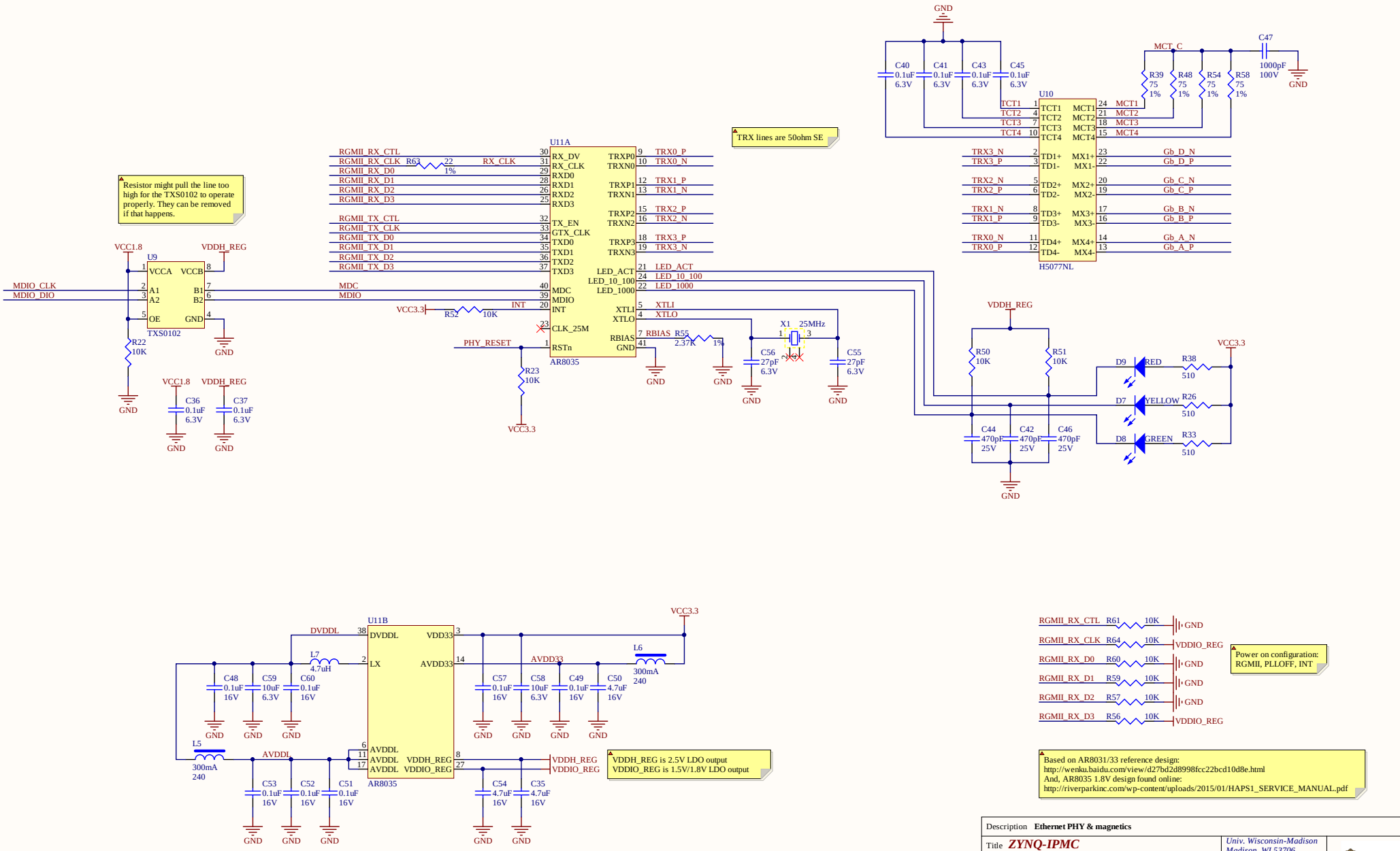
CS pins can be swapped if it improves layout



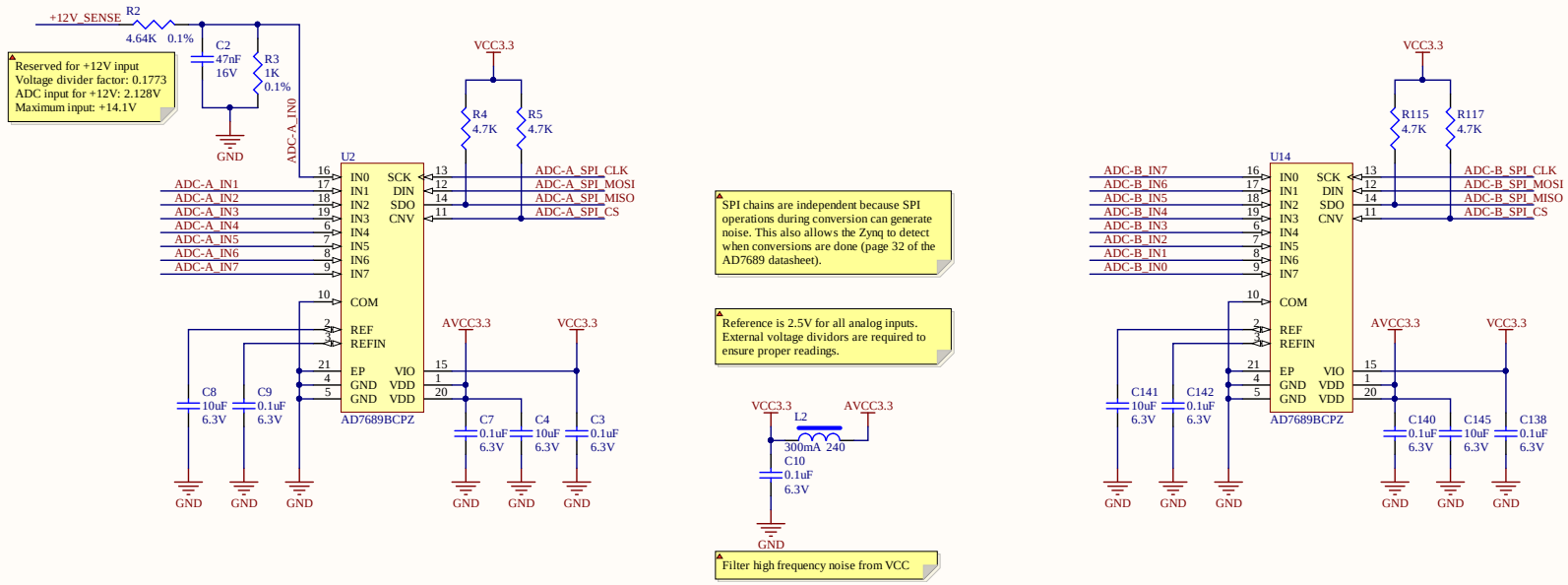


QSPI has 64MBytes
Needs 50ohm lines
C should be pulled LOW, but there is already the Zynq strap-pins.
40 MHz is the max speed allowed due to the hold times imposed by Zynq.
Check ZC702 schematic for more details.

Description	**EEPROMs and Flash**		
Title	***ZYNQ-IPMC***		*Univ. Wisconsin-Madison Madison, WI 53706*
Size: A3	Number: 9	Revision: revB1	
Date: 6/20/2019	Time: 3:04:01 PM	Sheet 9 of 11	
File: ZynqPeripherals.SchDoc			Author: *Marcelo Vicente*



Description	**Ethernet PHY & magnetics**		
Title	***ZYNQ-IPMC***		*Univ. Wisconsin-Madison Madison, WI 53706*
Size: A3	Number: 10	Revision: revB1	
Date: 6/20/2019	Time: 3:04:01 PM	Sheet 10 of 11	
File: Ethernet.SchDoc			Author: *Marcelo Vicente*



Description	**On-board ADCs**		
Title	***ZYNQ-IPMC***		*Univ. Wisconsin-Madison Madison, WI 53706*
Size: A3	Number: 11	Revision: revB1	
Date: 6/20/2019	Time: 3:04:02 PM	Sheet 11 of 11	
File: AnalogSense.SchDoc			Author: *Marcelo Vicente*