Jiawen Wu

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EDUCATION

Texas A&M University, College Station, TX — Aug 2023 – Jun 2028 (Expected)

- Ph.D. in Computer Engineering | *Advisor: Prof. Jeyavijayan Rajendran*

Tianjin University, Tianjin, China — Aug 2019 – Jun 2023

- B.S. in Electrical and Computer Engineering

PUBLICATIONS

- **Jiawen Wu** and Jeyavijayan Rajendran. "ChipZK: A Trusted Computing Infrastructure for Chiplets Using Zero-Knowledge Proofs," *SRC TECHCON*, 2025.
- Saichand Samudrala, **Jiawen Wu**, Chen Chen, Haoxuan Shan, Jonathan Ku, Yiran Chen, and Jeyavijayan Rajendran. "Performance Analysis of Zero-Knowledge Proofs," *IEEE International Symposium on Workload Characterization (IISWC)*, 2024.
- Jonathan Ku, Junyao Zhang, Haoxuan Shan, Saichand Samudrala, **Jiawen Wu**, Qilin Zheng, Ziru Li, Jeyavijayan Rajendran, and Yiran Chen. "ModSRAM: Algorithm-Hardware Co-Design for Large Number Modular Multiplication in SRAM," *Design Automation Conference (DAC)*, 2024.
- Jianan Mu, Huajie Tan, **Jiawen Wu**, Haotian Lu, Chip-Hong Chang, Shuai Chen, Shengwen Liang, Jing Ye, Huawei Li, and Xiaowei Li. "Energy-efficient NTT Design with One-bank SRAM and 2-D PE Array," *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2023.
- Zhuo Li, Huiyan Wang, Xiangdong Yi, Xinyi Zhang, **Jiawen Wu**, Yubin Zhang, Peng Luo, and Kaihua Liu. "PFDCT: An Enhanced Transport Layer Protocol for Precise Flow Control in Data Centers," *Electronics*, 2023.

PROFESSIONAL DEVELOPMENT

- Poster: ChipZK: A Trusted Computing Infrastructure for Chiplets Using Zero-Knowledge Proofs, *GCRI Summit*, 2025. — College Station, TX
- Talk & poster: ChipZK: A Trusted Computing Infrastructure for Chiplets Using Zero-Knowledge Proofs, *SRC TECHCON*, 2025. — Austin, TX
- Poster: Performance Analysis of Zero-Knowledge Proofs, *Design Automation Conference (DAC)*, 2025. — San Francisco, CA
- Poster: Performance Analysis of Zero-Knowledge Proofs, *Defense TechConnect Innovation Summit*, 2024. — Austin, TX
- Poster: Performance Analysis of Zero-Knowledge Proofs, *GCRI Summit*, 2024. — College Station, TX

SERVICE

- Reviewer for *IEEE Transactions on Smart Grid (TSG)*. — 2025

EXPERIENCES

Research Assistant | ZKP Acceleration Software / Hardware Co-Design — Aug 2023 – Present

Secure and Trustworthy Hardware (SETH) Lab, Texas A&M University, College Station, TX

- Performed comprehensive performance analyses of Zero-Knowledge Proof (ZKP) protocols on CPUs, identifying microarchitectural bottlenecks, memory consumption issues, and optimization opportunities.
- Provided critical insights for enhancing ZKP scalability and efficiency through microarchitecture-specific tuning and parallel computation strategies.

- Proposed a hardware-software co-design platform featuring efficient data representations for essential arithmetic operations (modular multiplication) and introduced a novel process-in-memory architecture to improve power efficiency.
- Implemented solutions and simulations across CPU, FPGA, and ASIC platforms.

Research Assistant | NTT Hardware Accelerator for PQC/FHE Dec 2022 – Jun 2023
Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China

- Developed a scalable, conflict-free design methodology for a Number Theoretic Transform (NTT) hardware accelerator by formulating a novel memory partition and coefficient assignment scheme that eliminates pipeline stalls regardless of polynomial length, modulus, or number of processing elements.
- Validated the conflict-free memory pattern and estimated the achievable clock cycles through FPGA and ASIC simulation of the generated accelerator designs.

Research Assistant | Data Center Network Congestion Control Apr 2021 - Apr 2022

School of Microelectronics, Tianjin University, Tianjin, China

- Developed a data center fat-tree network topology on the ns3 platform and compared the performance of different algorithms, including TCP NewReno, DCTCP, L2DCT, and ICTCP.
- Proposed a new PFDCT algorithm deployed on sender, giving timeout caused by packet transmissions different priorities, achieving 20% higher fairness with good throughput and flow complete time.

PROJECTS

Sparse CNN Inference Hardware Accelerator Design Dec 2022 – Jun 2023
School of Microelectronics, Tianjin University, Tianjin, China

- Implemented a sparse data encoding compression scheme with per-channel expansion on Xilinx FPGA platform with AMD Vitis HLS and evaluated on VGG network.
- Achieve up to 3.08× speedup and 2.3× energy efficiency improvement compared to the dense CNN accelerator.

Automatic Management of Devices for Robotic Applications Jul 2022 - Aug 2022
Department of Computer Science, The University of Hong Kong, Remote

- Designed a layer of device pooling that allows multiple apps to apply the use of devices automatically on ROS.

Sobel Edge Detection Hardware Accelerator Design Mar 2022 - Jun 2022
School of Microelectronics, Tianjin University, Tianjin, China

- Developed Sobel edge detection algorithm on a Xilinx Zynq FPGA, and implemented through HLS-level design methodology.

The Design of 2.4GHz RF Power Amplifier Based on CMOS Process Sep 2021 - Dec 2021
School of Microelectronics, Tianjin University, Tianjin, China

- Designed a three-stage differential linear power amplifier operating at 2.4 GHz using SMIC 180-nm CMOS. Results show that our design achieved a 26.67dBm maximum output power and a PAE of 21.06%.

TEACHING EXPERIENCE

Teaching Assistant | Security of Embedded Systems (ECEN 426 / ECEN 759) Fall 2024, Fall 2025
Department of Electrical and Computer Engineering, Texas A&M University, College Station, TX

- Assisted in teaching an undergraduate course with 50 in-person and 55 online students.
- Mentored lab projects focused on temporal thermal covert channels in FPGAs and hardware trojans detection.
- Worked under the guidance of Prof. Jeyavijayan Rajendran.

TECHNICAL SKILLS

Programming Languages: C++, Python, Verilog, Go, Rust.
Tools: Synopsys DC, Synopsys VCS, Synopsys LC, AMD Xilinx Vivado, AMD Xilinx Vitis, Intel VTune Profiler, perf, Docker, gem5.