老叶说事
《高阶会员专属-第3期》

IEEE期刊论文导读：带你彻底了解死区补偿的本质与可行的补偿方法

《高阶会员专属-第3期》IEEE期刊论文导读：带你彻底了解死区补偿的本质与可行的补偿方法

IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 11, NO. 2, MARCH 1996

Inverter Output Voltage Synthesis Using Novel Dead Time Compensation

Jong-Woo Choi, *Student Member, IEEE,* and Seung-Ki Sul, *Member, IEEE*

《高阶会员专属-第3期》IEEE期刊论文导读：带你彻底了解死区补偿的本质与可行的补偿方法

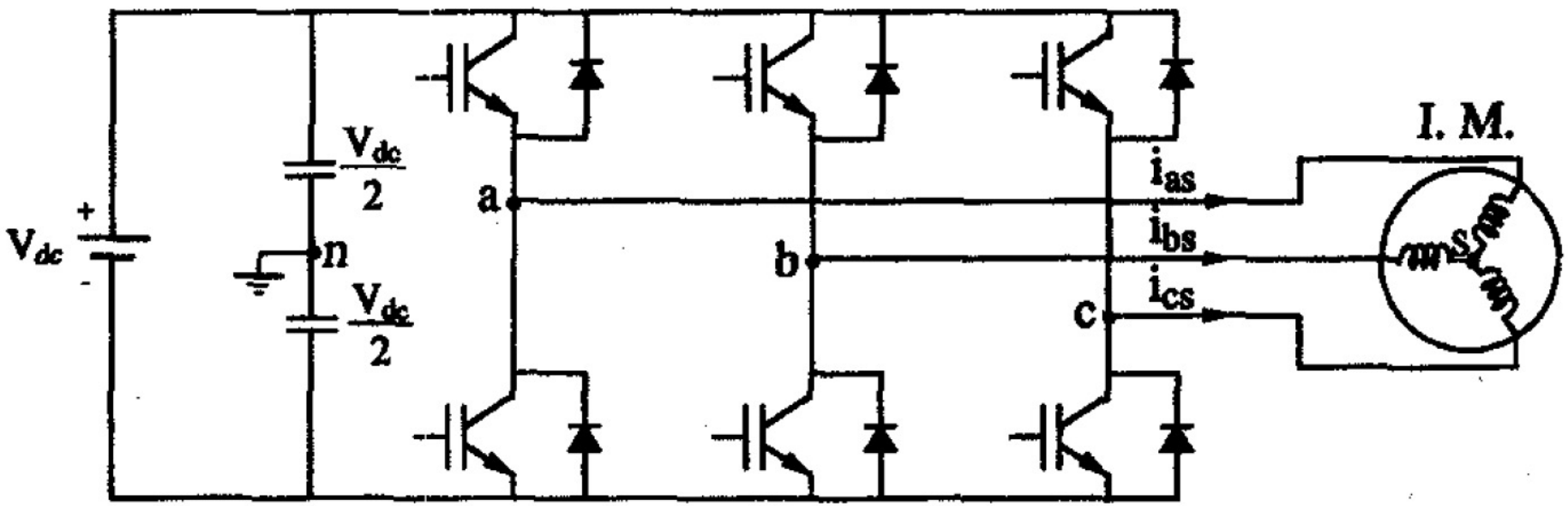


Fig. 1. Three-phase PWM inverter with an induction motor load.

《高阶会员专属-第3期》IEEE期刊论文导读：带你彻底了解死区补偿的本质与可行的补偿方法

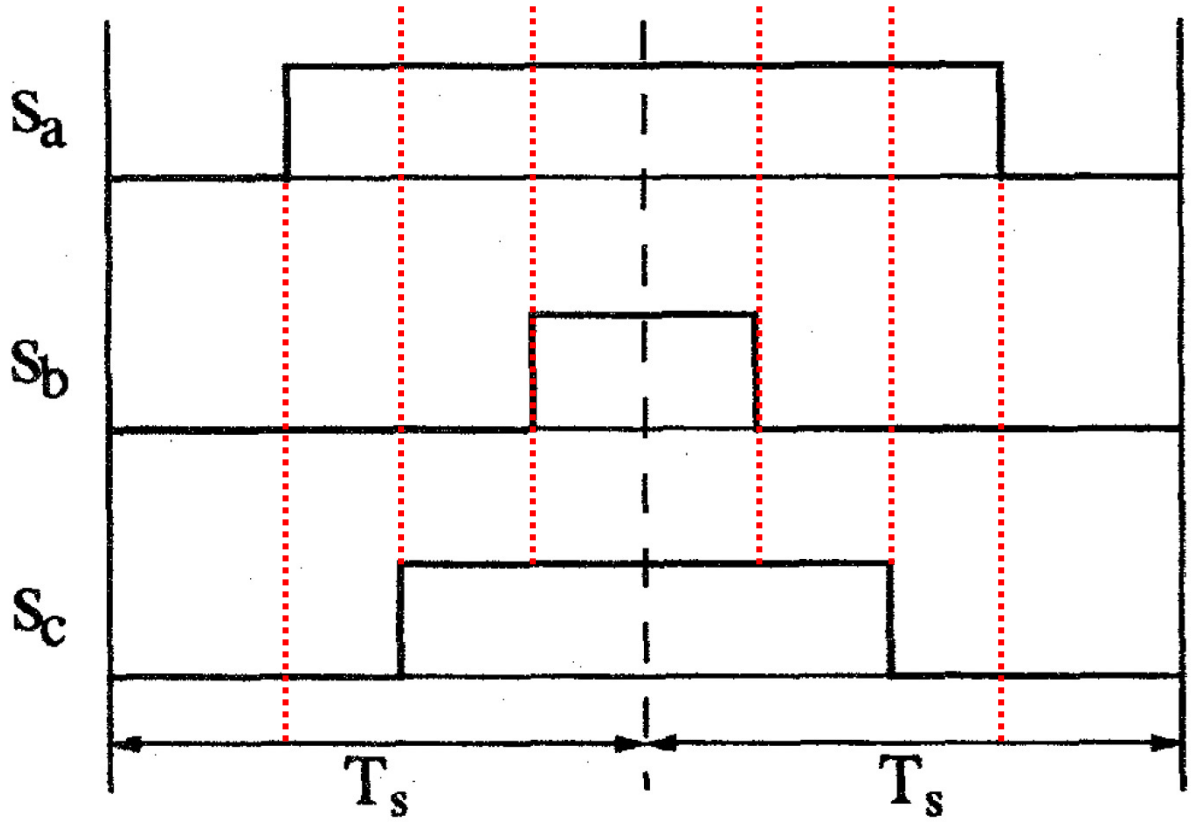
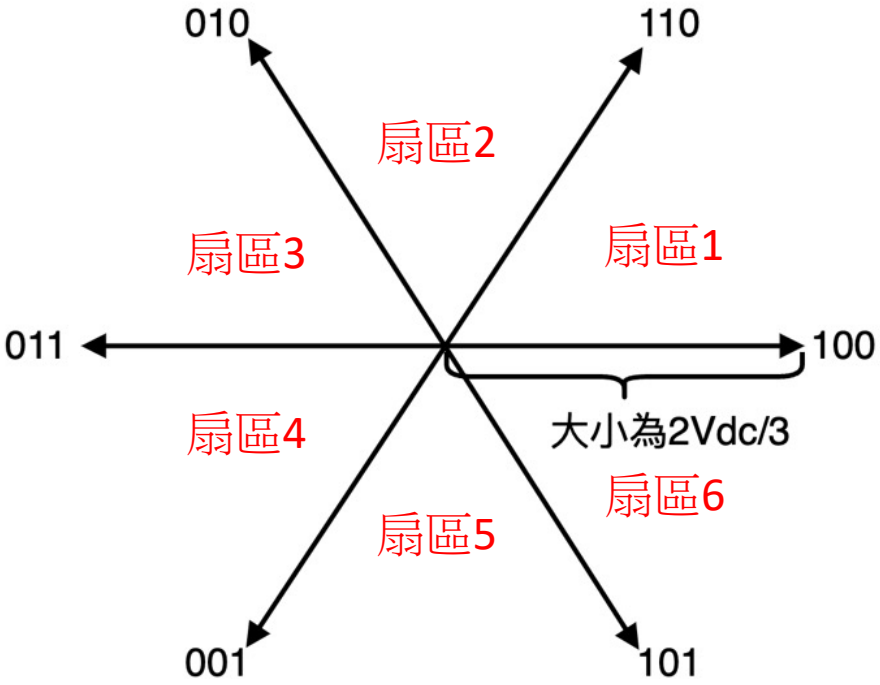


Fig. 2. Typical gating pulse pattern of the space vector PWM.



《高阶会员专属-第3期》IEEE期刊论文导读：带你彻底了解死区补偿的本质与可行的补偿方法

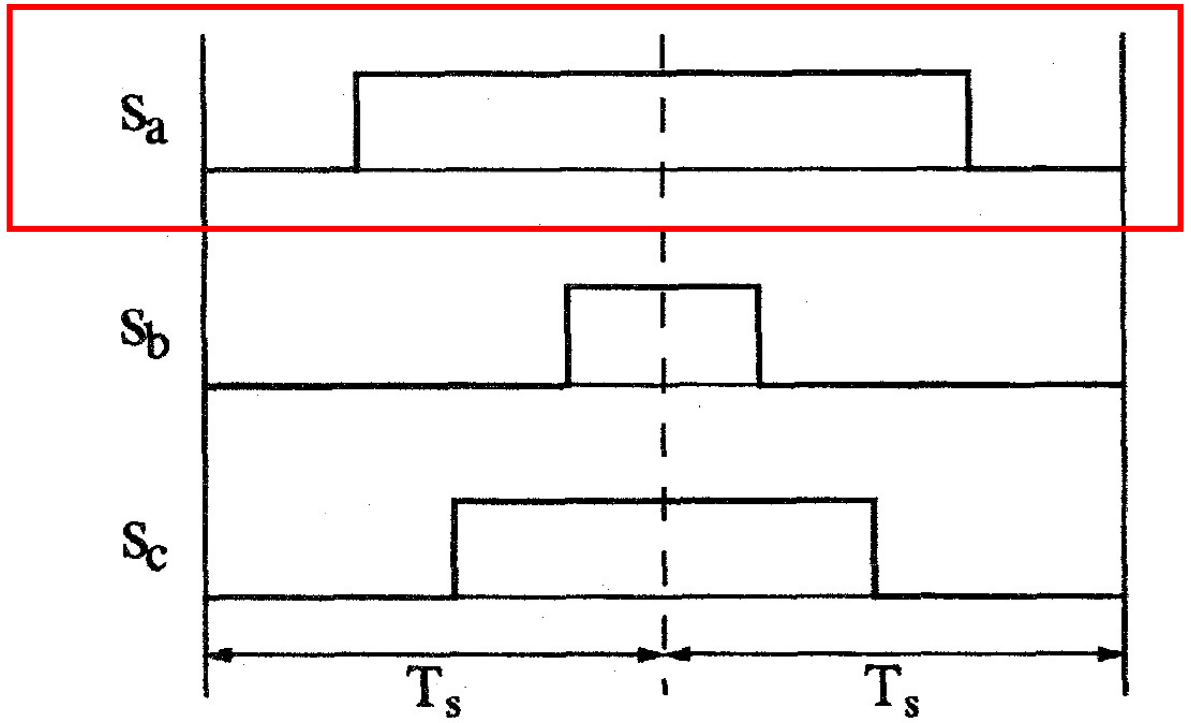
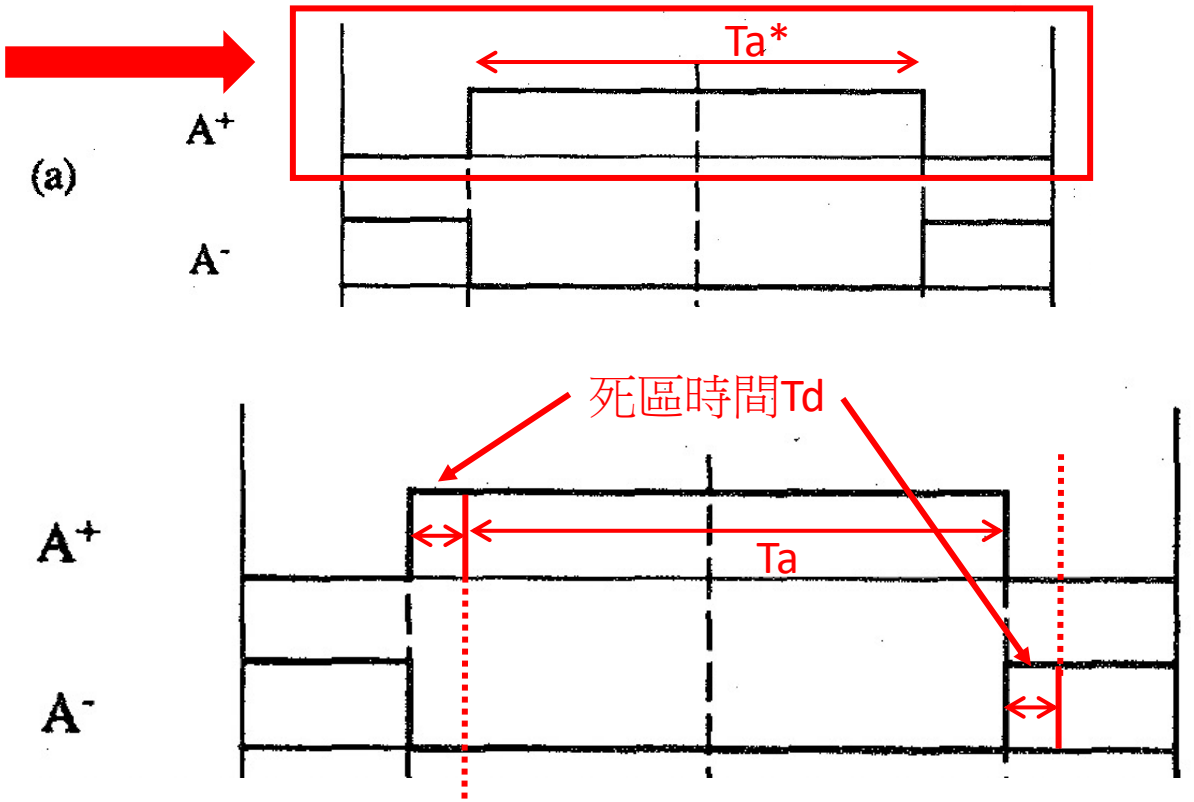


Fig. 2. Typical gating pulse pattern of the space vector PWM.



若a相電流為正（流入馬達），則死區時間中，電流將透過a臂下方的二極體續流，讓VaN為-Vdc/2

the upper diode will conduct. From this concept, the novel

《高阶会员专属-第3期》IEEE期刊论文导读：带你彻底了解死区补偿的本质与可行的补偿方法

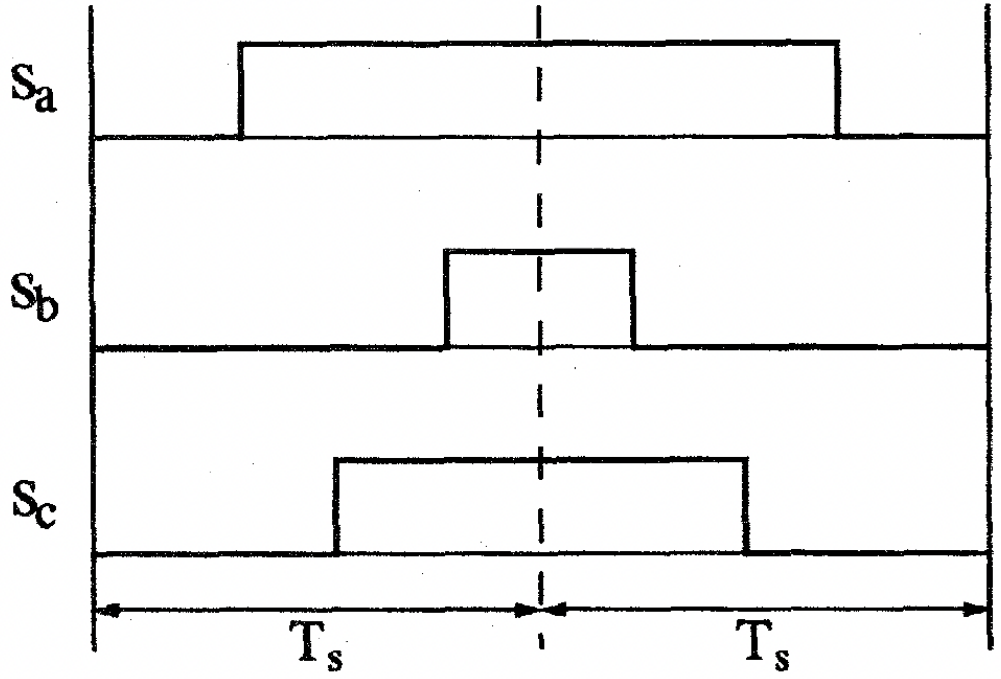
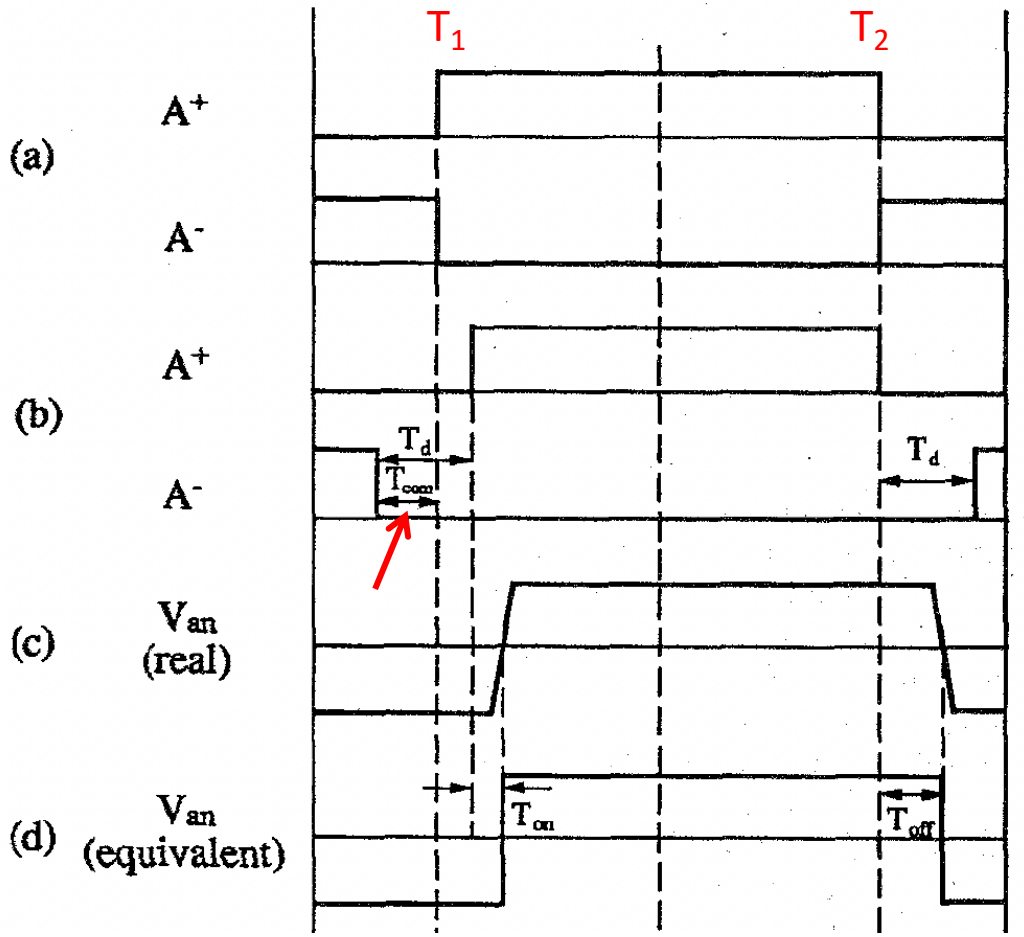


Fig. 2. Typical gating pulse pattern of the space vector PWM.

the upper diode will conduct. From this concept, the novel dead time compensation method may be illustrated as follows



《高阶会员专属-第3期》IEEE期刊论文导读：带你彻底了解死区补偿的本质与可行的补偿方法

III. Voltage Distortion Analysis and Compensation Strategy

In PWM inverter system, in addition to dead time effect there exist the voltage drops of the power devices that distort the output voltage. If the current (i_{as}) flows to load, the actual phase to center voltage is

$$v_{an} = \frac{V_{dc}}{2} - V_{ce} \quad (\text{when } S_a = 1) \tag{8}$$

$$v_{an} = -\frac{V_{dc}}{2} - V_d \quad (\text{when } S_a = 0) \tag{9}$$

where

V_{ce} voltage drop of the active switch

V_d voltage drop of freewheeling diode

S_a 1 (upper switch is on), 0 (lower switch is on).

When the current (i_{as}) flows from load, the actual phase to center voltage is varied as

$$v_{an} = \frac{V_{dc}}{2} + V_d \quad (\text{when } S_a = 1) \tag{10}$$

$$v_{an} = -\frac{V_{dc}}{2} + V_{ce} \quad (\text{when } S_a = 0). \tag{11}$$

So, the actual phase to center voltage by considering the voltage drop of the power devices varies with switching state and current direction, and it can be written in the form assuming that the current direction does not change for a sampling period, which is reasonable in high-frequency switching

$$v_{an} = (V_{dc} - V_{ce} + V_d)\left(S_a - \frac{1}{2}\right) - \frac{1}{2}\text{sign}(i_{as})(V_{ce} + V_d). \tag{12}$$

Generally, the voltage drops of the active switch and freewheeling diode increase with current. Thus, it may be assumed that the voltage drops of the active switch and of the freewheeling diode linearly increases with current at the normal operating region and can be modeled as follows:

$$V_{ce} = V_{ce0} + r_{ce}|i_{as}| \tag{13}$$

where

V_{ce0} threshold voltage of the active switch

r_{ce} on-state slope resistance of the active switch

$$V_d = V_{d0} + r_d|i_{as}| \tag{14}$$

用線性模型對開關與二極管建模