A Compensation Method for Time Delay of Full-Digital Synchronous Frame Current Regulator of PWM AC Drives

Bon-Ho Bae, *Member, IEEE,* and Seung-Ki Sul, *Fellow, IEEE*

***Abstract*—The voltage output is inevitably delayed in a full-digital implementation of a current regulator due to an arithmetic calculation and the pulsewidth modulation. In the case of the synchronous frame current regulator, the time delay is accompanied by a frame rotation. In some applications where the ratio of the sampling frequency to the output frequency is insufficient, such as a high-power drive or a super-high-speed drive, the effect of the frame rotation during the delay time causes a phase and magnitude error in the voltage output. The error degrades the dynamic performance and can cause instability in the current regulator at high speed. It is also intuitively known that advancing the phase of the voltage output can mitigate this instability. In this paper, the errors in the voltage output and the instability problems have been studied analytically and a compensation method for the error is proposed. Using a computer simulation and complex root locus analysis, a comparative study with conventional methods has been carried out and the utility of the proposed method has been verified experimentally.**

***Index Terms*—Digital delay, pulsewidth-modulation (PWM) ac drives, synchronous reference frame current regulator.**

I. Nomenclature

Symbols

e	Back electromotive force (EMF) voltage.
i	Instantaneous currents.
j	Operator $= 1\angle\pi/2$.
L, R	Inductance and resistance.
ω	Angular frequency.
V	Instantaneous voltages.
λ	Flux.

Subscripts (Used Singly or in Combination)

s, m, r	Stator, mutual, and rotor.
d, q	d and q axes.
$\_ff$, $\_fb$	Feedforward and feedback term.
e	Synchronous reference frame.

Superscripts (Used Singly or in Combination)

s, e	Satic and synchronous reference frame.
$*$	Reference value.

Paper IPCSD 02–084, presented at the 2001 Industry Applications Society Annual Meeting, Chicago, IL, September 30–October 5, and approved for publication in the IEEE Transactions on Industry Applications by the Industrial Drives Committee of the IEEE Industry Applications Society. Manuscript submitted for review November 1, 2001 and released for publication February 17, 2003.

B.-H. Bae is with the General Motors Corporation Advanced Technology Center, Torrance, CA 90505 USA (e-mail: bonho.bae@gm.com).

S.-K. Sul is with the School of Electrical Engineering #024, Seoul National University, Seoul 151-742, Korea (e-mail: sulsk@plaza.snu.ac.kr).

Digital Object Identifier 10.1109/TIA.2003.810660

II. Introduction

In a modern digital ac drive system, all the signal processes including the current regulation loop and the pulsewidth-modulation (PWM) block are implemented in the digital domain. In addition, the synchronous frame current regulator has become the industry standard for regulating the current in polyphase ac machines due to its capability to control the ac signals over a wide frequency range [1], [2]. In a full-digital implementation, there is an inevitable execution time delay, which is commonly one sampling period. Furthermore, in implementing PWM logic in a digital way, there is a further time delay. The delay caused by the PWM is complex to analyze, but a half sampling time delay of a zeroth-order holder is a good approximation for a space-vector PWM (SVPWM), which places active vectors at the center of a PWM period. If the PWM information is updated at each sampling point, there is a minimum time delay of one-and-a-half sampling periods. In the case of a synchronous frame current regulator, the time delay results in an angle error by a frame rotation, which causes a phase and magnitude error in the voltage output. In general-purpose ac drive applications, such errors can be neglected in the design of a current regulator. However, in some applications where the ratio of the sampling frequency to the output frequency is insufficient, such errors deteriorate the system performance considerably and the system can even be unstable as a result of the error. In a traction drive, the switching frequency of the inverter is still approximately in the 1-kHz range but the maximum output frequency is in the range of a few hundred hertz, and the ratio between the switching frequency and the output frequency is less than 10. Even using the asymmetrical PWM, which updates the output voltage twice per cycle, a one-and-a-half sampling period delay corresponds to approximately 20° in the electric angle at the top speed of the drive. Furthermore, in an active power filter whose power rating is lower than the MVA range, the switching frequency is around a few kilohertz, but the maximum frequency to synthesize considering the 13th harmonics is 780 Hz. Again, the ratio between the switching frequency and the output frequency is less than 10. Even with latest insulated gate bipolar transistor (IGBT) technology where the switching frequency can be as high as 20 kHz, in the field of a high-frequency direct-drive air compressor and micro gas turbine generator, the output frequency of the inverter should extend to the kilohertz range. Once more, the effect of a delay to the rotation of a

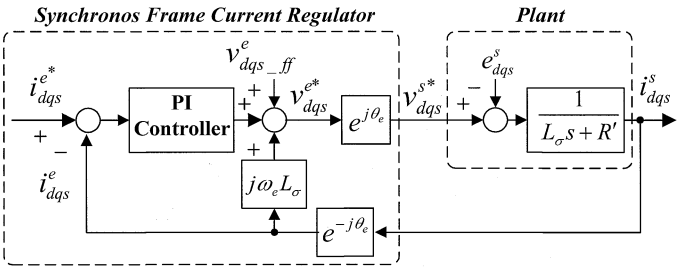


Fig. 1. Complex vector block diagram of a synchronous frame current regulator with a decoupling control.

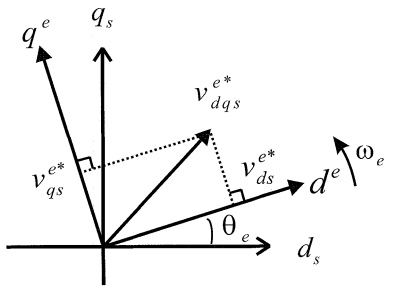


Fig. 2. Synchronous reference frame quantities represented in the stationary reference frame.

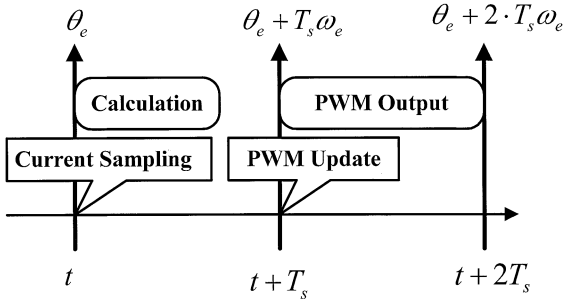


Fig. 3. Time sequence of current sampling, calculation, and PWM output.

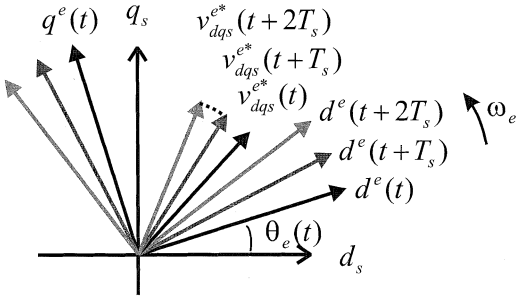


Fig. 4. Rotation of the synchronous reference frame corresponding to the time sequence.

synchronous frame would be an essential issue when trying to obtain a reasonable operating performance.

The problem caused by the delay time has attracted a great deal of interest. The degradation of the current control performance in a slow switching application was studied and a dynamic current tracking control was proposed, which is based on the synchronous optimal PWM and requires offline calculation [3]. Some authors focused on the time delay in the sampling of the voltage and current signals, and analyzed the limitation of the bandwidth of a current regulator according to the time delay in the sampling and the PWM [4]–[6]. In addition, some papers focused on the effect of the signal measurement and processing delay on the compensation of the harmonics by the PWM converter [7]. However, the analyses did not consider the characteristics of the synchronous frame current regulator caused by the rotation of the reference frame during the delay time. On the other hand, it is intuitively known that advancing the phase of the voltage output can mitigate the performance degradation [8].

This paper focuses on both deriving and evaluating an analytic solution to compensate for the error caused by a frame rotation during the time delay from the current sampling to the output of the PWM. In addition, a compensation method for the error is proposed and its effectiveness are verified by a comparative study based on computer simulations and experiments. Using the complex vector root locus, it is shown that the proposed compensation method could solve the instability problem of the current regulator even with a relatively large delay angle.

III. Synchronous Frame Current Regulator

The complex vector block diagram of a synchronous frame current regulator with a decoupling control is shown in Fig. 1. With the load of an induction motor, the decoupling terms and back-EMF voltage are as follows [9]:

$$v^e_{dqs\_\mathrm{ff}} = e^e_{dqs} = -R_r\frac{L_m}{L_r^2}\lambda^e_{dqr} + j\omega_r\frac{L_m}{L_r}\lambda^e_{dqr}. \tag{1}$$

In addition, the equivalent R–L terms are as follows:

$$L_\sigma = L_s - \frac{L_m^2}{L_r} \quad R' = R_s + \left(\frac{L_m}{L_r}\right)^2 R_r. \tag{2}$$

In the case of the permanent-magnet synchronous motor (PMSM),

$$v^e_{dqs\_\mathrm{ff}} = e^e_{dqs} = j\omega_r K_e \tag{3}$$

where K_e is the back-EMF constant. The equivalent R–L terms are as follows:

$$L_\sigma = L_s \quad R' = R_s. \tag{4}$$

The angle between the synchronous reference frame and the stationary reference frame is represented by θ_e. In the case of the rotor-flux-oriented control of an induction motor, θ_e is the phase of the rotor flux in the stationary frame. A quantity in the synchronous frame can be represented as a stator referred quantity as shown in Fig. 2. Moreover, with a rotational transformation by θ_e, the transformations of the current and voltage are given by

$$v^{s^*}_{dqs} = v^{e^*}_{dqs}e^{j\theta_e} \tag{5}$$

$$i^{e^*}_{dqs} = i^{s^*}_{dqs}e^{-j\theta_e}. \tag{6}$$

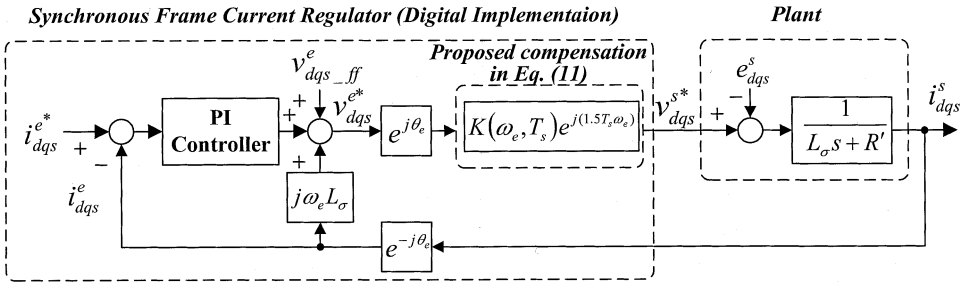


Fig. 5. Complex vector block diagram of the synchronous frame current regulator using the proposed compensator.

IV. Compensation Method for Time Delay of Full-Digital Synchronous Frame Current Regulator

Fig. 3 shows the typical time sequence of current sampling, computation, and the PWM output, where T_s is the sampling period of the current regulator. As shown in Fig. 3, one sampling time is delayed during the execution of the control algorithm. In addition, the PWM output is refreshed after one sampling time at $(t+T_s)$, and the PWM output is activated during the next period from $(t+T_s)$ to $(t+2T_s)$. In the case without a time delay, the voltage vector in the synchronous frame $v^{e^*}_{dqs}$, which is the output of current regulator, is represented in a stationary frame, as shown in Fig. 2, and the transformation to the stationary reference frame is given by (5). However, in practical cases with the time sequence of Fig. 3, the synchronous reference frame rotates and the trace of a voltage output moves, as shown in Fig. 4. In Fig. 4, the rotation of the synchronous frame is represented by $d_e(t)$, $d_e(t+T_s)$, and $d_e(t+2T_s)$ and the corresponding trace of the voltage vector in the digital implementation $v^{e^*}_{dqs}$ is expressed by $v^{e^*}_{dqs}(t)$, $v^{e^*}_{dqs}(t+T_s)$, and $v^{e^*}_{dqs}(t+2T_s)$. Because the PWM output is activated from $(t+T_s)$ to $(t+2T_s)$, the voltage output $v^{e^*}_{dqs}$ is represented as the stator referred quantity by the dotted trace between the voltage vector $v^{e^*}_{dqs}(t+T_s)$ and $v^{e^*}_{dqs}(t+2T_s)$. Under the assumption that the synchronous frequency ω_e is constant during the time delay, the stator referred voltage reference for the PWM generation $v^{s^*}_{dqs\_\mathrm{digital}}$ can be derived as (8) by averaging the dotted trace of voltage vector shown in Fig. 4

$$v^{s^*}_{dqs\_\mathrm{digital}} = \frac{1}{T_s}\int_{Ts}^{2Ts} v^{e^*}_{dqs} e^{j(\omega_e\tau+\theta_e)} d\tau \tag{7}$$

$$= K(\omega_e, T_s)\, e^{j(1.5T_s\omega_e+\theta_e)} v^{e^*}_{dqs} \tag{8}$$

where

$$K(\omega_e, T_s) \equiv \frac{2}{\omega_e T_s}\sin\left(\frac{\omega_e T}{2}\right). \tag{9}$$

If the R–L time constant is longer enough when compared to the sampling time, the current can be derived by integrating the difference between the output voltage and the back-EMF, and the current developed by the voltage calculated by (8) coincides with that developed by the voltage trajectory represented by the dotted line in Fig. 4.

From the relationship between the voltage output of the ideal case in (5) and that of the time-delayed case in (8), the error caused by the conventional transformation in (5) can be calculated as follows:

$$f_{\mathrm{error}} = \frac{e^{j\theta_e} v^{e^*}_{dqs}}{K(\omega_e, T_s)\, e^{j(1.5T_s\omega_e+\theta_e)} v^{e^*}_{dqs}} = \frac{e^{j(-1.5T_s\omega_e)}}{K(\omega_e, T_s)}. \tag{10}$$

From (10), the error in the voltage output caused by the frame rotation can be summarized as follows.

1) The magnitude of the voltage vector is changed by a scalar value $1/K(\omega_e, T_s)$ which is larger than a single unit.
2) The phase of the voltage vector is delayed by the rotating angle of the reference frame during one-and-a-half sampling periods.

From the error equation, a compensation method for the time delay in the full-digital synchronous current regulator can be derived using the inverse function of the error as follows:

$$f_c = \frac{1}{f_{\mathrm{error}}} = K(\omega_e, T_s)\, e^{j(1.5T_s\omega_e)}. \tag{11}$$

Fig. 5 shows the complex vector block diagram of a synchronous current regulator with the proposed compensation method in (11).

TABLE I
Parameters of PMSM and Specifications of Control

Motor Parameters	
Rated power	1 kW
Number of poles	8
Rated current	5.7 A_{rms}
Rated torque	3.18 Nm
Rated speed	3,000 r/min
Maximum speed	5,000 r/min
Stator inductance, L_s	6.5 mH
Stator resistance, R_s	0.9155 Ω
Control Parameters	
Sampling time	400μs
Switching frequency	1.25 kHz
Current control bandwidth	100 Hz

V. Simulation 1

A computer simulation was carried out to investigate the validity of the proposed compensation method of (11). The parameters of the 1-kW PMSM and simulation conditions are shown in Table I.

The simulation was coded using MATLAB/Simulink with the time sequence shown in Fig. 3, and the SVPWM was precisely

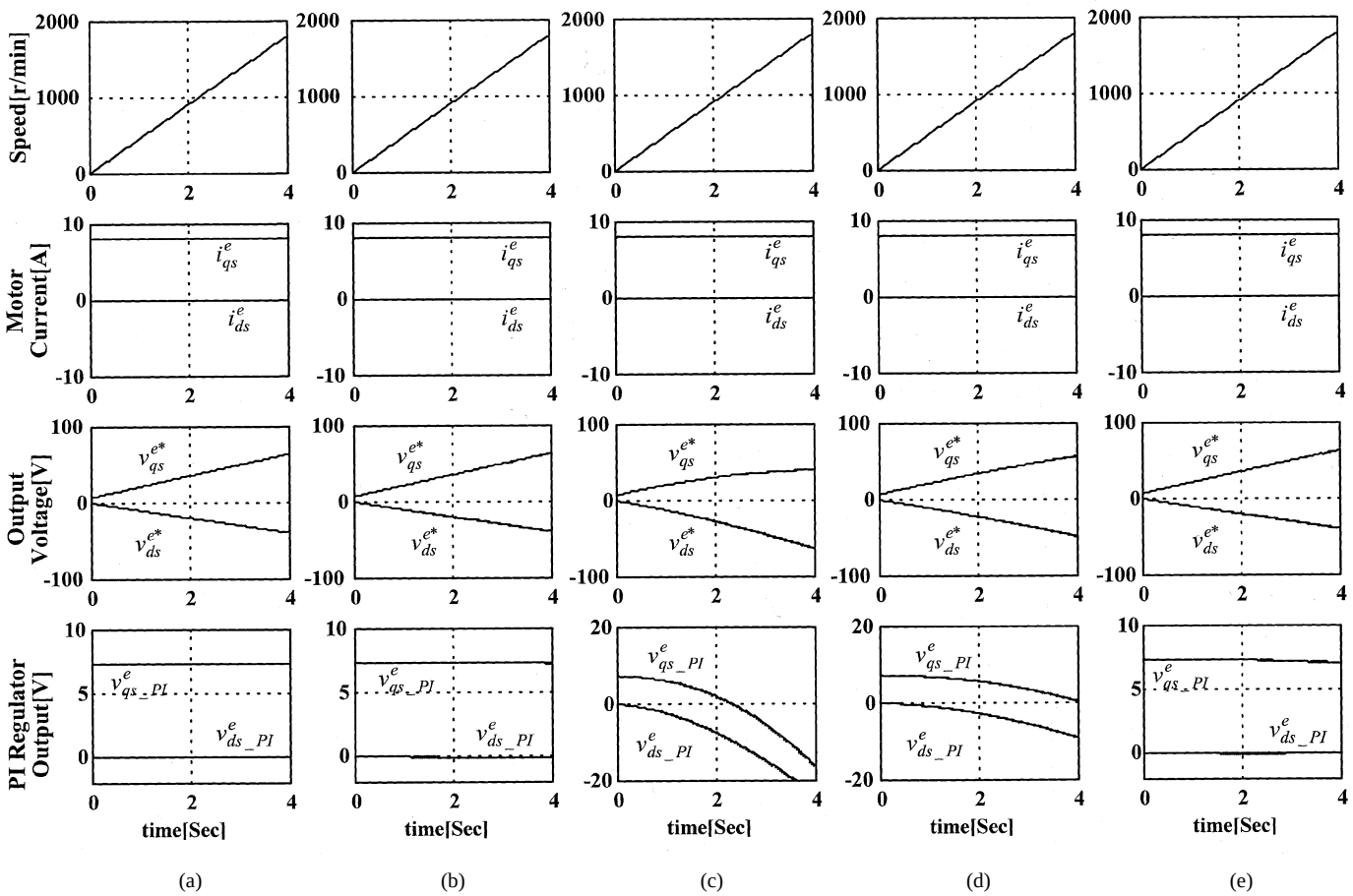


Fig. 6. Simulation reslults of the current regulators with the conventional and proposed compensation methods. (a) Analog implementation. (b) Digital implementation with the proposed method. (c) Digital implementation without compensation. (d) Digital implementation only with phase advancing, $f_c = e^{j(Ts\omega^e)}$. (e) Digital implementation only with phase advancing, $f_c = e^{j(1.5Ts\omega^e)}$.

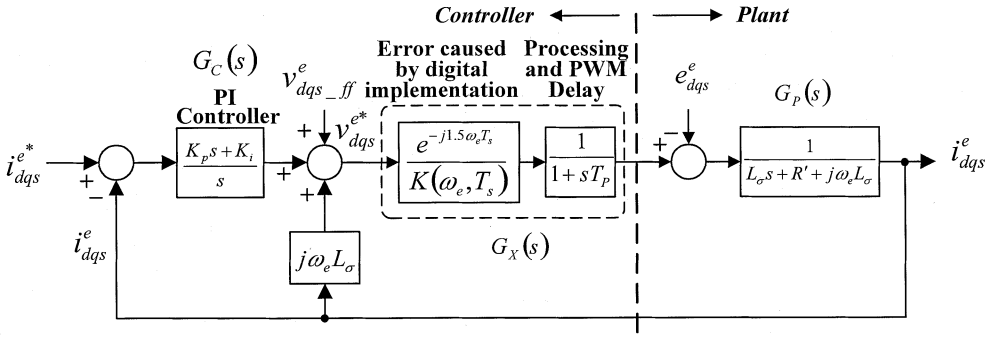


Fig. 7. Complex vector block diagram of a synchronous current regulator without compensation.

implemented by the simulink C mex-files. The results of the simulations are shown in Fig. 6. The PMSM was accelerated slowly from a standstill to a speed of 1800 r/min. From the top to the bottom, the traces show the motor speed, the $d-q$ currents, the voltage output of the synchronous current regulator, and the voltage output of the proportional and integral (PI) controller. Because the errors in the voltage output are compensated for by the PI controller of the current regulator, the traces of the voltage outputs of the PI regulator $V^e_{ds\_PI}$ and $V^e_{qs\_PI}$ reflect the errors caused by the digital implementation. In the case of analog implementation [of Fig. 6(a)] and the digital implementation with the proposed compensation [of Fig. 6(b)], the traces of the control variables are identical and the voltage outputs of the PI current regulator are constant corresponding to the constant currents. This result shows that the proposed method effectively compensates for the error in the voltage output caused by the digital implementation. However, the errors in the voltage outputs increase in proportion to the excitation frequency, and the outputs of the PI current regulator deviate from the constant values in the case of the digital implementation without compensation [of Fig. 6(c)]. From the results with the conventional intuitive compensation methods [of Fig. 6(d) and (e)], it can be seen that the phase leading technique is not perfect but is effective in mitigating the errors.

TABLE II
PARAMETERS OF LOAD AND SPECIFICATIONS OF CONTROL

R	0.9166 Ω
Lσ	6.5 mH
Sampling time T_s	400 μs
Current control bandwidth	100 Hz

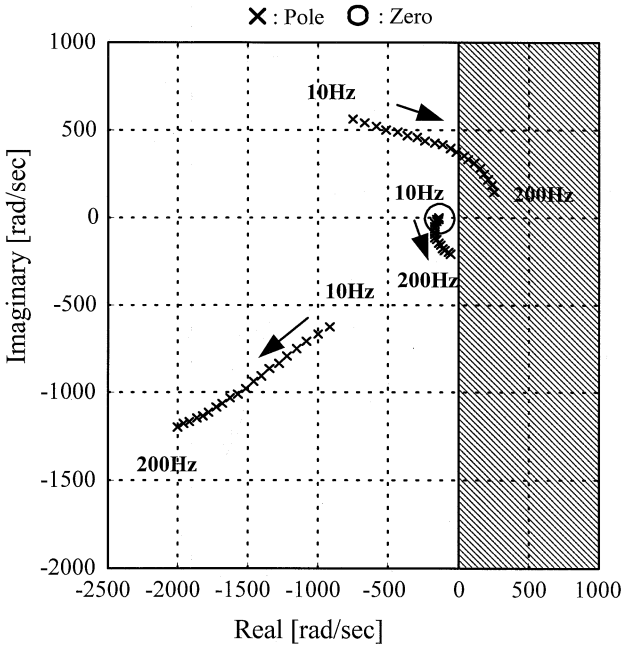
VI. INSTABILITY PROBLEM OF CONVENTIONAL METHOD

It is known that the synchronous current regulator is able to regulate the ac signals over a wide frequency range. However, in some applications where the ratio of the sampling frequency to the output frequency is insufficient, it can be seen that the synchronous current regulator loses its stability as the excitation frequency increases. In this section, the stability problems are discussed by means of complex vector root locus analysis.

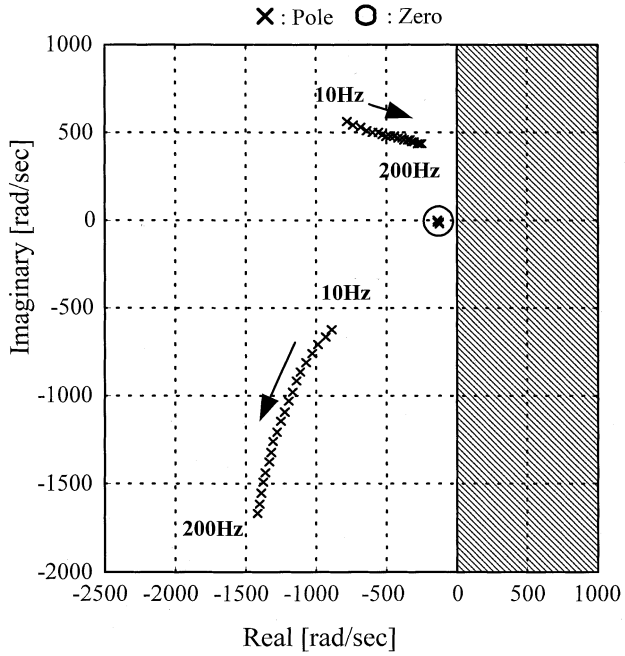
Fig. 7 shows the complex vector block diagram of the conventional synchronous current regulator with the error caused by the time delay and the frame rotation. The time delay was modeled as a first-order low-pass filter [4]. The delay caused by the processing and the PWM output T_p was approximated as one-and-a-half sampling periods. The sampling/feedback delay of the current measurement was neglected on the assumption that the fundamental component of current is instantaneously sampled at the midpoint of zero space vectors [4], [10]. The PI current regulator was tuned by selecting a controller zero equals to the break frequency of the R–L load, i.e., $K_i/K_p = R'/L_\sigma$. Using the complex vector notation shown in Fig. 7, the transfer function of the current regulator can be derived as (12)

$$\frac{i^e_{dqs}}{i^{e*}_{dqs}} = \frac{G_C\,G_X\,G_P}{1 + G_C\,G_X\,G_P - (j\omega_e L_\sigma)G_X\,G_P}. \qquad (12)$$

In order to simplify the analysis, a simple R–L load was assumed and the back-EMF term and feedforward term were omitted. In many motor drive applications, these terms are not critical for the current controller because these are relatively slowly varying terms composed of the flux and mechanical speed of the machine. Table II shows the parameters used for the analysis, which are equivalent to the parameters of the PMSM shown in Table I. Fig. 8(a) shows the complex root locus of the transfer function in (12), with the variation in the synchronous frequency from 10 to 200 Hz. In Fig. 8(a), it can be seen that with a constant sampling time and with a fixed current regulation bandwidth, the pole of the system moves to the right half plane of the s domain with the increase in the output frequency. In this situation, the transition to the unstable region occurs at 120 Hz. In the case of the complex root locus with proposed compensation method in Fig. 8(b), the poles of the system always remain in the stable region. The instability in Fig. 8(a) is mainly caused by cross coupling between the d- and q-axes variables. This is prominent in the scalar representation in Fig. 9, where θ_D represents the rotation of the reference frame during the delay time. The thick lines show the cross couplings caused by the error of the phase in the voltage output. These cross-coupling terms also cause an oscillatory response, which deteriorates the dynamic response of the current regulator.



(a)



(b)

Fig. 8. Complex vector root locus of the current regulator according to the increase in the excitation frequency. (a) Without compensation, (b) With the proposed compensation.

VII. SIMULATION 2

A computer simulation was carried out by using MATLAB/Simulink in order to investigate the effectiveness of the proposed compensation method and to confirm the result of the root locus analysis. The motor and control parameters are shown in Table I. The motor was accelerated with the rated output current up to the rated speed in order to check the stability at the high excitation frequency. In addition, the current reference was changed rapidly at 1500 r/min in

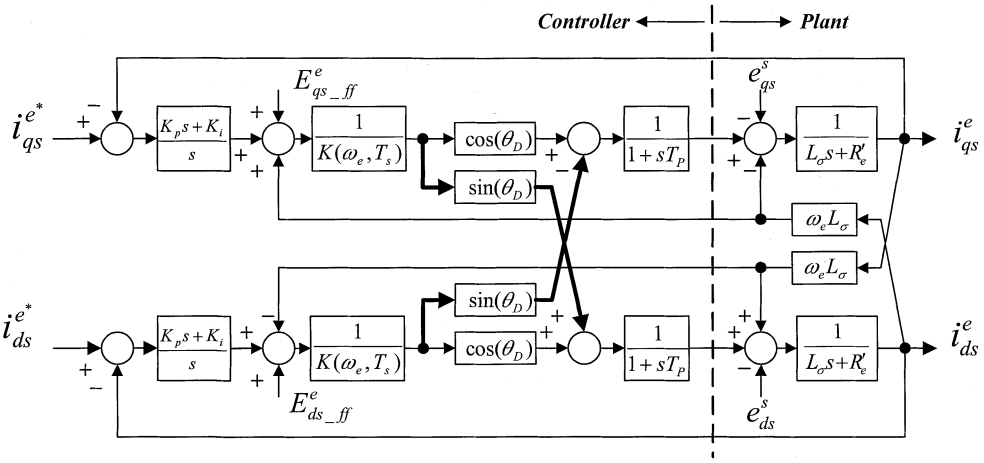


Fig. 9. Block diagram of the synchronous current regulator without the proposed compensation.

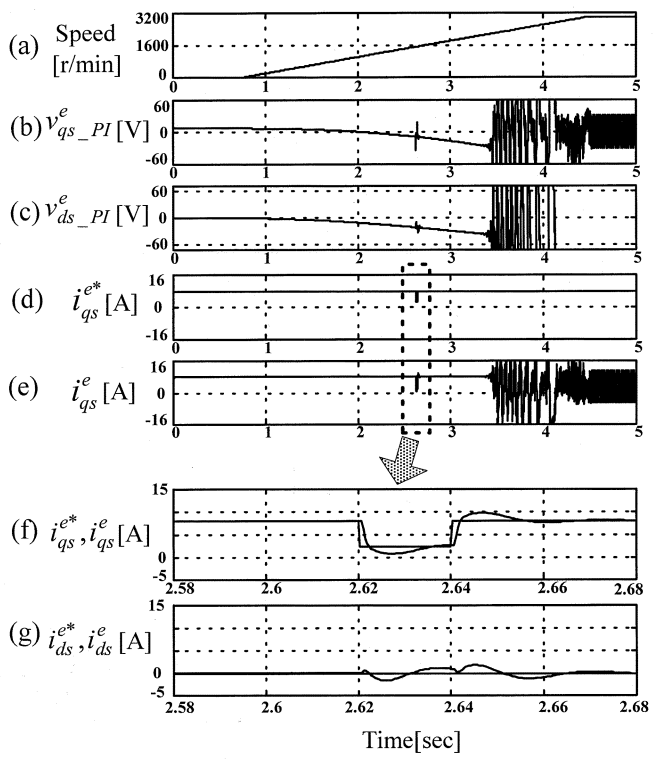


Fig. 10. Simulation result without the proposed compensation. (a) Speed. (b) Output of q-axis PI regulator. (c) Output of d-axis PI regulator. (d) q-axis current reference. (e) q-axis current. (f) Magnified q-axis current reference and measured value. (g) Magnified d-axis current reference and measured value.

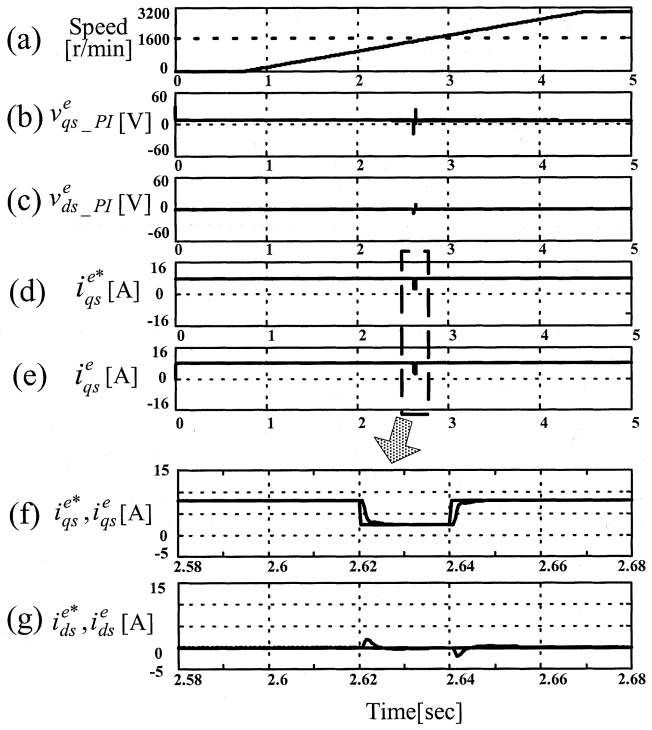


Fig. 11. Simulation result with the proposed compensation. (a) Speed. (b) Output of q-axis PI regulator. (c) Output of d-axis PI regulator. (d) q-axis current reference. (e) q-axis current. (f) Magnified q-axis current reference and measured value. (g) Magnified d-axis current reference and measured value.

order to compare the dynamic characteristics of the two cases with and without the proposed compensation. The simulation results without the proposed compensation are shown in Fig. 10. As shown in the q-axis current waveform in Fig. 10(e), the regulator loses control at a speed of 2100 r/min, which corresponds to an excitation frequency of 130 Hz. This simulation result is similar to the result of the root locus analysis, which shows the instability at 120 Hz. The effects that were not considered in the root locus analysis, e.g., PWM effect and discrete sampling, cause this deviation. Fig. 11 shows the simulation result with the proposed compensation method. The results show that the current is controlled effectively at 3000 r/min despite the low switching frequency by the proposed control. At a speed of 3000 r/min, a one-and-a-half of sampling time delay correspond to 43° in the electric angle.

The responses to a step change in the q-axis current command are marked by the dotted-line squares, which were magnified in Figs. 10(f) and (g) and 11(f) and (g), in order to simplify the comparison. Compared to the magnified response of the proposed control, the magnified response without compensation in Fig. 10 shows more oscillation and overshoot due to the effect of cross coupling. The simulation results show that the proposed

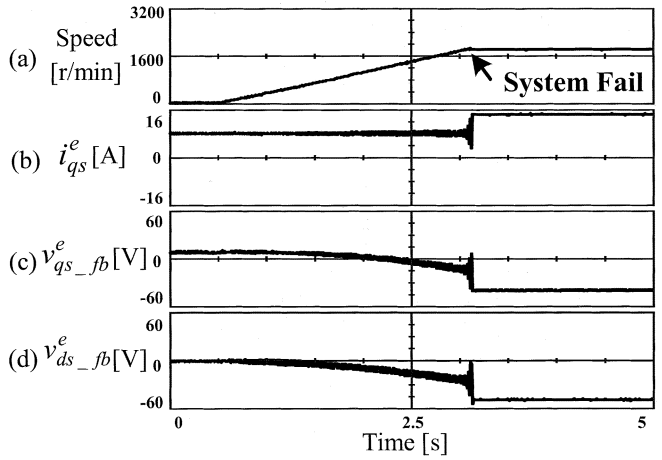


Fig. 12. Experimental result without the proposed compensation (acceleration test up to the rated speed). (a) Speed. (b) q-axis current. (c) Output of q-axis PI regulator. (d) Output of d-axis PI regulator.

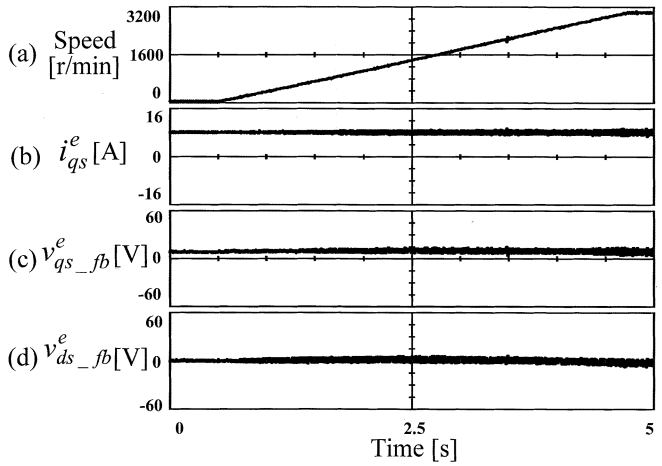


Fig. 13. Experimental result with the proposed compensation (acceleration test up to the rated speed). (a) Speed. (b) q-axis current. (c) Output of q-axis PI regulator. (d) Output of d-axis PI regulator.

compensation method improves the stability and dynamic performance of the synchronous current regulator.

VIII. Experimental Results

Experiments were carried out in order to verify the validity of the proposed control. A 1.25-kHz IGBT inverter-fed 1-kW PMSM, whose parameters are shown in Table I, was used for the test. The synchronous frame current regulator was fully implemented in the software using a digital signal processor (DSP) TMS320VC33. The detailed parameters of the control are shown in Table I. The inverter was fed by a dc-link voltage of 310 V_{dc} and the SVPWM with a dead time of 3 μs was implemented using a programmable logic device. As a load machine, a 1.5-kW PMSM, which was driven by a 1.5-kW servo drive, was directly coupled to the shaft of the 1-kW PMSM. Figs. 12 and 13 show the results of the acceleration test up to the rated speed with a sampling time of 400 μs. In these experiments, the references for the d and q-axes current regulator were set to 0 and 8 A, respectively. In addition, the motor was accelerated from 0 to 3000 r/min using the 1.5-kW

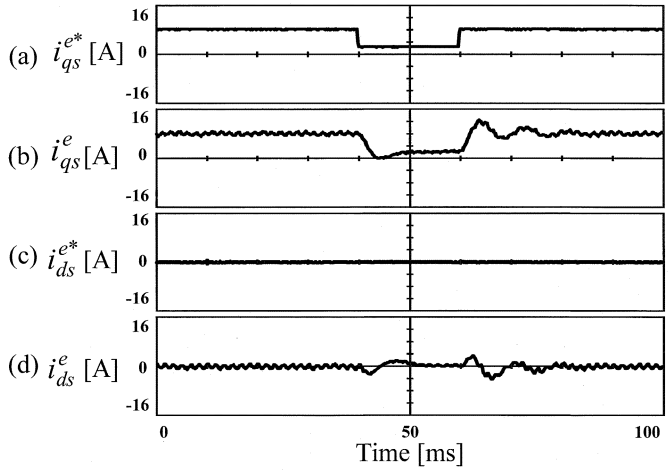


Fig. 14. Experimental result without the proposed compensation (step response of the current regulator at 1500 r/min). (a) q-axis current reference. (b) q-axis current measured. (c) d-axis current reference. (d) d-axis current measured.

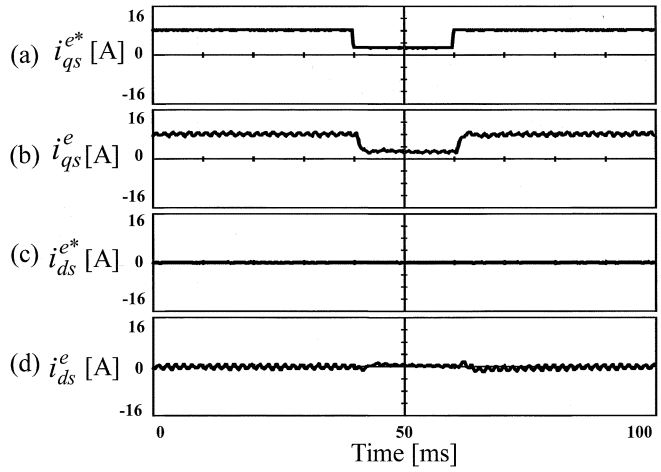


Fig. 15. Experimental result with the proposed compensation (step response of the current regulator at 1500 r/min). (a) q-axis current reference. (b) q-axis current measured. (c) d-axis current reference. (d) d-axis current measured.

load machine. Fig. 12 shows the results of the acceleration test without the proposed compensation. The output voltages of the d and q-axes PI regulator deviate from the constant values according to the increase in speed, and these deviations correspond to the results of the simulation 1 in Fig. 6. At 1850 r/min, the synchronous frame current regulator becomes unstable due to the errors caused by the rotation of the reference frame during the time delay. This speed corresponds to an electric frequency of 123 Hz, and matches well with the results of the root locus analysis and computer simulations. The result of the acceleration test with the proposed compensation is shown in Fig. 13. In contrast to the results shown in Fig. 12. The output voltages of the d- and q-axes PI regulator are constant regardless of the increase in speed and the current is well regulated up to a rated speed of 3000 r/min, where the ratio between the switching frequency and the output frequency is 12.5. Figs. 14 and 15 show the step response of the synchronous current regulator with and without the proposed compensation at 1,500 r/min. The q-axis current reference was changed

TABLE III
PARAMETERS OF SUPER-HIGH-SPEED PMSM AND SPECIFICATIONS OF CONTROL

Motor Parameters	
Rated output	131 kW
Number of Poles	2
Rated speed	70,000 r/min
Rated voltage	360 V_{rms}
Rated torque	17.9 Nm
Rated current	237 A_{rms}
Stator resistor, R_s	0.0055 Ω
Stator inductance, L_s	28 μH
Control Parameters	
Sampling time	33.33μs
Switching frequency	15 kHz

from the rated value to 30% of the rated value and back to the rated value at 1500 r/min. The current waveform without the compensation is shown in Fig. 14. The measured q-axis current of Fig. 14(b) shows a relatively large overshoot and a sluggish response due to cross coupling caused by the angle error in the voltage output. Fig. 15 shows the current waveform of the step response with the proposed control. This result shows no overshoot and rapid current control dynamics. These results show that the proposed compensation improves the stability and dynamics of the synchronous frame current regulator.

Furthermore, more experiments were carried out using a super-high-speed PMSM for a turbo-compressor in order to verify the feasibility of the proposed control on the high-speed high-switching-frequency system. The parameters of the PMSM and the brief specifications of control are shown in Table III. The IGBT inverter was fed by a dc-link voltage of 620 V_{dc} and the swiching frequency for the SVPWM was set as high as 15 kHz in oder to generate the 1.2-kHz output voltage. The air was compressed by the two impellers, whch were mounted at the ends of the rotor, and the load was controlled by adusting the damper of the compressor system. As a position sensor was not reliable at the super-high speed, a sensorless vector control was implemented using the voltage model of the machine [11]. In the case of the voltage-model-based sensorless control, the phase and magnitude error in the voltage output causes an error in the estimated angle. In order to compensate the error in the ouput voltage, the proposed compensation method was implemented using the DSP TMS320VC33. The proposed compensation, given by (11), was easily implemented using some arithmetic including three trigonometric functions, which took no more than a few microseconds using the DSP. In this application, the ratio of the sampling frequency to the output frequency is 30 at the rated speed. This ratio is not small enough to cause an instability problem in the current regulator but it can cause a significant angle error in the voltage-model-based sensorless control strategy.

Fig. 16 shows the experimental results using the super-high-speed PMSM. The motor speed was regulated at 50 000 r/min and the load of the compressor system was maintained constant by controling the damper. The experimental results compares the control characteristics with and without the proposed

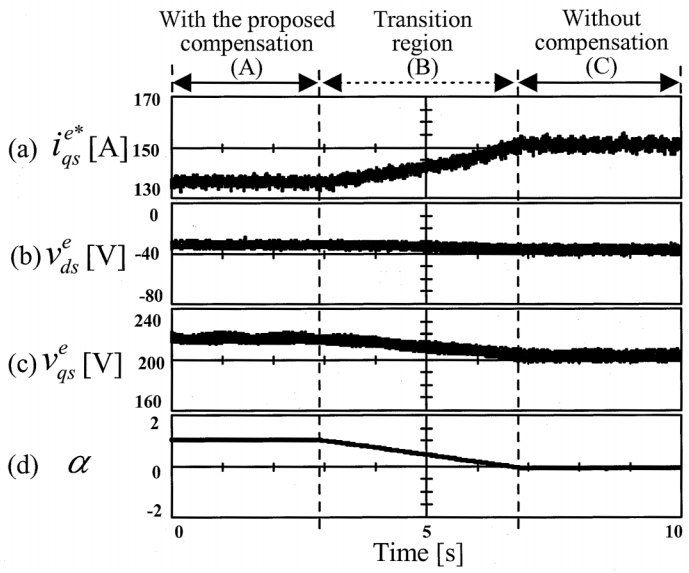


Fig. 16. Experimental result using the super-high-speed PMSM. (a) q-axis current. (b) d-axis voltage reference. (c) q-axis voltage reference. (d) Weighting function for the proposed compensation.

control. In region (A), in Fig. 16, the proposed compensation was activated and the compressor system was operating with the minimum q-axis current. In the region (B), the weighting function for the compensation α was decreasing to zero and the compensation was reduced according to the following:

$$f_c = \{\alpha K(\omega_e, T_s) + (1-\alpha)\} \cdot e^{j(1.5\alpha T_s \omega_e)}. \quad (13)$$

In region (C), the compensation was disabled and the motor was operating without compensation. Considering the sampling time and the motor speed, the phase error in the output voltage corresponds to a delay by 15°. In addition, the voltage reference, which is the output voltage of the current regulator, leads the real output voltage by 15° and it causes a similar phase lead in the estimated angle of the sensorless control. The experimental results without compensation show that the q-axis current reference was increased about 5% by the angle error and the q-axis output voltage was decreased by the negative d-axis current component which was generated by the leading angle error.

The experimental results at the super-high speed show that the proposed compensation is feasible on the high-speed high-switching-frequency system using some arithmetic and trigonometry. In addition, it is shown that the proposed compensation is effective in the voltage-model-based sensorless strategy.

IX. CONCLUSION

In this paper, the effects of a time delay in a modern digital synchronous frame current regulator were investigated. The study focused on the errors in the voltage output caused by the rotation of the synchronous reference frame during the time delay, and an effective compensation method was proposed. The computer simulation was used to carry out comparative studies with the conventional method, and it was demonstrated that the

proposed compensation method improves the stability and dynamic performance of the current regulator. A stability study has been carried out using the complex vector root locus. The results show that the conventional synchronous current regulator can lose stability in the case where the ratio of the sampling frequency to the excitation frequency is insufficient, and the proposed compensation method is effective in stabilizing the system. Furthermore, experiments on the synchronous frame current regulator with the proposed compensation were carried out. The experimental results prove that the proposed control method improves the stability and dynamics of a synchronous current regulator by compensating for the voltage errors due to the rotation of the reference frame during the time delay.

REFERENCES

[1] T. R. Rowan and R. L. Kerkman, "A new synchronous current regulator and an analysis of current-regulated PWM inverter," *IEEE Trans. Ind. Applicat.*, vol. IA-22, pp. 678–690, July/Aug. 1986.

[2] D. W. Novotony and T. A. Lipo, *Vector Control and Dynamics of AC Drives*. New York: Oxford Univ. Press, 1996.

[3] J. Holtz and B. Beyer, "Fast current trajectory tracking control based on synchronous optimal pulsewidth modulation," *IEEE Trans. Ind. Applicat.*, vol. 31, pp. 1110–1120, Sept./Oct. 1995.

[4] V. Blasko, V. Kaura, and W. Niewiadomski, "Sampling of discontinuous voltage and current signals in electrical drives: A system approach," *IEEE Trans. Ind. Applicat.*, vol. 34, pp. 1123–1130, Sept./Oct. 1998.

[5] W. L. Roux and J. D. van Wyk, "The effect of signal measurement and processign delay on the compensation of harmonics by PWM converter," *IEEE Trans. Ind. Electron.*, vol. 47, pp. 297–304, Apr. 2000.

[6] S. H. Song, J. W. Choi, and S. K. Sul, "Current measurement in digitally controlled AD drives," *IEEE Ind. Applicat. Mag.*, vol. 6, pp. 51–62, Jul./Aug. 2000.

[7] P. Mattavelli and F. Fasolo, "A closed-loop selective harmonic compensation for active filters," in *Conf. Rec. IEEE APEC'96*, 1996, pp. 399–405.

[8] S. J. Lee and S. K. Sul, "Harmonic reference frame based current controller for active filter," in *Conf. Rec. IEEE APEC*, 2000, pp. 1073–1080.

[9] F. Briz, M. W. Degner, and R. D. Lorenz, "Analysis and design of current regulators using complex vector," *IEEE Trans. Ind. Applicat.*, vol. 36, pp. 817–825, May/June 2000.

[10] Y. Yamamoto, T. Kodama, T. Yamada, T. Ihioka, and T. Niwa, "Digital current control method of induction motor using synchronous current detection with PWM signals" (in Japanese), *Trans. Inst. Elect. Eng. Jpn.*, vol. 112-D, no. 7, pp. 613–622, 1992.

[11] B.-H. Bae, S.-K. Sul, J.-H. Kwon, and J.-S. Shin, "Implementation of sensorless vector control for super-high speed PMSM of turbo-compressor," in *Conf. Rec. IEEE-IAS Annu. Meeting*, 2001, pp. 1203–1209.

Bon-Ho Bae (S'99–M'03) was born in Korea in 1966. He received the Ph.D. degree in electrical engineering from Seoul National University, Seoul, Korea, in 2002.

He joined Rotem Company (formerly Daewoo Heavy Industries Ltd.) in 1992 and worked for eight years on the development of propulsion systems for electric trains. His recent research projects were the development of the 1.2-MVA IGBT inverter for the traction system of a subway train, sensorless vector drive system with 130-kW 70 000-r/min PMSM for turbo-compressor, and the 42-V ISG system using the high-saliency-ratio IPMSM. He is currently with the General Motors Corporation Advanced Technology Center, Torrance, CA, and his research interests are electric machine drives and automotive applications.

Seung-Ki Sul (S'78–M'87–SM'98–F'00) was born in Korea in 1958. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 1980, 1983, and 1986, respectively.

From 1986 to 1988, he was an Associate Researcher with the Department of Electrical and Computer Engineering, University of Wisconsin, Madison. He then was with Gold-Star Industrial Systems Company as a Principal Research Engineer from 1988 to 1990. Since 1991, he has been a member of the faculty of the School of Electrical Engineering, Seoul National University, where he is currently a Professor. His current research interests are power electronic control of electric machines, electric vehicle drives, and power converter circuits.