Inverter Output Voltage Synthesis Using Novel Dead Time Compensation

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Abstract— **In this paper, a novel dead time compensation method is presented that produces inverter output voltages equal to reference voltages. An experimental result is also presented to demonstrate the validity of the proposed method. It shows that the compensation of the dead time is possible up to a sub-microsecond range. Also, the reference voltage can be used as a feedback value, which is essential for sensorless vector control and flux estimation. The method is based on space vector pulsewidth modulation (PWM) strategy and it can be carried out automatically by an inverter controller for initial setup without any extra hardware.**

I. Introduction

VOLTAGE-FED pulsewidth modulation (PWM) inverters have gained increasing popularity in industrial applications. In their application areas, the ac machine drive is one of the most important parts. By the development of fast-switching power devices such as power transistors and insulated gate bipolar transistors (IGBT's), a high-performance ac machine drive with fast response, low harmonics, and low audible noise is possible. In some applications, such as sensorless vector control and flux estimation, the inverter output voltages are needed to calculate desired state values. It is very difficult, however, to measure the output voltages because they are composed of discrete pulses. In other words, to measure inverter output voltages, the output voltages should be isolated and the high-frequency components in output voltages should be removed by a low-pass filter. Thus, due to the low-pass filter, the filtered output voltages suffer from phase delay and are not adequate for use in control purposes. Another method to obtain the output voltage is to use the reference voltages as the output voltage. Compared to the reference voltage, however, the inverter output voltages are much distorted because of the output voltage distortion.

In voltage-fed PWM inverter, there are several causes to distort output voltage. Some is caused by the dead time that is inevitable to prevent the shoot-through phenomenon. Others originate from the inherent characteristics of the switching devices such as the voltage drop, the output voltage transition slope, and the turn on/off time. Recently, remarkable efforts have been made to compensate for the voltage distortion by the dead time [1]–[8], but a few papers have mentioned the voltage distortion caused by the nonideal characteristic of the switching device such as turn on/off time [6], [7], voltage transition slope [8], and voltage drop effect [6], [7].

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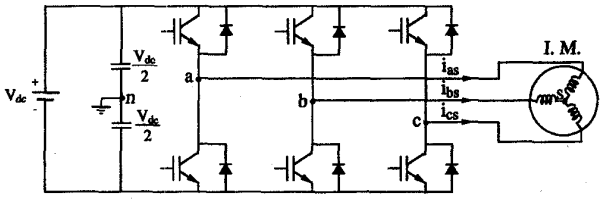

Fig. 1. Three-phase PWM inverter with an induction motor load.

To accurately compensate these effects, the turn on/off time, voltage transition slope, and the on-state voltage drop of the switching device should be known, and these are not exactly measurable and are dependent on the operating point. Thus, in these papers [6], [7], the knowledge of the switching device characteristics is assumed. As a result, the accurate output voltage compensation is not guaranteed.

In this paper, the analysis of the voltage distortion is discussed with consideration of the dead time effect and voltage drop of the power devices. For analysis of the voltage distortion, turn on/off delay time, voltage transition slope, and voltage drops of the power devices are also considered. From this discussion, a novel dead time compensation method is presented that produces inverter output voltages equal to the reference voltages. In this method, the optimal compensation time can be found without knowing the characteristics of the switching device. By this method, the reference voltages can be used as inverter output voltage because the proposed method accurately compensates the voltage distortion due to the dead time and device voltage drop. By applying this method to the general purpose PWM inverter system, a more accurate output voltage can be obtained without any extra hardware to compensate dead time effect. In addition, the proposed strategy is suitable for applying space vector PWM, which synthesizes accurate output voltage [9]. The method can also be used to determine stator resistance, including power device ohmic drop, which is essential in the voltage model flux estimation. Experimental results are also presented to demonstrate the validity of the proposed method.

II. Analysis of Dead Time Effect

The commonly used three-phase PWM inverter with an induction motor load is shown in Fig. 1. The typical gating pulse pattern of the space vector PWM is shown in Fig. 2.

During the dead time (T_d), both the power devices in the same leg cease to conduct and one of the diodes conduct. If the current flows to load, the lower diode will conduct. Otherwise,

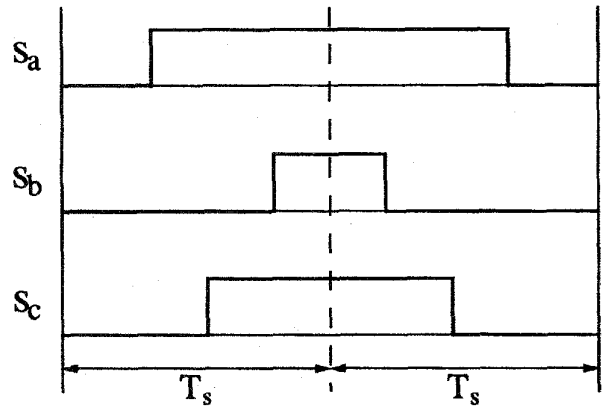

Fig. 2. Typical gating pulse pattern of the space vector PWM.

the upper diode will conduct. From this concept, the novel dead time compensation method may be illustrated as follows. For easy explanation, it is assumed that the current (i_{as}) flows to load, that is, the current flows in the positive direction.

Fig. 3(a) shows the ideal gating pulse pattern and Fig. 3(b) shows the proposed dead time compensation strategy. When the upper power device is scheduled to turn on at T_1, A^- gating pulse is first off at $T_1 - T_{\rm com}$ and A^+ gating pulse is on at $T_1 - T_{\rm com} + T_d$. When the lower power device is scheduled to turn off at T_2, A^+, gating pulse is off at T_2 and A^- gating pulse is off at $T_2 + T_d$. In both cases, the dead time (T_d) is guaranteed. The actual phase to center voltage with consideration of turn on/off time delay and voltage transition slope of the power devices is shown in Fig. 3(c). The equivalent phase to center voltage can be depicted as Fig. 3(d), where the voltage slope is considered as turn on/off time delay. In Fig. 3(d), the turn-on time means the time delay from the turn-on of the switch control signal to the effective turn-on of the power device. It includes the signal delay time of the gating circuit and the turn-on delay time of the power device. The turn-off time is defined in a similar way. From Fig. 3(a), the upper power device is designed to turn-on for $T_2 - T_1$. From Fig. 3(d), however, effective turn-on duration of the upper power device is $T_2 - T_1 + T_{\rm off} - T_{\rm on} - T_d + T_{\rm com}$. So, the time error resulting from dead time is given by

$$T_{\rm err} = T_{\rm off} - T_{\rm on} - T_d + T_{\rm com}. \tag{1}$$

When i_{as} is negative, the proposed dead time compensation strategy is shown in Fig. 3(e)~(g). A similar analysis can be performed and the time error is given by

$$T_{\rm err} = -(T_{\rm off} - T_{\rm on} - T_d + T_{\rm com}). \tag{2}$$

So, time error can be represented as follows:

$$T_{\rm err} = {\rm sign}(i_{as})(T_{\rm off} - T_{\rm on} - T_d + T_{\rm com}) \tag{3}$$

where

$${\rm sign}(i_{as}) = \begin{bmatrix} 1\text{: when } i_{as} > 0 \\ -1\text{: when } i_{as} < 0 \end{bmatrix}. \tag{4}$$

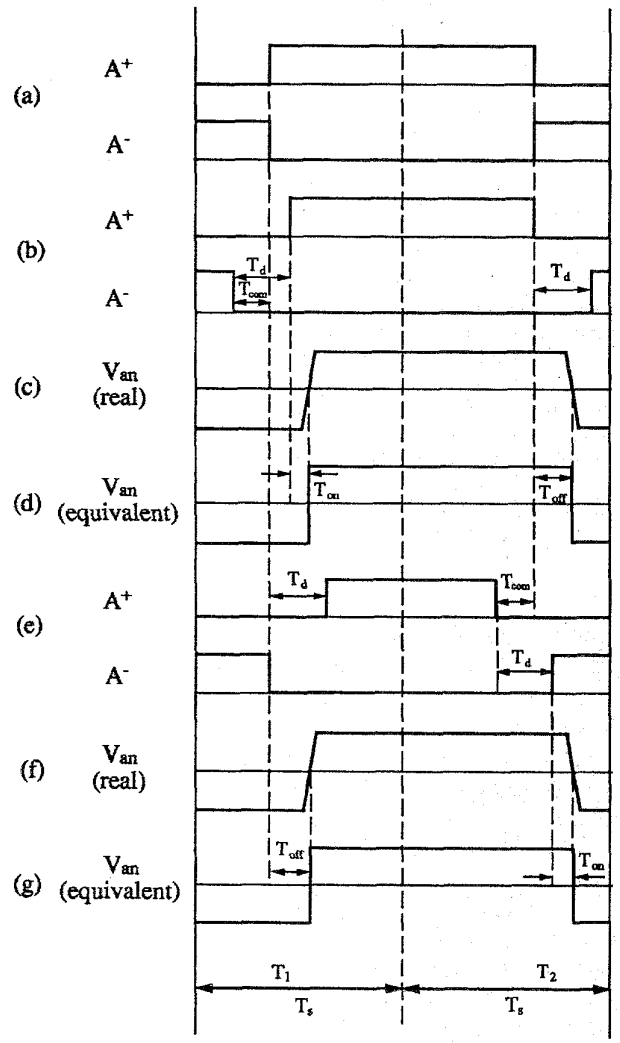

Fig. 3. Dead-time compensation strategy. (a) Ideal gating pulse pattern. (b) Gating pulse pattern with dead time ($i_{as} > 0$) (c) actual phase to center voltage ($i_{as} > 0$). (d) Equivalent phase to center voltage ($i_{as} > 0$) (e) gating pulse pattern with dead time ($i_{as} < 0$). (f) Actual phase to center voltage ($i_{as} < 0$). (g) Equivalent phase to center voltage ($i_{as} < 0$).

The effective time duration is the summation of the commanded time duration and time error and is given by

$$T_a = T_a^* + {\rm sign}(i_{as})M \tag{5}$$

where

$$M = T_{\rm off} - T_{\rm on} - T_d + T_{\rm com}.$$

If the same analysis is performed for the other phases, the times of the other two phases are as follows:

$$T_b = T_b^* + {\rm sign}(i_{bs})M \tag{6}$$

$$T_c = T_c^* + {\rm sign}(i_{cs})M. \tag{7}$$

From (5)–(7), it is seen that effective time durations differ from commanded time duration due to the compensation time and uncertain values such as turn-on and turn-off delay. Note that the compensation time $T_{\rm com}$ is controllable and the time M is also controllable.

III. Voltage Distortion Analysis and Compensation Strategy

In PWM inverter system, in addition to dead time effect there exist the voltage drops of the power devices that distort the output voltage. If the current (i_{as}) flows to load, the actual phase to center voltage is

$$v_{an} = \frac{V_{dc}}{2} - V_{ce} \quad (\text{when } S_a = 1) \tag{8}$$

$$v_{an} = -\frac{V_{dc}}{2} - V_d \quad (\text{when } S_a = 0) \tag{9}$$

where

V_{ce} voltage drop of the active switch

V_d voltage drop of freewheeling diode

S_a 1 (upper switch is on), 0 (lower switch is on).

When the current (i_{as}) flows from load, the actual phase to center voltage is varied as

$$v_{an} = \frac{V_{dc}}{2} + V_d \quad (\text{when } S_a = 1) \tag{10}$$

$$v_{an} = -\frac{V_{dc}}{2} + V_{ce} \quad (\text{when } S_a = 0). \tag{11}$$

So, the actual phase to center voltage by considering the voltage drop of the power devices varies with switching state and current direction, and it can be written in the form assuming that the current direction does not change for a sampling period, which is reasonable in high-frequency switching

$$v_{an} = (V_{dc} - V_{ce} + V_d)\left(S_a - \frac{1}{2}\right) - \frac{1}{2}\text{sign}(i_{as})(V_{ce} + V_d). \tag{12}$$

Generally, the voltage drops of the active switch and freewheeling diode increase with current. Thus, it may be assumed that the voltage drops of the active switch and of the freewheeling diode linearly increases with current at the normal operating region and can be modeled as follows:

$$V_{ce} = V_{ce0} + r_{ce}|i_{as}| \tag{13}$$

where

V_{ce0} threshold voltage of the active switch

r_{ce} on-state slope resistance of the active switch

$$V_d = V_{d0} + r_d|i_{as}| \tag{14}$$

where

V_{d0} threshold voltage of the freewheeling diode

r_d on-state slope resistance of the freewheeling diode

thus

$$v_{an} = (V_{dc} - V_{ce} + V_d)\left(S_a - \frac{1}{2}\right) - \frac{1}{2}\text{sign}(i_{as})(V_{ce0} + V_{d0}) - \frac{1}{2}(r_{ce} + r_d)i_{as}. \tag{15}$$

The mean phase to center voltage during two sampling periods can be represented by

$$V_{an} = (V_{dc} - V_{ce} + V_d)\left(\frac{T_a}{2T_s} - \frac{1}{2}\right) - \frac{1}{2}\text{sign}(i_{as})(V_{ce0} + V_{d0}) - \frac{1}{2}(r_{ce} + r_d)i_{as} \tag{16}$$

where T_s represents sampling period.

Similarly, the mean phase to center voltages are easily obtained

$$V_{bn} = (V_{dc} - V_{ce} + V_d)\left(\frac{T_b}{2T_s} - \frac{1}{2}\right) - \frac{1}{2}\text{sign}(i_{bs})(V_{ce0} + V_{d0}) - \frac{1}{2}(r_{ce} + r_d)i_{bs} \tag{17}$$

$$V_{cn} = (V_{dc} - V_{ce} + V_d)\left(\frac{T_c}{2T_s} - \frac{1}{2}\right) - \frac{1}{2}\text{sign}(i_{cs})(V_{ce0} + V_{d0}) - \frac{1}{2}(r_{ce} + r_d)i_{cs}. \tag{18}$$

Now, consider the following equations:

$$V_{an} = V_{as} + V_{sn} \tag{19}$$

$$V_{bn} = V_{bs} + V_{sn} \tag{20}$$

$$V_{cn} = V_{cs} + V_{sn}. \tag{21}$$

The absence of a neutral connection in the motor forces the constraint that

$$i_{as} + i_{bs} + i_{cs} = 0. \tag{22}$$

For any balanced load, the line to neutral voltages are constrained such that

$$V_{as} + V_{bs} + V_{cs} = 0. \tag{23}$$

These give

$$V_{sn} = \frac{1}{3}(V_{an} + V_{bn} + V_{cn}) = \frac{1}{3}(V_{dc} - V_{ce} + V_d)\left(\frac{T_a + T_b + T_c}{2T_s} - \frac{3}{2}\right) - \frac{1}{6}(V_{ce0} + V_{d0})\{\text{sign}(i_{as}) + \text{sign}(i_{bs}) + \text{sign}(i_{cs})\}. \tag{24}$$

Equations (16)–(24) lead to the following expressions for line to neutral voltages

$$V_{as} = V_{an} - V_{sn} = \frac{1}{3}(V_{dc} - V_{ce} + V_d)\frac{2T_a - T_b - T_c}{2T_s} - \frac{1}{6}(V_{ce0} + V_{d0})\{2\text{sign}(i_{as}) - \text{sign}(i_{bs}) - \text{sign}(i_{cs})\} - \frac{1}{2}(r_{ce} + r_d)i_{as} \tag{25}$$

$$V_{bs} = V_{bn} - V_{sn} = \frac{1}{3}(V_{dc} - V_{ce} + V_d)\frac{2T_b - T_c - T_a}{2T_s}$$

$$-\frac{1}{6}(V_{ce0}+V_{d0})\{2\text{sign}(i_{bs})-\text{sign}(i_{cs})-\text{sign}(i_{as})\}$$
$$-\frac{1}{2}(r_{ce}+r_d)i_{bs} \tag{26}$$

$$V_{cs}=V_{cn}-V_{sn}$$
$$=\frac{1}{3}(V_{dc}-V_{ce}+V_d)\frac{2T_c-T_a-T_b}{2T_s}$$
$$-\frac{1}{6}(V_{ce0}+V_{d0})\{2\text{sign}(i_{cs})-\text{sign}(i_{as})-\text{sign}(i_{bs})\}$$
$$-\frac{1}{2}(r_{ce}+r_d)i_{cs} \tag{27}$$

which become, with the aid of (5)–(7)

$$V_{as}=V_{as}^*+V_{as}'-\frac{1}{2}(r_{ce}+r_d)i_{as} \tag{28}$$

where

$$V_{as}^*=\frac{1}{3}(V_{dc}-V_{ce}+V_d)\frac{2T_a^*-T_b^*-T_c^*}{2T_s}$$
$$\approx\frac{1}{3}V_{dc}\frac{2T_a^*-T_b^*-T_c^*}{2T_s}$$
$$V_{as}'=V'\{2\text{sign}(i_{as})-\text{sign}(i_{bs})-\text{sign}(i_{cs})\}$$
$$V_{bs}=V_{bs}^*+V_{bs}'-\frac{1}{2}(r_{ce}+r_d)i_{bs} \tag{29}$$

where

$$V_{bs}^*\approx\frac{1}{3}V_{dc}\frac{2T_b^*-T_c^*-T_a^*}{2T_s}$$
$$V_{bs}'=V'\{2\text{sign}(i_{bs})-\text{sign}(i_{cs})-\text{sign}(i_{as})\}$$
$$V_{cs}=V_{cs}^*+V_{cs}'-\frac{1}{2}(r_{ce}+r_d)i_{cs} \tag{30}$$

where

$$V_{cs}^*\approx\frac{1}{3}V_{dc}\frac{2T_c^*-T_a^*-T_b^*}{2T_s}$$
$$V_{cs}'=V'\{2\text{sign}(i_{cs})-\text{sign}(i_{as})-\text{sign}(i_{bs})\}$$

$$V'=\frac{1}{6}\left\{(V_{dc}-V_{ce}+V_d)\frac{M}{T_s}-V_{ce0}-V_{d0}\right\}$$
$$\approx\frac{1}{6}\left\{V_{dc}\frac{M}{T_s}-V_{ce0}-V_{d0}\right\}. \tag{31}$$

"*" denotes the reference voltage and "′" denotes the distorted voltage. In (28)–(31), the term $V_{ce}-V_d$ is neglected because V_{dc} is much greater than $V_{ce}-V_d$. Though the turn-on and turn-off time also increases with current, the term $T_{\text{off}}-T_{\text{on}}$ may be considered to be a constant. Thus the term M is also regarded as a constant value.

Equations (28)–(31) lead to two considerable conclusions about compensation of dead time effect and voltage drop of the power devices. First, the term $\frac{1}{2}(r_{ce}+r_d)$ acts as a stator resistor. Therefore, in the case of the induction machine, the stator resistance should be the sum of real machine stator resistance r_s and the term $\frac{1}{2}(r_{ce}+r_d)$. The equivalent stator resistance is defined as the sum of the real stator resistance and the ohmic drop of power devices

$$r_s'=r_s+\frac{1}{2}(r_{ce}+r_d). \tag{32}$$

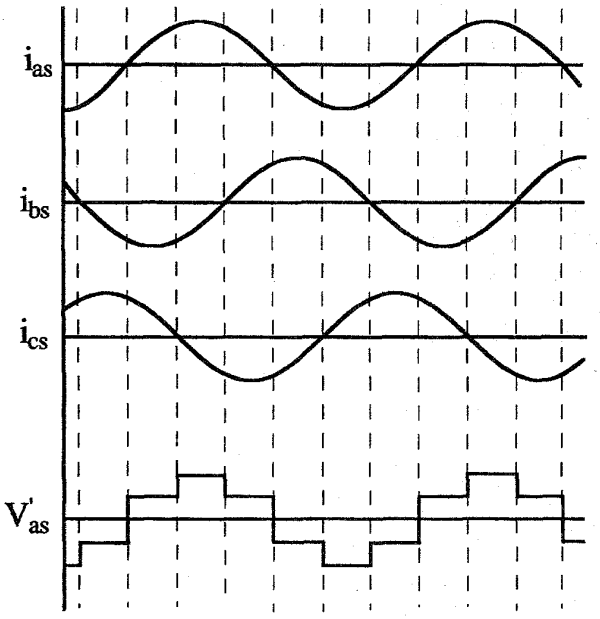

Fig. 4. Waveform of phase distorted voltage.

Second, the phase distorted voltage has the six-step waveform which has the peak of $\frac{2}{3}(V_{dc}\frac{M}{T_s}-V_{ce0}-V_{d0})$ and is the same phase with the phase current. This is depicted in Fig. 4.

To remove the distorted voltage, the peak of the distorted voltage must be zero, that is, from (31)

$$T_{\text{com}}=T_d-T_{\text{off}}+T_{\text{on}}+T_s\frac{V_{ce0}+V_{d0}}{V_{dc}}. \tag{33}$$

The accurate distortion voltage compensation is not to minimize the time M but to adjust the time M to compensate the voltage drop effect of the power devices. In this scheme, by adjusting the compensation time T_{com}, the distorted voltage can be removed.

IV. Strategy of Adjusting Compensation Time

Equation (33) contains many uncertain values such as turn-on time delay (T_{on}), turn-off time delay (T_{off}), voltage drops of the switch (V_{ce0}), and voltage drop of the freewheeling diode (V_{d0}). But these uncertain values are not exactly measurable and depend on the operating region. In addition, the difference between turn-off time and turn-on time is large and hundreds nsec order in case of IGBT. By considering high-frequency switching of IGBT inverters, the difference has considerable effect to the voltage synthesis. And the voltage drops also play an important part in distorting output voltages, which give more significant effect in the case of high-power switches.

Now, the method for searching T_{com} is illustrated. The current control loop with distorted voltage is shown in Fig. 5. In Fig. 5, the shaded area may be replaced by the system with increased resistance by $\frac{1}{2}(r_{ce}+r_d)$. In the case of the induction machine, it can be interpreted that the term $\frac{1}{2}(r_{ce}+r_d)$ due to the voltage drop effect is added to the stator resistance.

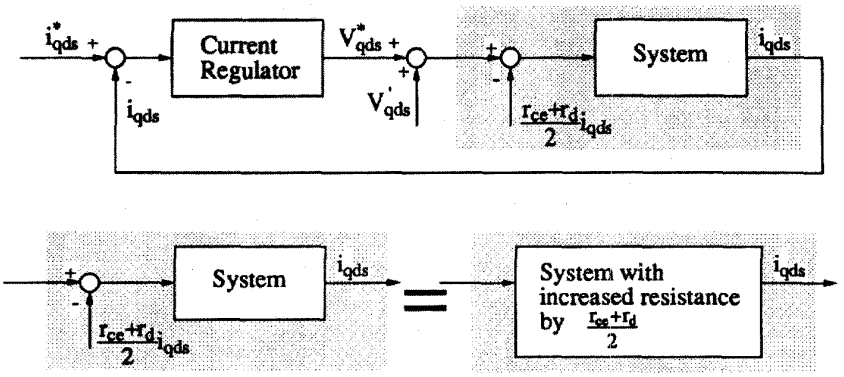

Fig. 5. Current control loop with distorted voltage.

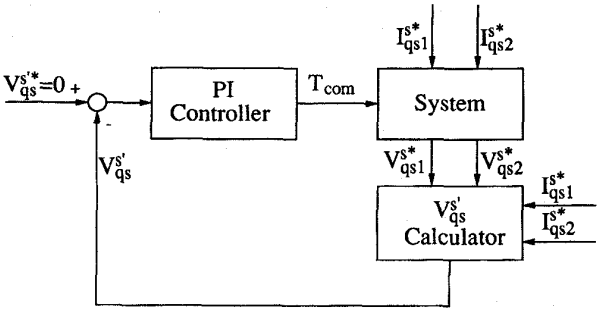

Fig. 6. Strategy of adjusting compensation time.

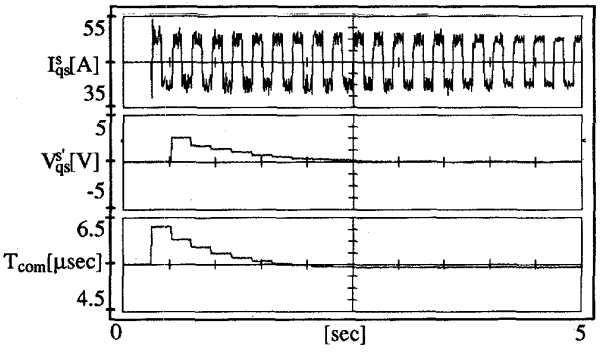

Fig. 7. Process of proposed strategy.

The main concept is that if the currents are well regulated, the reference voltages are distorted to compensate for the dead time and nonideal characteristics of the power device. So the distorted voltage can be detected from the reference voltage and by adjusting $T_{\rm com}$ the distorted voltage can be minimized.

If the stationary q-axis reference current $I_{qs}^{s^*}$ is positive dc value and the stationary d-axis reference current is zero, the following equations hold

$$I_{as}^* = I_{qs}^{s^*},\ I_{bs}^* = -\frac{I_{qs}^{s^*}}{2} \text{ and } I_{cs}^* = -\frac{I_{qs}^{s^*}}{2}. \tag{34}$$

If the currents are regulated, real currents flow in same direction with the reference current, thus

$$\text{sign}(I_{as}) = 1,\ \text{sign}(I_{bs}) = -1 \text{ and } \text{sign}(I_{cs}) = -1. \tag{35}$$

From (28)–(31), the distorted voltages can be derived as

$$V'_{as} = \frac{2}{3}\left(V_{dc}\frac{M}{T_s} - V_{ce0} - V_{d0}\right) \tag{36}$$

$$V'_{bs} = -\frac{1}{3}\left(V_{dc}\frac{M}{T_s} - V_{ce0} - V_{d0}\right) \tag{37}$$

$$V'_{cs} = -\frac{1}{3}\left(V_{dc}\frac{M}{T_s} - V_{ce0} - V_{d0}\right) \tag{38}$$

and

$$V_{qs}^{s'} = V'_{as} = \frac{2}{3}\left(V_{dc}\frac{M}{T_s} - V_{ce0} - V_{d0}\right) \tag{39}$$

$$V_{ds}^{s'} = \frac{V'_{cs} - V'_{bs}}{\sqrt{3}} = 0. \tag{40}$$

In this case, the voltage distortion occurs only on the q-axis. The q-axis distorted voltage can be determined by two dc tests. If the q-axis reference current is $I_{qs1}^{s^*}$, the reference voltage is distorted to compensate the distorted voltage $V_{qs}^{s'}$. Thus, in the steady state, the following equation holds

$$V_{qs1}^{s^*} = r'_s I_{qs1}^{s^*} - V_{qs}^{s'}. \tag{41}$$

In the case where the q-axis reference current is $I_{qs2}^{s^*}$, in the steady state, the following equation also holds

$$V_{qs2}^{s^*} = r'_s I_{qs2}^{s^*} - V_{qs}^{s'}. \tag{42}$$

Note the distorted voltage $V_{qs}^{s'}$ does not vary because it is related to the currents direction and two dc tests are done in the same current direction.

From (41) and (42), the q-axis distorted voltage $V_{qs}^{s'}$ and equivalent stator resistance r'_s may be calculated as

$$V_{qs}^{s'} = \frac{V_{qs1}^{s^*} I_{qs2}^{s^*} - V_{qs2}^{s^*} I_{qs1}^{s^*}}{I_{qs1}^{s^*} - I_{qs2}^{s^*}} \tag{43}$$

$$r'_s = r_s + \frac{r_{ce} + r_d}{2} = \frac{V_{qs1}^{s^*} - V_{qs2}^{s^*}}{I_{qs1}^{s^*} - I_{qs2}^{s^*}}. \tag{44}$$

The overall adjusting strategy is shown in Fig. 6. The distorted voltage obtained from (43) is the input of the PI controller and the compensation time is the output. By adjusting $T_{\rm com}$ to minimize the distorted voltage, the accurate inverter output voltages can be obtained and the reference voltages can be used as the output voltage feedback signal.

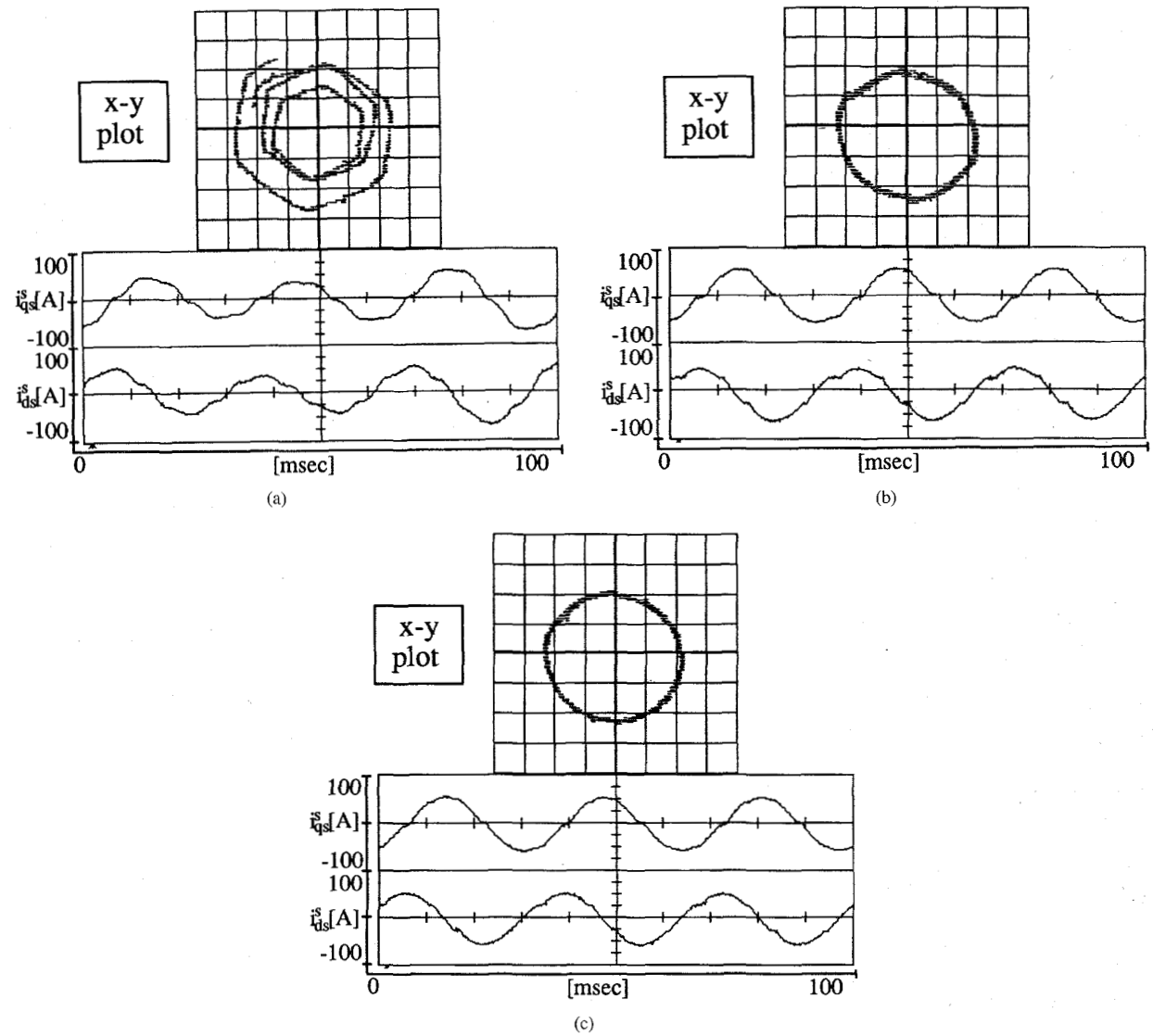

Fig. 8. Current waveforms. (a) No dead time compensation. (b) Only dead time compensation. (c) Proposed dead time compensation.

V. Experiment

The experiment has been carried out to demonstrate the validity of the dead time compensation strategy. The experiment system is an ac/dc/ac power conversion system. The source side line to line voltages are 220 V [rms] and the dc link voltage is regulated to maintain 370 [V]. The switching frequency is 5 kHz and the sampling time is 100 [μsec]. The load is a 22 kW induction machine and the power device is an IPM (intelligent power modules) whose current rating is 300 [A] and voltage rating is 600 [V]. In the experiment the dead time T_d is 6.3 [μsec].

Fig. 7 shows the process of the proposed strategy. From the top trace, the q-axis current I^s_{qs}, q-axis distorted voltage V'_{qs} and compensation time $T_{\rm com}$ are shown. In the experiment, the current reference $I^{s^*}_{qs1}$ and $I^{s^*}_{qs2}$ are 50 [A], 40 [A], respectively, and are varied at every 110 [msec]. The reference voltages, $V^{s^*}_{qs1}$ and $V^{s^*}_{qs2}$, are mean reference voltages during steady state. The final compensation time by this strategy is 5.45 [μsec]. The equivalent stator resistance $r_s + \frac{r_{ce}+r_d}{2}$ is found to be 0.067 [Ω], which is greater than the pure stator resistance (0.041 [Ω]) due to the voltage drop effect. In this experiment, It is seen that as adjusting compensation time, the current shows better regulation performance.

Three experiments have been done to compare the proposed method to the no dead time compensation case and the only dead time compensation case. In the only dead time compensation case, the dead time effect is compensated by adjusting the gating signal according to the current direction, where only the dead time is considered. Thus, this is an equivalent case where the compensation time is dead time. In most dead time compensation schemes, the compensation is done by adjusting the gating signal or by modifying the reference voltage according to the current direction. Two methods are functionally equivalent. Thus, the only dead time

compensation case may be said to be the commonly used method for dead time compensation.

The current waveforms at steady state is shown in Fig. 8 when the constant phase voltage reference (90 V [peak], 30 Hz) is applied to the load. The waveforms are the stationary q-axis current in the upper trace, and the stationary d-axis current in the lower trace. Fig. 8(a) shows the current waveforms when the dead time is not compensated, that is, the compensation time is equal to zero. Fig. 8(b) shows the current waveforms in the case of the only dead time compensation case, when the compensation time is equal to the dead time. In Fig. 8(c), the current waveforms is shown in the case of the proposed strategy. In Fig. 8(a), the currents are much distorted because of the distorted voltages. In Fig. 8(b), it is seen that the current is a little distorted and its x-y plot has the waveform like a hexagon. In Fig. 8(c), the currents maintain sinusoidal waveforms and its x-y plot has the waveform like a circle. In the case of Fig. 8(a) and (b), there exists the distorted voltage with the six-step waveform, which is the same phase with the phase current. The peak of the distorted voltages are 13.5 [V] in the case of Fig. 8(a), and 2 [V] in the case of Fig. 8(b). This experiment shows that the turn on/off time, voltage transition slope, and voltage drop of the switching device must be considered as well as dead time effect for the accurate voltage synthesis.

VI. Conclusion

A new compensation method for distorted voltage has been described in this paper that compensates both the dead time effect and the nonideal characteristics of the power devices in the PWM inverter system. The analysis of the voltage distortion is discussed with consideration of the dead time and the nonideal characteristics of the power devices. From this analysis, a novel dead time compensation method without any extra hardware is presented. Experimental results show considerable improvements in the output currents, thus verifying the validity of the proposed method. The proposed method produces the same inverter output voltages as the reference voltages, which may be advantageous in high-performance machine drive applications such as sensorless vector control and flux estimation. By applying this method to the general purpose PWM inverter system at the initial setup, a more accurate output voltage can be obtained. It can be applied with space vector PWM, which synthesizes accurate output voltage. In addition, the method can also be used to determine stator resistance including power device ohmic drop. Since no two motors are the same and the detailed behavior of any motor and its inverter changes slowly over time, by applying the proposed method whenever the inverter initiates its operation, more high control performance can be maintained.

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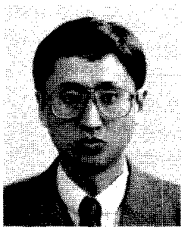

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