A New Compensation Strategy Reducing Voltage/Current Distortion in PWM VSI Systems Operating with Low Output Voltages

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Abstract—**In a voltage-fed PWM inverter, the relation between the reference voltage and the output voltage is nonlinear due to the dead time effect and the voltage drop of the switching devices. The nonlinear voltage distortion invokes serious problems such as current waveform distortion and deterioration of the performance. Especially, the clamping of current around the zero crossing point is the most serious problem in the low-frequency region. In this paper, the analysis of the zero current clamping phenomenon is discussed. From this analysis, a novel distorted voltage compensation method which eliminates zero current clamping is presented. Experimental results are also presented to demonstrate the validity of the proposed method.**

I. Introduction

VOLTAGE-FED PWM inverters have gained increasing popularity in industrial applications. In their application areas, the ac machine drive is one of the most important parts. Considering the development of the fast switching devices and modern control theory, a high-performance ac machine drive is expected to draw growing attention. In some applications such as sensorless vector control and direct vector control, the inverter output voltages are needed to calculate the desired state variables. Unfortunately, it is very difficult to measure the output voltage and it requires additional hardware. The most desirable method to obtain the output voltage is to use the reference voltage as the output voltage. Generally, the relation between the reference voltage and output voltage has a nonlinear characteristic due to the distorted voltage generated by a voltage-fed PWM inverter. Thus unless the distorted voltage is properly compensated, the reference voltage cannot be used as the output voltage. For this reason, the output voltage synthesis is very important in a voltage-fed PWM inverter. The distorted voltage may give rise to serious problems such as current waveform distortion, increased torque ripples, and unstable operation.

In a voltage-fed PWM inverter, there are several causes that distort output voltage. Some have originated from the inherent characteristic of the switching devices such as the voltage drop and the difference between turn-on and turn-off time. These effects vary with the direction of the current and should be taken into account for accurate output voltage synthesis [1]. Another cause is the dead time which is inevitable to prevent the shoot-through phenomenon [1]–[6]. Especially, when the current is nearly zero, the distortion of the output voltage is more severe (see Fig. 1). In Fig. 1, an oscillogram of an induction motor a-phase current waveform at low speed is shown and the a-phase current is very distorted when the magnitude of the current is nearly zero. Moreover, it is seen that the a-phase current is also distorted when the b- or c-phase current is nearly zero. Thus, the zero current clamping phenomenon results in the deterioration of the current waveform. This phenomenon is conspicuous when both the output frequency and voltage are low. Recently, remarkable efforts have been made to compensate for the voltage distortion by the dead time [1]–[6]. However, the zero current clamping phenomenon has hardly been studied and cannot be avoided in most of the papers [1]–[4]. The PWM strategy in [5] presents the solution of the zero current clamping but it requires extra hardware and a special PWM pattern in the neighborhood of zero crossing of the current. This PWM strategy restricts the number of switchings in the phase switches which convey the quasi-zero current to be small. Thus, this PWM increases the current ripple when the current is nearly zero.

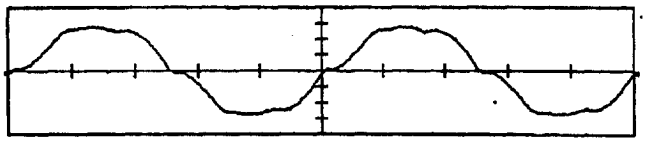

Fig. 1. Zero current clamping phenomenon.

This paper focuses on both the analysis of the zero current clamping phenomenon and the compensation of the distorted voltage to eliminate zero current clamping. In this compensation strategy, the distorted voltage is calculated in the real time and compensated in the feedforward manner. Combining the dead time compensation method in [1] which compensates not only the voltage drop effect and the turn-on/turn-off time effect, but also the dead time effect when the current is not nearly zero, this compensation strategy can accurately compensate the voltage distortion. Moreover, this scheme can be implemented by modifying only the software. So, with this method the reference voltage can be used as the inverter output

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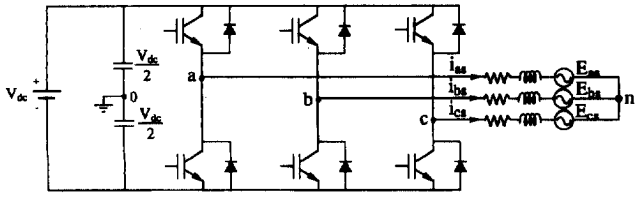

Fig. 2. Three-phase PWM inverter.

voltage without any extra hardware. By applying this method to the general purpose PWM inverter system, a more accurate output voltage synthesis is possible. Experimental results are also presented to demonstrate the validity of the proposed method.

II. Analysis of Zero Current Clamping

The commonly used three-phase PWM inverter is shown in Fig. 2, where the induction machine is modeled as an R-L network and a back-EMF. In the following discussions, V_{an}, V_{bn}, and V_{cn} denote the line-to-neutral voltages; V_{a0}, V_{b0}, and V_{c0} denote the pole voltages; E_{as}, E_{bs}, and E_{cs} denote the back-EMF's; and i_{as}, i_{bs}, and i_{cs} denote the phase currents. During the dead time, the current can flow through only the diode. Regardless of the current direction, the magnitude of the current decreases toward zero during dead time (T_d). If the current is nearly zero at the beginning of the dead time, the current decreases to zero and remains there during the rest of the dead time because the reverse voltage of the diode blocks the current flow.

If this phenomenon occurs in the a-phase current, the point "a" in Fig. 2 can be considered to be disconnected from the dc link because no current flows through the a-phase switches. Thus the line-to-neutral voltage (V_{an}) equals the a-phase back-EMF (E_{as}).

$$V_{an} = E_{as}. \tag{1}$$

This phenomenon is depicted in Fig. 3. It is seen from Fig. 3 that the voltage distortion occurs during zero current clamping time (T_z). In the following discussion, the voltage distortion due to the zero current clamping will be clearly examined.

The pole voltage V_{b0} and V_{c0} are defined by their switching functions and given by

$$V_{b0} = V_{dc}(S_b - \tfrac{1}{2}) \tag{2}$$
$$V_{c0} = V_{dc}(S_c - \tfrac{1}{2}). \tag{3}$$

In (2), the b-phase switching function S_b is 1 when the upper b-phase switch is on, and 0 when the lower b-phase switch is on. Similarly, the c-phase switching function S_c is 1 when the upper c-phase switch is on, and 0 when the lower c-phase switch is on. To solve V_{a0}, V_{bn}, and V_{cn}, consider the following equations:

$$V_{a0} = V_{an} + V_{n0} \tag{4}$$
$$V_{b0} = V_{bn} + V_{n0} \tag{5}$$
$$V_{c0} = V_{cn} + V_{n0}. \tag{6}$$

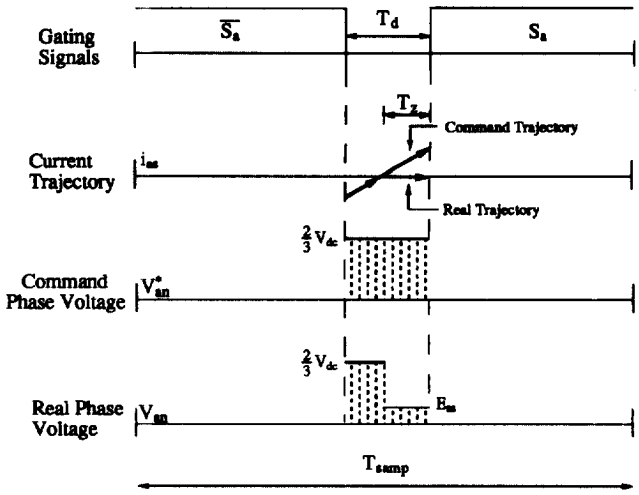

Fig. 3. Zero current clamping phenomenon.

The absence of a neutral connection in the motor forces the constraint which is

$$i_{as} + i_{bs} + i_{cs} = 0. \tag{7}$$

For any balanced load, the line-to-neutral voltages are constrained such that

$$V_{an} + V_{bn} + V_{cn} = 0. \tag{8}$$

These give

$$V_{n0} = \tfrac{1}{3}(V_{a0} + V_{b0} + V_{c0}). \tag{9}$$

By combining the voltage equations, V_{a0}, V_{bn}, and V_{cn} are solved as

$$\begin{aligned} V_{a0} &= \tfrac{3}{2}V_{an} + \tfrac{1}{2}(V_{bo} + V_{c0}) \\ &= \tfrac{3}{2}E_{as} + \tfrac{1}{2}(V_{bo} + V_{c0}) \end{aligned} \tag{10}$$

$$\begin{aligned} V_{bn} &= \frac{2V_{b0} - V_{c0} - V_{a0}}{3} \\ &= \frac{V_{b0} - V_{c0} - E_{as}}{2} \end{aligned} \tag{11}$$

$$\begin{aligned} V_{cn} &= \frac{2V_{c0} - V_{a0} - V_{b0}}{3} \\ &= \frac{V_{c0} - V_{b0} - E_{as}}{2}. \end{aligned} \tag{12}$$

From (1), (11), and (12), all the line-to-neutral voltages are distorted during the zero current clamping period by the term E_{as}, which results in current distortion. If these voltages are represented in the stationary dq-axis

$$\begin{aligned} V^s_{qs} &= V_{an} \\ &= E_{as} \end{aligned} \tag{13}$$

$$\begin{aligned} V^s_{ds} &= \frac{V_{cn} - V_{bn}}{\sqrt{3}} \\ &= \frac{V_{c0} - V_{b0}}{\sqrt{3}} \\ &= \frac{V_{dc}(S_c - S_b)}{\sqrt{3}}. \end{aligned} \tag{14}$$

Equations (13) and (14) imply that if the zero current clamping occurs in a-phase, only the stationary q-axis voltage

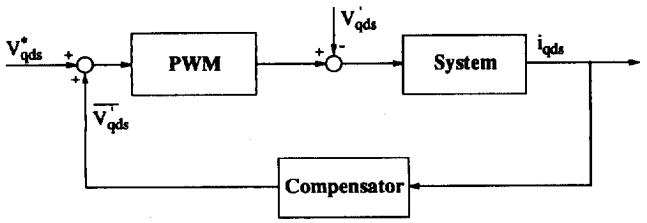

Fig. 4. Compensation of the distorted voltage.

is distorted. Thus the distorted voltages in the stationary reference frame can be determined as

$$V_{qs}^{s\prime} = V_{qs}^{s*} - V_{qs}^{s} = V_{an}^{*} - E_{as} \quad (15)$$

$$V_{ds}^{s\prime} = V_{ds}^{s*} - V_{ds}^{s} = 0. \quad (16)$$

The command voltage V_{an}^{*} means the scheduled voltage applied during the dead time and can be determined from the reference voltage vector and current direction. With similar analysis, if the zero current clamping occurs in b-phase, the distorted voltages are

$$V_{qs}^{s\prime} = V_{qs}^{s*} - V_{qs}^{s} = -\frac{1}{2}(V_{bn}^{*} - E_{bs}) \quad (17)$$

$$V_{ds}^{s\prime} = V_{ds}^{s*} - V_{ds}^{s} = -\frac{\sqrt{3}}{2}(V_{bn}^{*} - E_{bs}). \quad (18)$$

And if the zero current clamping occurs in c-phase, the distorted voltages are

$$V_{qs}^{s\prime} = V_{qs}^{s*} - V_{qs}^{s} = -\frac{1}{2}(V_{cn}^{*} - E_{cs}) \quad (19)$$

$$V_{ds}^{s\prime} = V_{ds}^{s*} - V_{ds}^{s} = \frac{\sqrt{3}}{2}(V_{cn}^{*} - E_{cs}). \quad (20)$$

III. Compensation Strategy

From the above discussion, the distorted voltages in the zero current clamping region can be predicted from the command voltage and back-EMF during the dead time. And the mean distorted voltage during a sampling period can be represented as follows:

$$\overline{V_{qs}^{s\prime}} = V_{qs}^{s\prime}\frac{T_z}{T_{\text{samp}}} \quad (21)$$

$$\overline{V_{ds}^{s\prime}} = V_{ds}^{s\prime}\frac{T_z}{T_{\text{samp}}} \quad (22)$$

where T_{samp} denotes the sampling period. By compensating the mean distorted voltage to the reference voltage, the zero current clamping phenomenon is eliminated. The overall compensation strategy is shown in Fig. 4.

IV. Practical Implementation

In this section, the practical implementation will be explained and the example is limited only on the a-phase. In the case of the other phases, the similar analysis is possible.

TABLE I
Command Voltages During the Dead Time

Mode	V_{as}^{*}		V_{bs}^{*}		V_{cs}^{*}	
	$I_{as}>0$	$I_{as}<0$	$I_{bs}>0$	$I_{bs}<0$	$I_{cs}>0$	$I_{cs}<0$
1	0	$\frac{2}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	0
2	$-\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	0	$\frac{2}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	0
3	$-\frac{2}{3}V_{dc}$	0	0	$\frac{2}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$
4	$-\frac{2}{3}V_{dc}$	0	$-\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	0	$\frac{2}{3}V_{dc}$
5	$-\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	0	0	$\frac{2}{3}V_{dc}$
6	0	$\frac{2}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	0	$-\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$

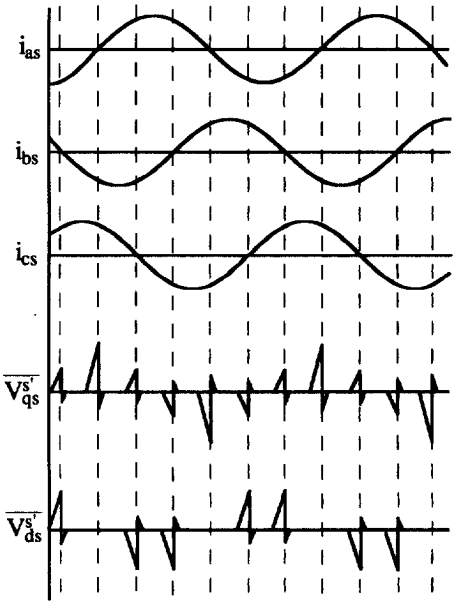

Fig. 5. Compensation voltages.

A. Back-EMF

The back-EMF can be calculated from the machine model. In the case of an induction machine, using the stator referred transient equivalent circuit, the voltage equations in a synchronous dq-axis may be represented as follows:

$$V_{qs}^{e} = r_s i_{qs}^{e} + \sigma L_s \frac{di_{qs}^{e}}{dt} + \omega\sigma L_s i_{ds}^{e} + E_{qs}^{e} \quad (23)$$

$$V_{ds}^{e} = r_s i_{ds}^{e} + \sigma L_s \frac{di_{ds}^{e}}{dt} - \omega\sigma L_s i_{qs}^{e} + E_{ds}^{e} \quad (24)$$

where ω is synchronous speed, r_s is the stator resistance, and σL_s is the stator transient inductance such that

$$\sigma L_s = L_s - \frac{L_m^2}{L_r}. \quad (25)$$

Thus, in the steady-state, the back-EMF in a synchronous dq-axis can be calculated as

$$E_{qs}^{e} = V_{qs}^{e*} - r_s i_{qs}^{e} - \omega\sigma L_s i_{ds}^{e} \quad (26)$$

$$E_{ds}^{e} = V_{ds}^{e*} - r_s I_{ds}^{e} + \omega\sigma L_s i_{qs}^{e}. \quad (27)$$

After filtering (26) and (27) to reject high-frequency components and then transforming them to the abc-axis, the three-phase back-EMF's E_{as}, E_{bs}, and E_{cs} are obtained.

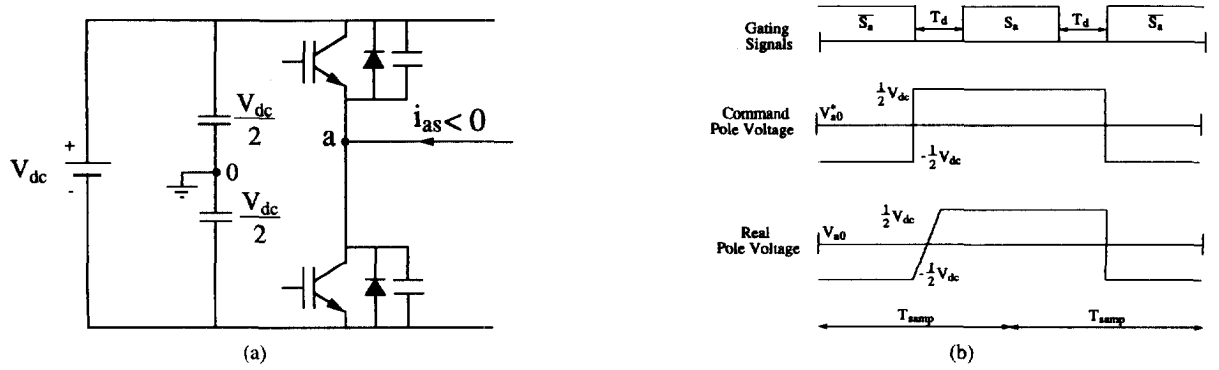

Fig. 6. Voltage distortion by the nonideal diode: (a) PWM inverter with nonideal diode and (b) voltage distortion due to the nonideal diode.

B. Current on the Point of the Switching

To accurately compensate the distortion voltage, the current on the point of the switching is needed. Unfortunately, only the sampled current by an analog-to-digital converter is available in most applications. If the sampled current is used as the current on the point of the switching to compensate the distorted voltage, less accurate compensation may be obtained. Thus, for more accurate compensation of the distortion voltage, the current on the point of the switching should be estimated. The switching point of each phase is found from the PWM switching patterns. The current trajectory can be predicted from the reference voltage, back-EMF, stator transient inductance and the sampled current by the analog-to-digital converter.

C. Command Voltage

The command voltage during the dead time is the scheduled voltage to compensate the dead time effect, and is the function of the current direction and the mode of the reference voltage vector defined in [7]. For example, if the a-phase current is negative, the upper switch of the a-phase is treated to conduct during the dead time. And if the reference voltage vector lies in mode 1, both the lower switches of the b-phase and c-phase are turned on during the a-phase dead time. Thus in this case, the a-phase command voltage during the dead time is $\frac{2}{3}V_{\rm dc}$. In this way, all the command voltages are obtained and summarized in Table I. In Table I, I_{as}, I_{bs}, and I_{cs} mean the currents on the point of each phase switching.

D. Zero Current Clamping Time

In this study, the resistance voltage drop is ignored because the operating region in which the current is nearly zero is of interest. With the information of the I_{as}, V_{an}^*, and E_{as}, the zero current clamping time T_z is estimated as

$$T_z = T_d + I_{as}\frac{\sigma L_s}{V_{an}^* - E_{as}}. \tag{28}$$

Since the zero current clamping time is greater than zero and less than dead time, the estimated time in (28) does not hold when it is less than zero or greater than dead time. In that case, it means that the zero current clamping phenomenon does not occur during the dead time. On the other hand, if the calculated zero current clamping time is greater than zero and less than dead time, the zero current clamping phenomenon is expected to occur and the distorted voltage compensation should be carried out.

E. Zero Current Clamping Region

The zero current clamping region is the current boundary where the zero current clamping phenomenon occurs, and it can be predicted from (28). If $V_{an}^* - E_{as}$ is positive, the zero current clamping region is

$$-\frac{T_d(V_{an}^* - E_{as})}{\sigma L_s} < I_{as} < 0 \tag{29}$$

otherwise

$$0 < I_{as} < -\frac{T_d(V_{an}^* - E_{as})}{\sigma L_s}. \tag{30}$$

In the steady-state, when the a-phase current passes zero from negative to positive, the reference voltage vector lies in mode 6 and the back-EMF is positive. Thus from Table I and (29) and (30), the zero current clamping region is

$$-\frac{T_d\left(\frac{2}{3}V_{dc} - E_{as}\right)}{\sigma L_s} < I_{as} < \frac{T_d E_{as}}{\sigma L_s}. \tag{31}$$

F. Distorted Voltage Compensation

In the above case, if the current is negative, the compensation voltages are

$$\overline{V_{qs}^{s\prime}} = \frac{1}{T_{\rm samp}}\left[I_{as}\sigma L_s + \left(\frac{2}{3}V_{\rm dc} - E_{as}\right)T_d\right] \tag{32}$$

$$\overline{V_{ds}^{s\prime}} = 0. \tag{33}$$

If the current is positive, the compensation voltages are

$$\overline{V_{qs}^{s\prime}} = \frac{1}{T_{\rm samp}}\left(I_{as}\sigma L_s - E_{as}T_d\right) \tag{34}$$

$$\overline{V_{ds}^{s\prime}} = 0. \tag{35}$$

By performing a similar analysis to all the zero current regions, the compensation voltages are found as shown in Fig. 5. It is seen from (31) that if the stator transient inductance is small, the zero current clamping region is extended. If the output frequency is low, the current stays in the zero current clamping region for a long time. And if the reference voltage is

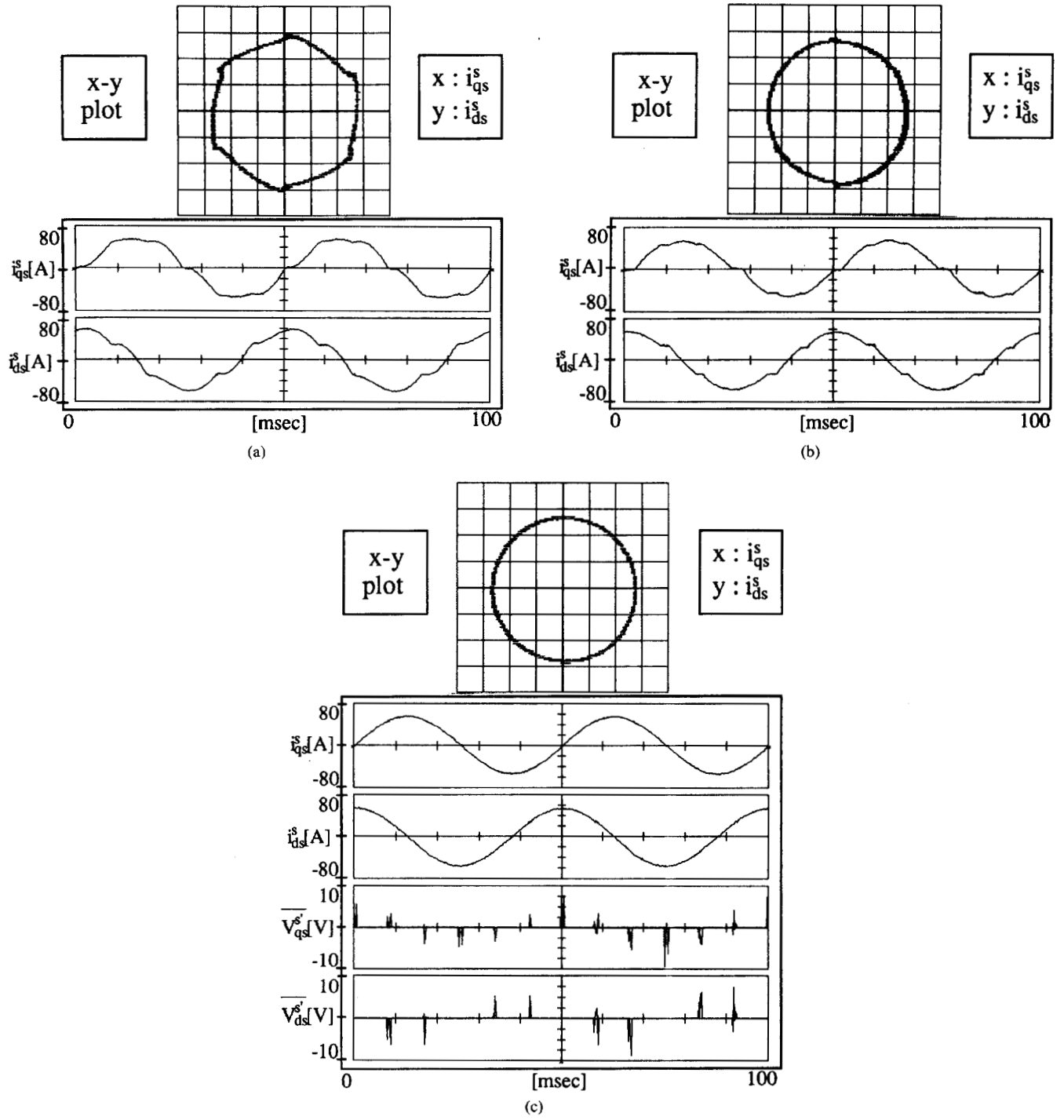

Fig. 7. Current waveforms: (a) No dead time compensation, (b) dead time compensation strategy [1], and (c) proposed strategy.

low, the distorted voltage occupies more of a portion in output voltage. Thus in the case of the low stator transient inductance, the low output frequency, and the low reference voltage, the voltage distortion due to zero current clamping is more severe.

V. Another Reason for Zero Current Clamping

Another reason to distort output voltage is the nonideal characteristic of the diode [6]. Assume that the a-phase current is negative and nearly zero. In Fig. 6, the rising of the pole voltage V_{a0} is somewhat slow at the switching point. At that point, the upper diode is reverse biased so that it will not provide the current path. Therefore the current must first charge the lower effective parasitic capacitor before the upper diode can conduct. The rate of change of the voltage is inversely proportional to the parasitic capacitance and directly proportional to the current. In a low current region, this phenomenon is more remarkable, which results in the output voltage distortion.

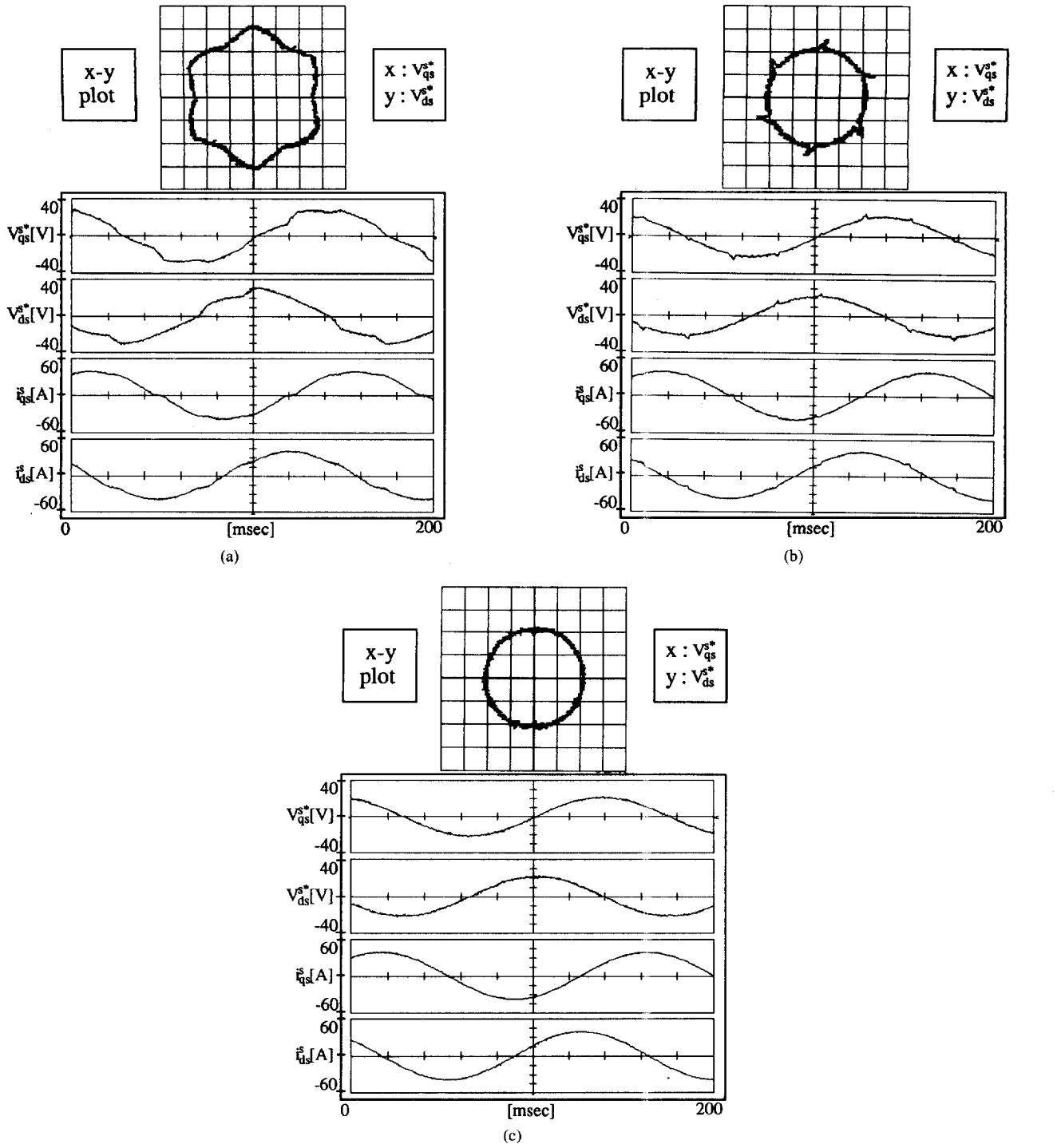

Fig. 8. Voltage and current waveforms: (a) no dead time compensation, (b) dead time compensation strategy [1], and (c) proposed strategy.

To simplify this problem, it is assumed that this phenomenon occurs only when the magnitude of the current is below I_{set} and its effect is linearly increased as the magnitude of current is decreased. Then, if the a-phase current is negative and nearly zero, the compensation voltages are modeled as follows:

$$\overline{V_{qs}^{s\prime}} = R_{\text{set}}(I_{as} + I_{\text{set}}) \tag{36}$$

$$\overline{V_{ds}^{s\prime}} = 0. \tag{37}$$

In (36), the fictitious resistance (R_{set}) is introduced to model the voltage distortion and can be determined by the characteristics of the power devices. The current level (I_{set}) can also be determined by the characteristics of the power devices. If the a-phase current is positive and nearly zero, the compensation voltages are

$$\overline{V_{qs}^{s\prime}} = R_{\text{set}}(I_{as} - I_{\text{set}}) \tag{38}$$

$$\overline{V_{ds}^{s\prime}} = 0. \tag{39}$$

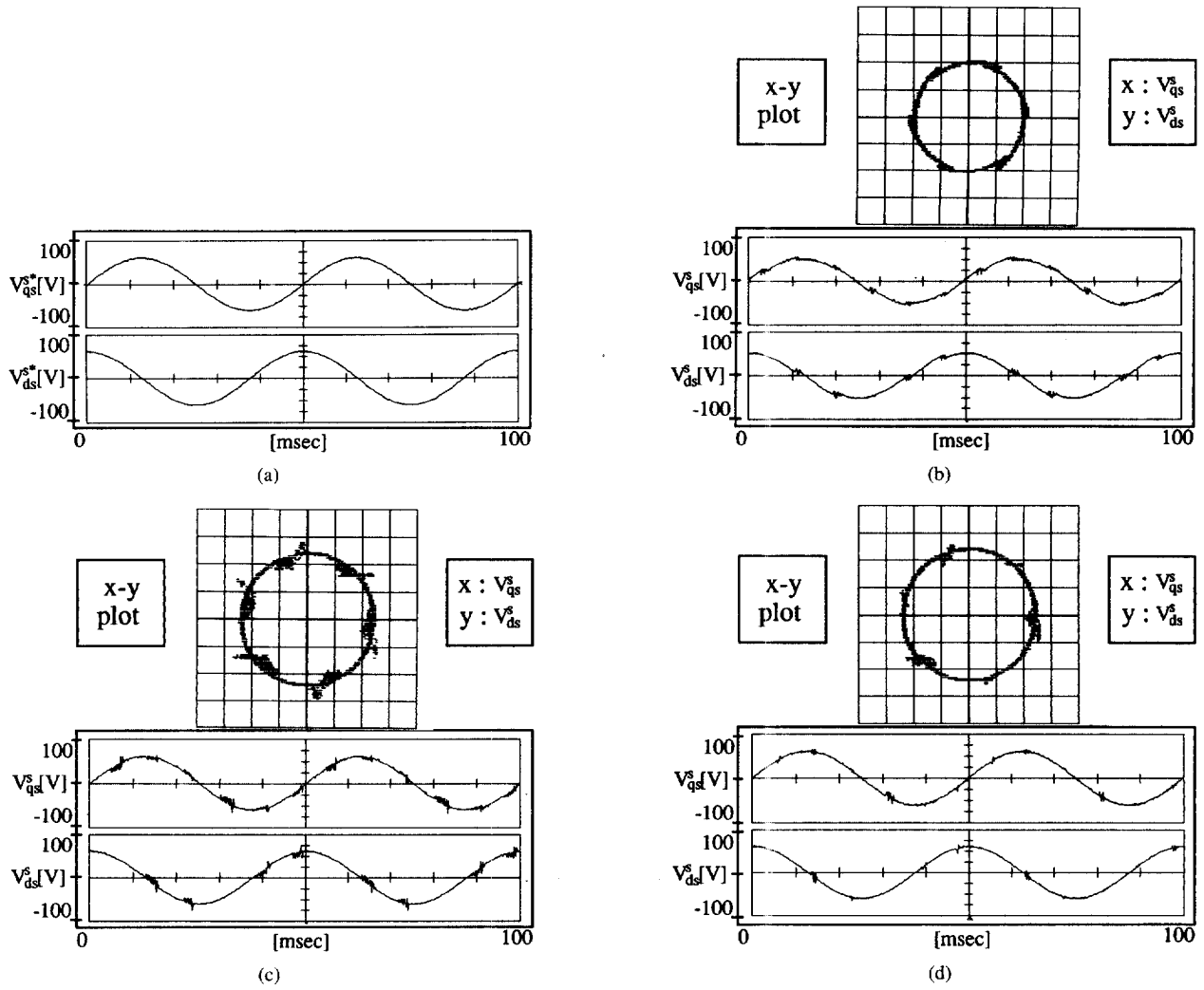

Fig. 9. Output voltage waveforms: (a) reference voltages, (b) no dead time compensation, (c) dead time compensation strategy [1], and (d) proposed strategy.

Note these compensation voltages are same formulas with (32)–(35), and thus are easily combined with the proposed scheme.

VI. Experiment

Experimental results are presented to show the validity of the proposed distorted voltage compensation strategy in the zero current clamping region. The power device is an IPM (Intelligent Power Module) whose current rating is 300 [A] and voltage rating is 600 [V] and the dc-link voltage is about 310 [V]. The switching frequency is 5 [kHz] and the sampling time is 100 [μs]. The dead time T_d is 6.3 [μs] and the load is the 22 [kW] induction machine whose parameters are listed in the Table II. The stator transient inductance σL_s is about 1 [mH].

The experiment is divided into three parts. One is to observe the current distortion when the constant voltage is applied and another is about the voltage distortion when the current is regulated. The last experiment presents the real output voltage waveforms when the constant voltage is applied. In each case, the proposed scheme is compared with no dead time compensation case and the dead time compensation scheme in [1].

TABLE II
Induction Machine Parameters

Stator Resistance (r_s)	**0.0413 [Ω]**
Rotor Resistance (r_r)	**0.0407 [Ω]**
Stator Inductance (L_s)	**13.65 [mH]**
Mutual Inductance (L_m)	**13.28 [mH]**
Rotor Inductance (L_r)	**13.95 [mH]**

A. Current Distortion

In this experiment, the peak phase voltage is set to 60 [V] (20 [Hz]). The dq-axis current waveforms in the steady state are shown in Fig. 7. In Fig. 7(a), the currents are very distorted because of the distorted voltage. In Fig. 7(b), it is seen that the current is nearly sinusoidal except in the zero current clamping region. In Fig. 7(c), the currents maintain sinusoidal waveforms and their x–y plot exhibits the round shape. The improvement is apparent. The stationary q-axis and d-axis compensation voltages are also shown in Fig. 7(c). By

adding these compensation voltages to the reference voltages, the accurate voltage synthesis is possible.

B. Voltage Distortion

In this experiment, the machine is operated at constant speed (200 [r/min]) with constant current reference. The dq-axis reference voltages and current waveforms in the steady-state are shown in Fig. 8. In Fig. 8(a), the reference voltages are very distorted to regulate the current because the distorted voltages are not compensated at all. The waveforms in Fig. 8(b) show that distorted voltages are not compensated in the zero current clamping region. In Fig. 8(c), the voltages maintain sinusoidal waveforms, which show the perfect distorted voltage compensation. The current waveforms in Fig. 8(c) show the best regulation performance by the distorted voltage compensation.

C. Output Voltages

To verify the validity of the output voltage synthesis using the proposed method, the real output voltage is monitored with the additional hardware. The voltages across the lower devices of the inverter are delivered to the control board through the optic fiber. In the control board, the monitored voltages are reconstructed to the dq-axis voltages using the concept of the space vector modulation in real time. In this experiment, the peak phase voltage command is 60 [V] (20 [Hz]) as shown in Fig. 9(a). The monitored dq-axis output voltage waveforms in the steady state are shown in Fig. 9(b)–(d). In Fig. 9(b), the voltages are very distorted because of the dead time effect. It is also observed that the fundamental component of the voltage is reduced. In Fig. 9(c), it is seen that the voltages are distorted in the zero current clamping region. The output voltage synthesis using the proposed scheme is seen in Fig. 9(d). The output voltages are slightly distorted compared to the reference voltage. The high-frequency ripple of the output voltage in the zero clamping region has little effect on the output current. It is mainly due to the current measuring error (Especially, in this system, the c-phase current is not measured and is calculated with a- and b-phase currents). These results show the great improvement in the output voltage synthesis.

VII. Conclusions

In this paper, the detailed analysis of the zero current clamping phenomenon is made. From this analysis, a novel distorted voltage compensation method which eliminates zero current clamping is presented. With this method, the reference voltage can be used as the inverter output voltage without any extra hardware. By applying this method to the general purpose PWM inverter system, a more accurate output voltage synthesis is possible with no additional cost. Experimental results verify the effectiveness of the proposed method.

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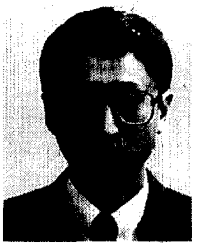

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