Single Current Sensor Technique in the DC Link of Three-Phase PWM–VS Inverters: A Review and a Novel Solution

Frede Blaabjerg, *Member, IEEE,* John K. Pedersen, *Member, IEEE,* Ulrik Jaeger, and Paul Thoegersen, *Member, IEEE*

***Abstract*— A review of the existing methods to determine the output currents in a pulsewidth modulation voltage-source (PWM–VS) inverter using a single current sensor in the dc link is presented, and a novel solution is proposed. The unique arrangement of the dc link allows full protection of the inverter from short circuits and overloads. Also, a new method of sampling the dc-link current is described that produces true values of the output currents at the centers of switching intervals. Results of investigation of an experimental setup have shown that full protection of the inverter has been accomplished and the output currents can accurately be determined within the whole operating area.**

***Index Terms*—AC drives, current sampling, modulation, sensor reduction.**

NOMENCLATURE

$\Delta\theta$	Voltage vector position change in one switching period.
$\Delta\theta_e$	Angle error of current sampling.
D	Duty cycle.
$D1$, $D2$	Diodes in inverter.
$Error$	Error signal from the overcurrent protection.
f	Fundamental frequency.
$f(\theta)$	Lookup table value.
$f_{\rm sw}$	Switching frequency.
i_1, i_2, i_3	Phase currents.
i_A, i_B, i_C	Sampled output currents by sample/hold circuit in a half switching period.
$i_{\rm DC}$	DC-link current.
$i_{\rm DC1}$	Positive dc-bus current.
$i_{\rm DC2}$	Negative dc-bus current.
$I_{\rm limit}$	Overcurrent limit.
$I_{\rm PE}$	Earth or ground current.
$I_{\rm PE,\,limit}$	Earth current limit.
$I_{\rm SH}$	Short-circuit current.
l_c	Cable length.
$N1$	Number of windings carrying the positive dc-bus current.
$N2$	Number of windings carrying the negative dc-bus current.
PE, $error$	Error signal from the earth fault protection.
$PQ1$, $PQ2$	Gate signals to IGBT.
$s1$, $s2$, $s3$	PWM signals for three phases.
$SAMPLEA$, $SAMPLEB$, $SAMPLEC$	Sample signals for dc-link currents.
$SAMPLEE$	Sample signal for earth current.
θ	Voltage vector position.
$T1$, $T2$, $T3$, $T4$, $T5$	Transistors in inverter.
t_b	Blanking time.
t_c	Center time of double-sided modulation.
$TCLXX$	Counter values in CAPCOM registers XX.
t_d	Minimum time delay in sampling.
t_{e1}, t_{e2}	Sample time of earth current.
t_p	Duration of one active voltage vector.
t_{s1}, t_{s2}, t_{s3}, t_{s4}	Sampling instants in the dc link.
$T_{\rm sw}$	Switching period.
t_t	Duration of current pulse in cable.
$\underline{u}_s$	Voltage reference vector.
$U_{\rm DC}$	DC-link voltage in inverter.
$U_{\rm ref}$	Voltage vector length.
v_s	Traveling speed of voltage.
$Z_{\rm SH}$	Short-circuit impedance to earth or to ground.

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F. Blaabjerg and J. K. Pedersen are with the Institute of Energy Technology, Aalborg University, DK-9220 Aalborg East, Denmark (e-mail: fbl@iet.auc.dk; jkp@iet.auc.dk).

U. Jaeger and P. Thoegersen are with the Transmission Division, Danfoss Drives A/S, DK-6300 Graasten, Denmark (e-mail: ulrik_jaeger@danfoss.com; paul_thoegersen@danfoss.com).

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I. INTRODUCTION

POWER electronic converters improve the performance and reduce the energy consumption in many industrial and domestic applications. A converter which has a very widespread use is a three-phase hard-switched inverter supplied from a three-phase diode rectifier. The main applications are motor control [1]–[3], uninterruptible power supply (UPS), high power factor rectifiers [4], [5], and compensators of

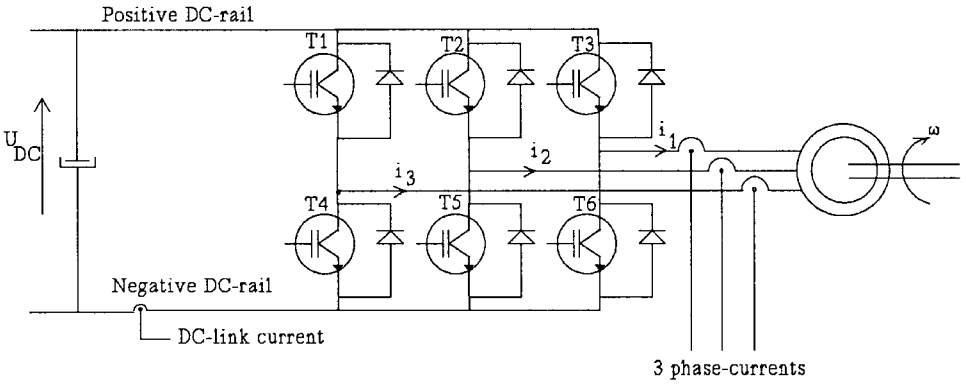


Fig. 1. Fully protected B6 inverter for motor drive.

reactive and harmonic currents in power systems [6], [7]. The information about the currents in the three output phases is of importance. Also, a power converter should be protected against possible fault conditions like short circuit of the dc link, short circuit of the output phases, and possible ground faults.

An effective method to obtain full information about the output currents (three phase) is to measure those directly by three current sensors and, optionally, to protect the dc link with a fourth current sensor. However, this approach is not economical, and an alternative is to measure the dc-link current and, based on this signal and pulsewidth modulation (PWM) information output, currents can be determined (reconstructed), as proposed in [8]. This strategy needs only one current sensor, and it uses a voltage vector with one active transistor and a voltage vector with two active transistors to obtain information about two output currents from which the third can easily be calculated [8]. This method has some disadvantages. The output current cannot be determined properly when one active vector is used only for a short time, and protection of the inverter is not ensured in all fault cases. The currents are sampled at different times within a switching interval, and effects of cables between an inverter and a load are not taken into account.

Various approaches have been proposed in [9]–[20], but all of them have certain limitations. The method described in [19] can solve almost all problems, except that the dc-link current sensor should be rated to measure the double dc current, which both gives a poorer resolution of the current measurement and a more expensive current sensor. This paper proposes a solution for accurate determination of the output currents in a normally rated dc-current sensor in the dc link which provides complete fault protection. Also, an improved sensing technique is presented, which is very useful when long cables are used and which also gives an instantaneous sampling of the currents.

The inverter topology and the relationship between the dc-link current, the output current, and the voltage vector are defined first. Next, a review of all known proposals to improve the concept in [8] is done. The proposed solutions are presented and different fault situations are discussed. An implementation of the solutions is shown and test results are described.

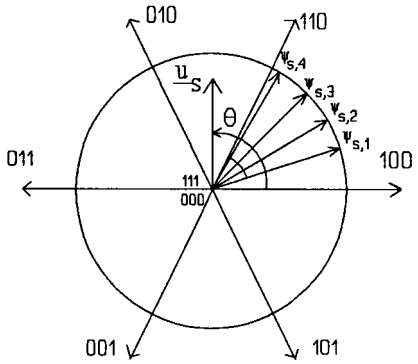


Fig. 2. Eight discrete voltage vectors in a B6 inverter and some stator-flux vectors.

II. Topology and Definitions

The most common topology for motor drives is a B6 inverter with six transistors and six diodes, as shown in Fig. 1.

In general, an inverter for motor drives must satisfy several requirements, such as the following:

- overload protection;
- ground-fault protection;
- short-circuit protection of dc link;
- full phase-current information.

The topology shown in Fig. 1 fulfills these requirements, but four current sensors must be used. In some inverters, the dc-link current sensor is omitted by employing a blanking time in the inverter bridge.

In the case of a B6 inverter, the space-vector modulation strategies are well known, so they are only briefly described here. The B6 inverter has eight discrete voltage vectors represented with two zero vectors and six active vectors. Fig. 2 shows the possible voltage vectors and certain stator-flux vectors for a B6 inverter.

An optimized switching sequence when changing the stator-flux vector in the sector between 100 and 110, should be [23]

$$000 \rightarrow 100 \rightarrow 110 \rightarrow 111 \rightarrow 111 \rightarrow 110 \rightarrow 100 \rightarrow 000. \quad (1)$$

A minimum torque ripple is obtained by choosing the zero-vector time of 000 and 111 equal. The result is a simple

TABLE I
RELATIONSHIP BETWEEN VOLTAGE VECTOR, DC-LINK CURRENT, AND ACTUAL OUTPUT CURRENTS

Voltage Vector	DC-link current i_{DC}
$\underline{u}_s$ = (100)	+ i_1
$\underline{u}_s$ = (110)	- i_3
$\underline{u}_s$ = (010)	+ i_2
$\underline{u}_s$ = (011)	- i_1
$\underline{u}_s$ = (001)	+ i_3
$\underline{u}_s$ = (101)	- i_2
$\underline{u}_s$ = (000) = (111)	0

modulation curve, as shown in [23]. It is well known that it is possible to determine the phase current in the three phases by a dc-link current sensing. Table I shows the relationship between the active voltage vectors and the actual dc-link current.

The modulation technique described for a B6 inverter ensures that two active voltage vectors will be present during each switching interval, allowing determination of the output currents. A general demand for the modulation strategy is that a zero vector, an active vector with one active switch, and an active vector with two active switches should be present during each switching period. However, the sequence (111)–(110)–(001) is not allowed, because only i_3 is then known. A ground fault can be detected when a zero vector is used. Problems arise for a current-sensing strategy described when the duty cycles of two phases are almost equal, because only a very small amount of time is available to measure the actual output current in the dc link. The following five cases can cause trouble:

1) low modulation index;
2) reference voltage $\underline{u}_s$ passes an active vector;
3) overmodulation;
4) long cables between the inverter and the load;
5) phase shift in the current measurement.

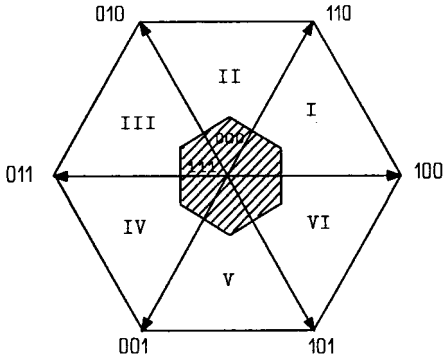
A. Low Modulation Index

At a low modulation index, the duty cycles or the PWM signals for the three phases will have an almost equal duration. The result is that the active voltage vector is not being used long enough to ensure a proper sampling of the dc-link current. Fig. 3 illustrates the problem in a double-sided modulation strategy.

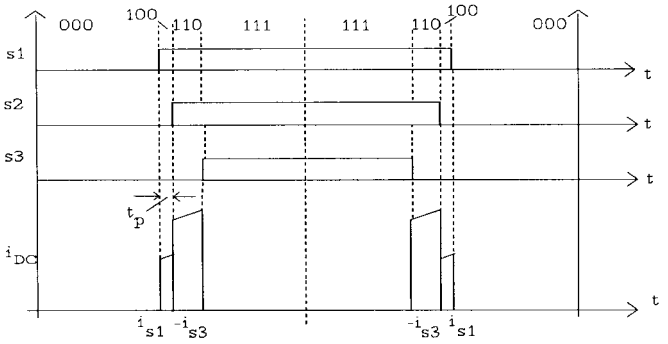
The duration of the active vector is denoted by t_p in Fig. 3. It is necessary to generate a minimum time delay t_d from which a proper sampling can be obtained. The delay time is dependent on the reverse recovery time of the diode or the transistor behavior, the influence of blanking time t_b, and the sampling time of the dc-link current. Improper output current determination may otherwise occur.

B. Reference Voltage $\underline{u}_s$ Passes an Active Vector

A minimum delay time t_d can be difficult to obtain when the reference voltage $\underline{u}_s$ passes an active vector. Fig. 4 shows the area where problems appear, and an example of the PWM signals is also shown.

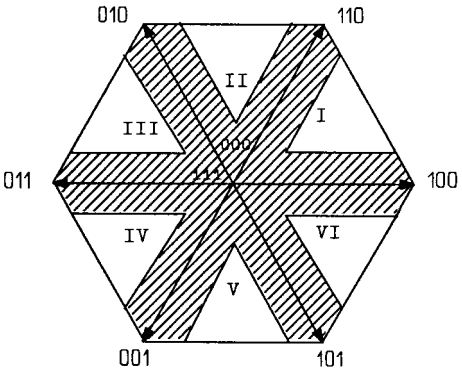


(a)

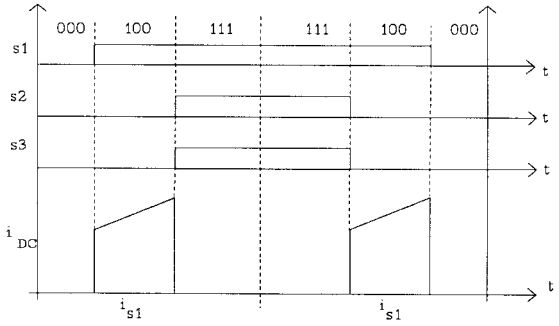


(b)

Fig. 3. Three-phase PWM signals and dc-link current at low modulation index. (a) Voltage vector area. (b) Example of three PWM signals.



(a)



(b)

Fig. 4. Three-phase PWM signals and dc-link current when the reference voltage passes an active voltage vector. (a) Voltage vector area. (b) Example of three PWM signals.

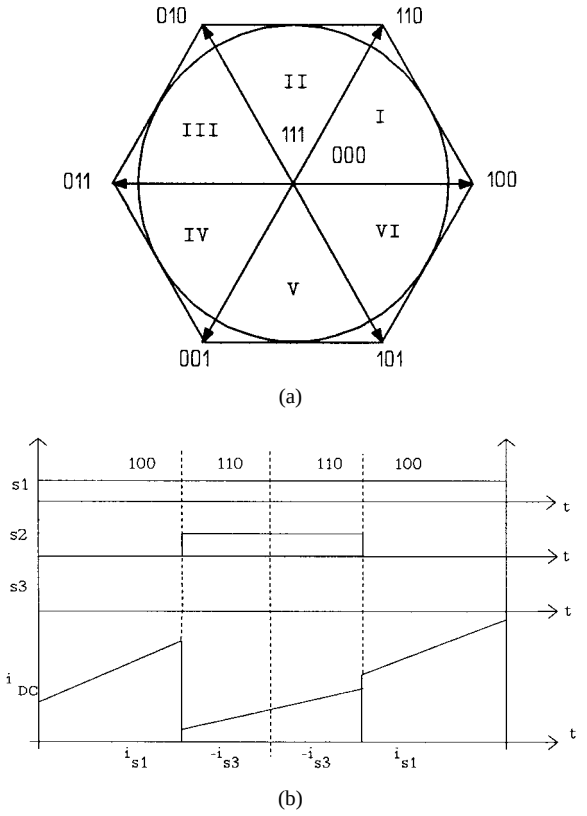


Fig. 5. Three-phase PWM signals and dc-link current when the reference voltage is in the overmodulation range. (a) Voltage vector area. (b) Example of three PWM signals.

One of the output currents is always correctly sampled because of the sufficient amount of time, but the other output currents cannot be directly sampled if the duration of the active vector is too short. Thus, two output currents cannot be sampled correctly.

C. Overmodulation

When the inverter enters overmodulation, there is not enough time for the space-vector modulation to use a zero voltage vector. The whole switching time is spent on active vectors. Fig. 5 shows PWM signals when the inverter operates in the overmodulation range.

If space-vector modulation is used with only one branch switch over (1 BSO), the two output currents will contribute to the dc-link current in one sampling period. However, no zero vectors are present, and it can be difficult to detect a high-impedance ground fault in the system.

D. Long Cables

Practical conditions are much less ideal with long (up to several hundred meters) cables between the inverter and the load (motor). Three-phase cables with or without screens have waveguide properties, i.e., each inverter voltage-vector switching action leads to a traveling voltage/current wave down along the cable which reflects at the load, doubling the voltage and traveling back to the inverter. This is seen as a short circuit, due to the dc-link capacitor receiving reversed current. Two measured current waveforms are shown in Fig. 6 with different cable lengths l_c. Both a switching period and a zoom of one switching vector state change are shown.

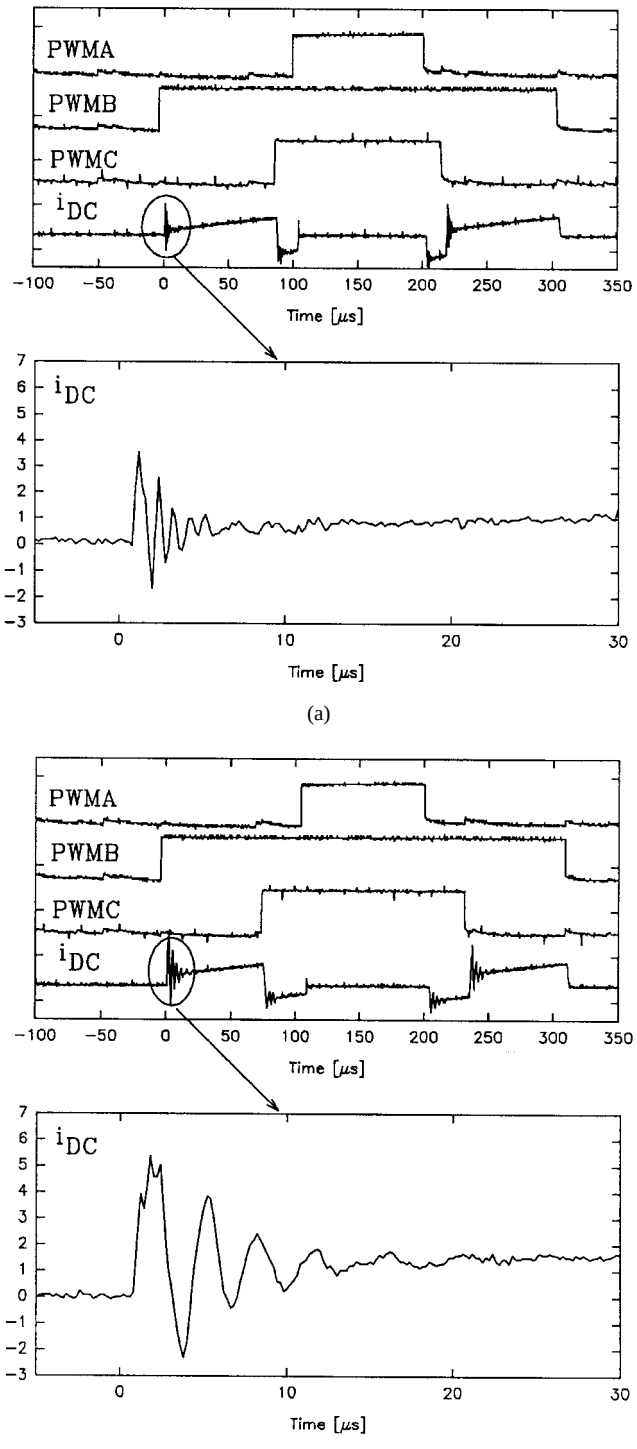


Fig. 6. Measured dc-link current and PWM signals with two different cable lengths to the motor. (a) $l_c = 10$ m. (b) $l_c = 100$ m.

Fig. 6 shows that, when a vector state changes, the cable initially loads the inverter with an almost fixed current and, afterwards, when the voltage traveling wave returns to the inverter, a current oscillation appears, which is damped by the cable. The oscillation is caused by the traveling wave which

moves between the inverter and the motor. The duration t_t of the first current pulse is given by the voltage traveling speed v_s and the length l_c of the cable:

$$t_t = \frac{2 \cdot l_c}{v_s} \tag{2}$$

where

t_t duration of current pulse in cable;
l_c cable length;
v_s traveling speed of voltage.

The traveling speed depends on the cable type, but half the speed of light is typical (150 m/μs). The damped resonant circuit current also depends on the length of the cable. After two periods, the current is almost stabilized and ready to be sampled. However, a delay between a voltage-vector state and the current sampling will be necessary.

The same kind of problems is also present when the zero-vector current is sampled (ground-fault current) because of the similar behavior with regard to the shield of the cable. Again, a delay is necessary to obtain a reliable measurement in the zero-vector state. This cannot be seen in Fig. 5, because an unshielded cable is used.

E. Phase Shift in the Current Measurement

Only one current sensor is used, and it is not possible to get simultaneous current samples. A delay will, in practice, be present between the two current samples when the two active voltage vectors are used. If a high ratio between the switching frequency and the fundamental frequency is used, only very small inaccuracies result, but, at a low ratio, the influence can be significant. The angle error $\Delta\theta_e$ can be expressed as

$$\Delta\theta_e = \frac{1}{4} \cdot \frac{360^\circ}{f_{sw}} \cdot f \tag{3}$$

where

$\Delta\theta_e$ angle error of current sampling;
f_{sw} switching frequency;
f fundamental frequency.

Here, it is assumed that the two samplings are made a half switching period apart (worst case). The result is poor accuracy of the output current measurement.

III. Review of the Existing Solutions

Several papers and patents exist in the area of single-sensor techniques in the dc link, where some of the problems discussed in the previous paragraph are more or less solved. Reference [8] was the first to propose the dc-link current use, followed shortly by [10]. In [8], the dc-link current sensing is used in different PWM schemes, which are natural PWM, delta modulation, and preprogrammed PWM. The methods are used in a simple control scheme for an induction motor [9] with good results, but problems related to very low modulation index, long cables, delay of current sampling, and protection of earth faults are not discussed. The problem with too short sampling time for a specific current is solved by a filter in the acquisition circuit. The sampling method has been patented in [16].

In [10], a discrete modulation method is used to control an induction motor where only active switching vectors are used in a resonant converter. It does not have the same problems from a hard-switched PWM–VS inverter. Reference [11] deals with troubles related to the active vector period, which is too short, which are alleviated by replacing all active vectors less than 30 μs with a zero vector and then adding the missing time in the next switching period. Serious problems arise at low modulation index, because of harmonic distortion and the poor performance of the drive at low speed [11].

In [12], an identification method (least square) is used to determine the three output currents accurately by a dc-link current sensing. The algorithm used is efficient, but again problems arise when the active switching state is too short. These current samples are excluded and the method cannot be used at low modulation index. Problems related to faults and cable influence are not discussed.

References [15] and [17] deal with the current determination for a permanent-magnet machine. In [15], it is proposed to sample the dc-link current at the center of each active vector, which gives a better current sampling. Two adjustment schemes for the duty cycles in a single-ended modulation strategy are also proposed. One is based on reducing the zero-vector time if one of the active vectors is too short. The other method uses no zero vectors when the active vectors are too short, but uses two complementary voltage vectors closest to those already used. It introduces more switchings, but information about all three output currents exists in one sampling period. In [17], the problem with a phase shift of the two samples is discussed and solved by an observer, which is also used when the time duration of the active vectors is too short. Problems arise at very low modulation index.

Recently, two methods to obtain correct output current measurements were proposed, which can work in the whole operating area of the inverter. One method consists of adjusting the duty cycles within one switching period with no voltage error between the switchings [18], while the other uses two switching periods to adjust the PWM signals [20]. It is illustrated in Fig. 7.

Both methods make it possible to operate at low speed, but the one in [20] needs a higher sample rate in order to avoid phase errors between samplings. Both approaches can easily be implemented in a microcontroller.

Few papers and patents have considered noise in the dc-link sensing including cables, but [13] proposes a method which integrates the respective current in each active switching period and then divides it with the active duration time. This gives a filtered and an average current for that vector state which also can be used when long cables are used (see Fig. 6). In this patent, a compensation of the phase shift between the two current samples is also proposed, but it needs some trigonometric calculations.

A very rarely considered practical problem is protection from all possible faults in an inverter, especially ground faults. In [14], a ground-fault detection scheme is patented based on a current sensor in the positive dc bus and a current sensor in the negative dc bus. When a zero vector is used, the current

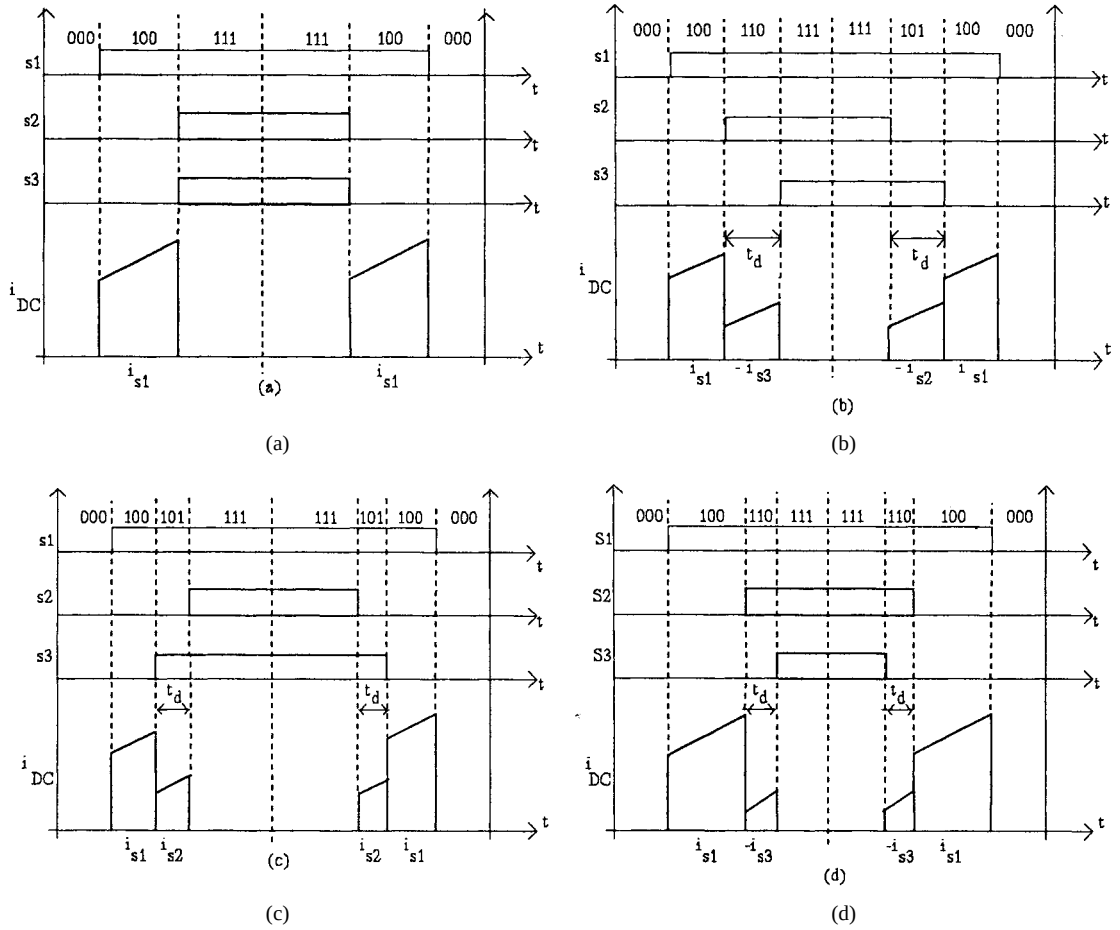


Fig. 7. PWM signals and measured dc-link current. (a) Nonmodified signals. (b) Modified signals proposed in [18]. (c) and (d) Modified signals in two switching periods proposed in [20].

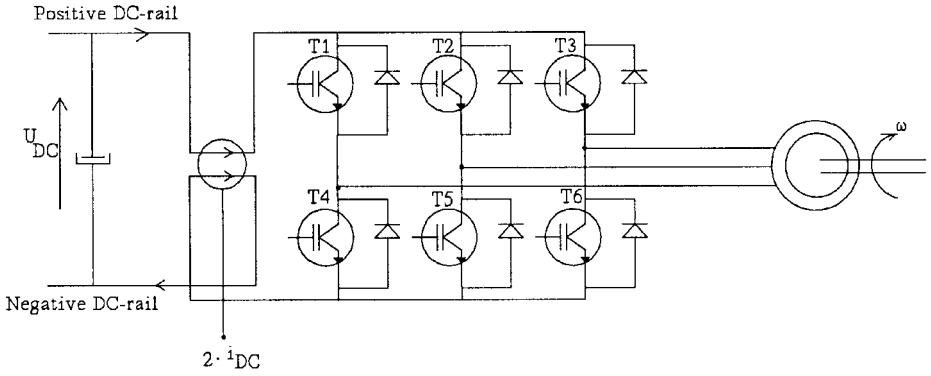


Fig. 8. Fully protected PWM–VS inverter with one current sensor, according to [19].

should be zero. An improved method, which requires only one sensor, is proposed in [19]. The topology is shown in Fig. 8.

It uses both the positive and the negative bus currents in a Hall-element current sensor. In normal situations, i_{DC} is measured twice. Any ground fault can easily be detected [19].

IV. The Proposed Solution

Review of the literature results in the conclusion that two major problems still exist. It is the phase shift of the current sensing and the requirement in [19] that the current sensor should be designed for a double current. Those problems are solved in a new topology where the last disadvantage is solved [21]. It is shown in Fig. 9.

An extra winding is added to this topology, compared with Fig. 8, and the sign of the current in the Hall-element sensor is changed. The measured current in the dc link is now

$$i_{\mathrm{DC}} = N1 \cdot i_{\mathrm{DC1}} - N2 \cdot i_{\mathrm{DC2}} \tag{4}$$

where

i_{DC} resulting dc-link current;
i_{DC1} positive dc-bus current;
i_{DC2} negative dc-bus current;

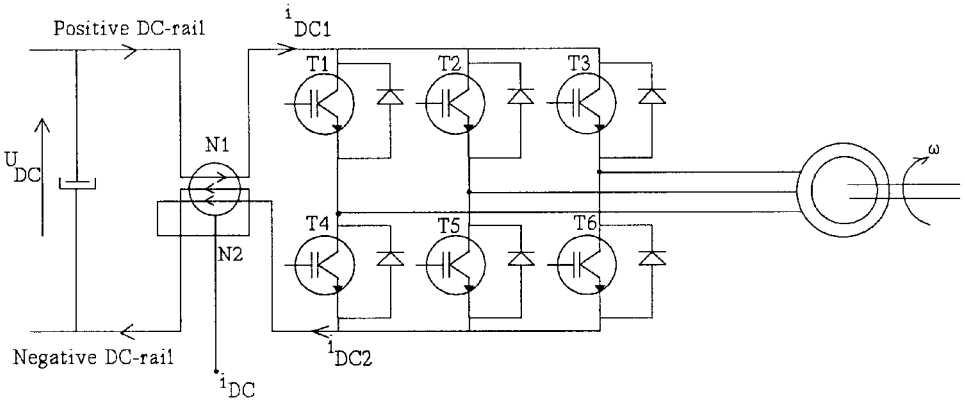


Fig. 9. Proposed diagram of a fully protected PWM–VS inverter with one current sensor.

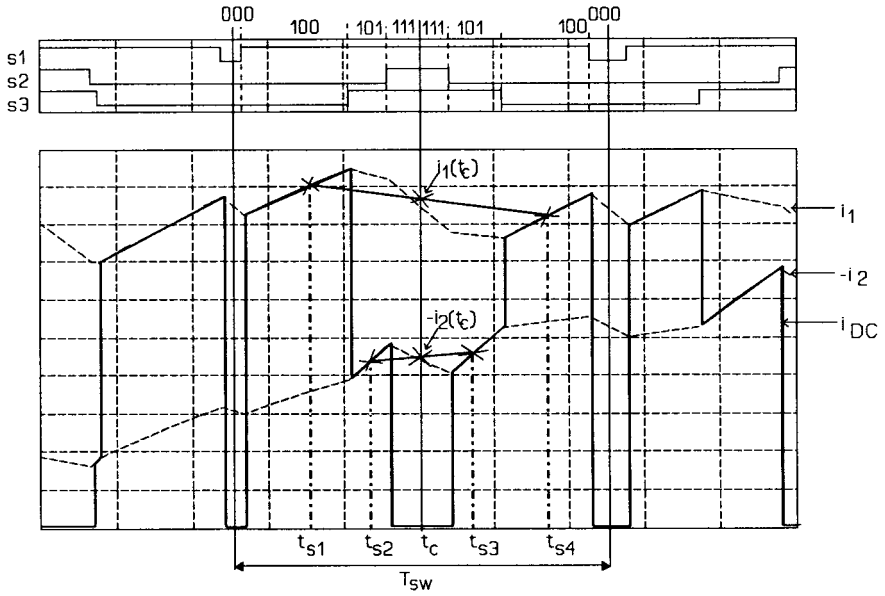


Fig. 10. Current waveforms and voltage vectors during one switching period with the new proposed sampling method.

$N1$ number of windings carrying the positive dc-bus current;

$N2$ number of windings carrying the negative dc-bus current.

If $N1 \neq N2$, the dc-link current measured will be as specified in Table I. A high resolution is obtained in the dc-link current sensing if one of the following two conditions is used:

$$N1 = N2 + 1 \tag{5}$$

or

$$N2 = N1 + 1. \tag{6}$$

A typical selection will be $N1 = 1$ and $N2 = 2$.

A new way to sample the dc-link current has been presented in [22]. The current is sampled in both the leading and the lagging part of the switching period (T_{sw}). This gives a true output current measurement without any phase delay, and it can easily be implemented into an ASIC.

During normal operation, two output current values can be recorded during a switching sequence, [see (1)]. In the switching sequence shown in (1), there are two active (nonzero) voltage vector states (100 and 110) during which the measured i_{DC} signal reflects $+i_1$ and $-i_2$, respectively. Typical current waveforms for an induction motor operating without cables during such a switching sequence are shown in Fig. 10.

Considering the ideal phase-current measurement system (i.e., all current values known all the time without delay), a closer look at Fig. 10 reveals two problems with the dc-link current measurement method. The first problem is that the two available output current signals are not present at the same time. The second problem is that the current values change quite rapidly during the active voltage-vector states where the measurements are done.

In [13], an ingenious solution for both problems has been demonstrated. During each active voltage-vector state, the dc-current signal is applied to a corresponding analog integrator. Thus, it is possible to calculate the average current value during the measurement period, avoiding the second problem mentioned. Furthermore, the timing problem is solved by using the known instants for the two measurements in combination with the known angle and the angular speed of the reference

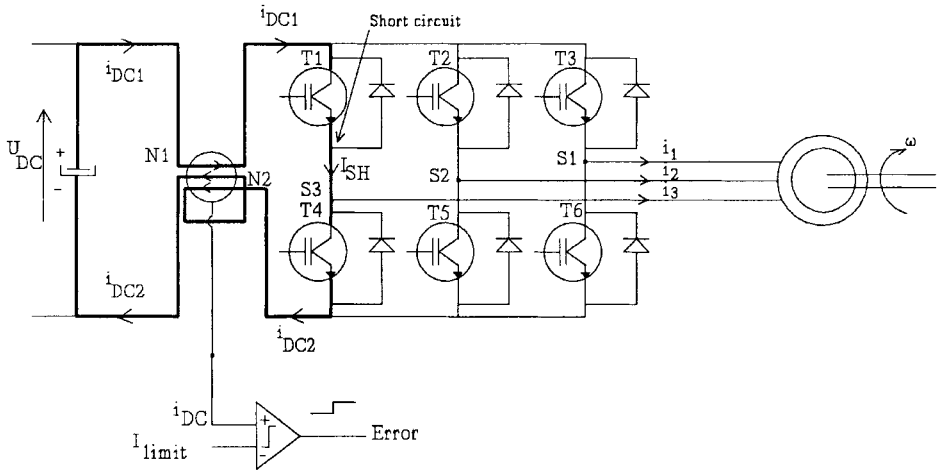


Fig. 11. Short circuit in the dc link of the inverter and its detection.

voltage vector, in order to calculate all three phase-current values.

In order to avoid analog signal processing and to reduce the amount of necessary calculations, an alternative solution is proposed here. The timing problem is solved by using the phase-current information recorded in both sides of the symmetrical switching sequence. In this way, the estimated phase-current value at time t_c in Fig. 10 can be calculated as a simple average of those two recorded values. This can be done for both the available phase-current signals, and the third phase value can be calculated again using basic arithmetic operations. All three phase-current values are estimated concurrently (referred to same time instant) and independently of the reference voltage.

In Fig. 10, the current is sampled in the center of the active vectors, and the output currents at the time instant t_c can be calculated as

$$i_1(t_c) = \frac{i_{\mathrm{DC}}(t_{s1}) + i_{\mathrm{DC}}(t_{s4})}{2} \tag{7}$$

$$i_2(t_c) = -\frac{i_{\mathrm{DC}}(t_{s2}) + i_{\mathrm{DC}}(t_{s3})}{2} \tag{8}$$

$$i_3(t_c) = -[i_1(t_c) + i_2(t_c)] \tag{9}$$

where i_1, i_2, i_3 are the phase currents and t_c is the center time of double-sided modulation.

Note that two simultaneously sampled currents are determined on the basis of four nonsimultaneously sampled dc-link currents.

The second problem (di/dt) can be solved in different ways considering the demands to the output signal, which should reflect the average value of the current signal during the actual active voltage-vector state. Disregarding analog/mixed signal processing, there are two obvious solutions based on sampling and digital signal processing. The first solution is a single sampling method where the sampling instant is adjusted to the center of the actual voltage-vector state period [19], as shown in Fig. 10. A second solution is based on oversampling, i.e., high-speed sampling with digital averaging, which is more robust with respect to noise and, thus, gives the same benefits as the analog integration method of [13] described above.

The proposed method, which basically is based on an average of one switching period, is also useful in transient conditions. All sampled signals are updated each switching period (and even to the same time instant in the center), and they can be used for all kinds of control, including field-oriented control with fast current-control loops with sampling times as low as the switching period. The only limitation in relation to traditional synchronized sampling (sampling in the zero vectors) with three current sensors is that it is not possible to operate with a current sample rate which is twice the switching frequency. In smaller drives (<10 kW) this is not a practical limitation, because higher switching frequencies are used (>4 kHz).

The current waveforms shown in Fig. 10 represent idealized conditions, i.e., cable length equal to zero and no stray capacitance in the load.

V. Fault Situations

Various fault situations can appear in an inverter, and they are discussed for the proposed topology.

A. Short Circuit of DC Link

The first fault situation is a short circuit in the dc link when two transistors are on at the same time (shoot-through). Some faults in the control electronics can be the reason for such a fault. The proposed topology protects against such a fault, and Fig. 11 shows a case when $T1$ and $T4$ are on at the same time.

A short-circuit current I_{SH} will be measured by the current sensor ($i_{\mathrm{DC}} = I_{\mathrm{SH}}$) and, if I_{SH} exceeds a given current limit I_{limit}, an error signal can be generated by a comparator. The inverter will then be turned off. The same type of faults will be present when $T2$ and $T5$ are on or $T3$ and $T6$ are on simultaneously.

B. Short Circuit of Two Output Phases

The second fault situation is when two output phases are shorted. Fig. 12 shows when $S2$ and $S3$ are shorted accidentally.

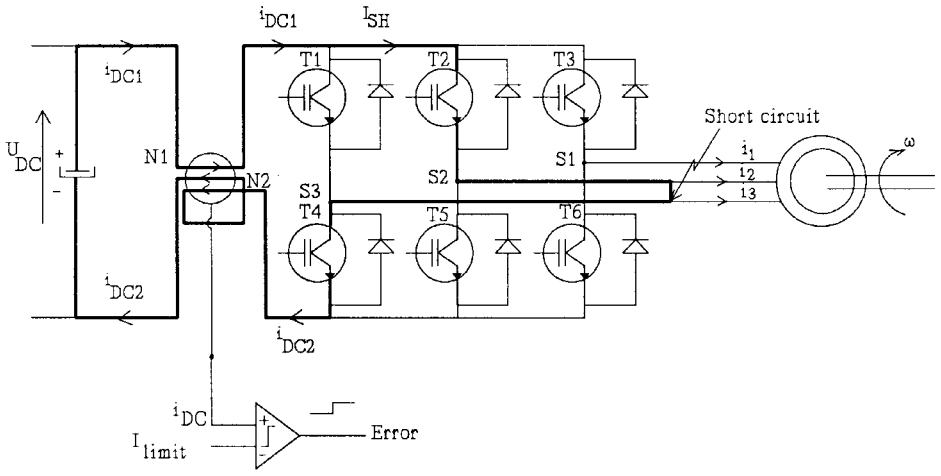


Fig. 12. Short circuit of two output phases of the inverter and its detection.

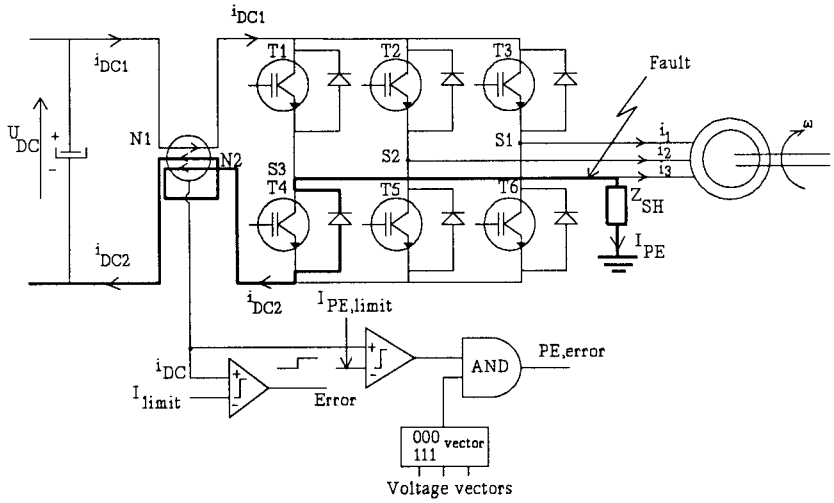


Fig. 13. Ground or earth fault in the inverter and its detection.

Again, a short-circuit current $I_{\rm SH}$ will flow in the circuit and be measured by the current sensor ($i_{\rm DC} = I_{\rm SH}$). The current rise will only be limited by the inductance in the circuit. If the measured current exceeds a maximum current $I_{\rm limit}$, an error signal will be generated by a comparator, and the inverter will be turned off.

C. Ground or Earth Faults

The third fault situation is when one of the phases has connection to earth or to ground. This situation is normally the most difficult to detect because two kinds of faults exist. Fig. 13 illustrates an earth fault for phase $S3$.

If the connection has a low impedance, a high ground current $I_{\rm PE}$ will be present and measured by the current sensor. When the current $i_{\rm DC}$ exceeds $I_{\rm limit}$ ($i_{\rm DC} = N1 \cdot I_{\rm PE}$ or $i_{\rm DC} = N2 \cdot I_{\rm PE}$), an error will be generated by a comparator. If the ground connection has a relatively high impedance, the current will normally never exceed $I_{\rm limit}$. However, an earth fault can be detected when the inverter uses a zero vector (000 or 111), because, in that case, normally no current should be measured by the current sensor. An extra comparator combined with the switch-vector states can now detect such errors. A low current limit $I_{\rm PE,\,limit}$ is introduced for that purpose. A second error (PE, $error$) can be generated. This error will, in many cases, not require an instantaneous shutdown of the inverter, but the whole system can run down and give an error message.

VI. Implementation

The current-sensing technique and protection scheme are implemented in a microcontroller and some extra logic circuits. A 16-b microcontroller, SIEMENS SAB80C166, is used as modulator and as control for the current sensing, because it has special capture/compare registers. The logic circuit performs the protection. Fig. 14 shows the implementation of modulation and the current sensing techniques in the microcontroller.

The modulation is straightforward with a lookup table. If the voltage-vector duration is too small, a duty-cycle correction is done as proposed in [18], and this adjustment should be significant to avoid the cable influence. In Fig. 14, it is labeled as "Adjustment of TCL." A double-sided modulation strategy is used where the dc-link current is sampled six

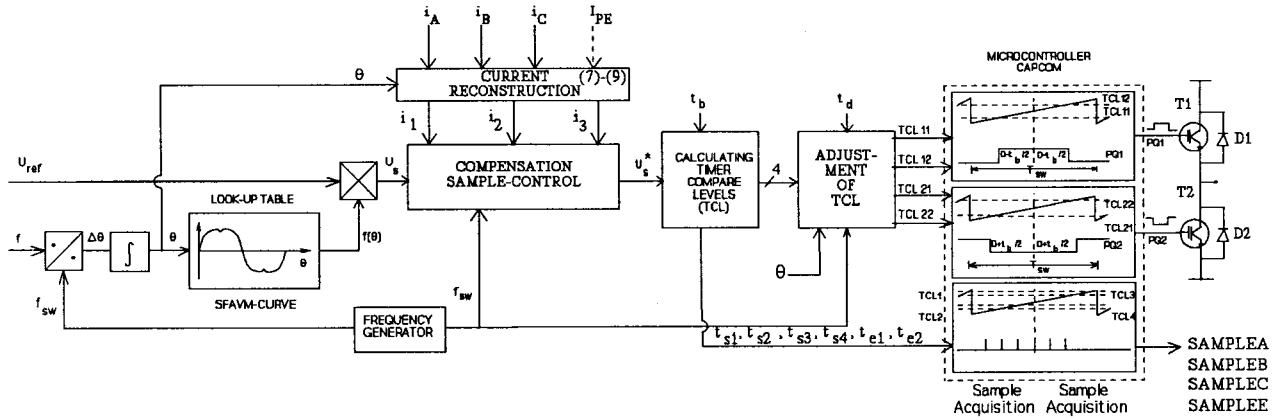


Fig. 14. Implementation of modulation and sampling technique in a microcontroller.

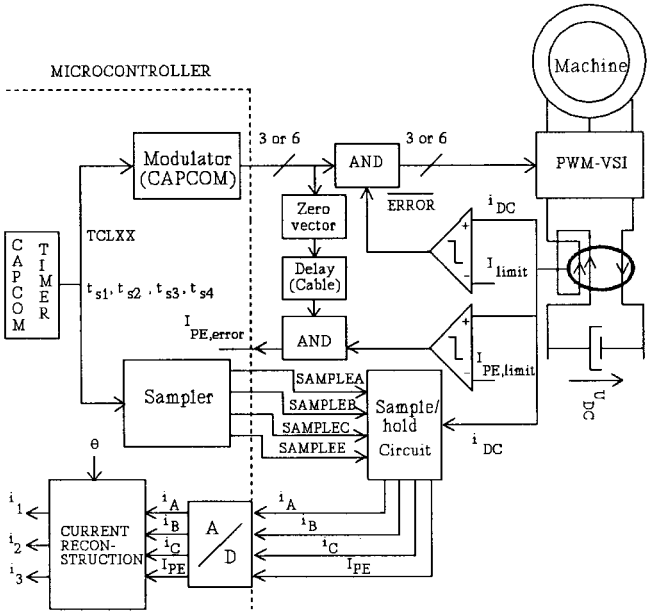


Fig. 15. Realization of current-sampling technique and protection.

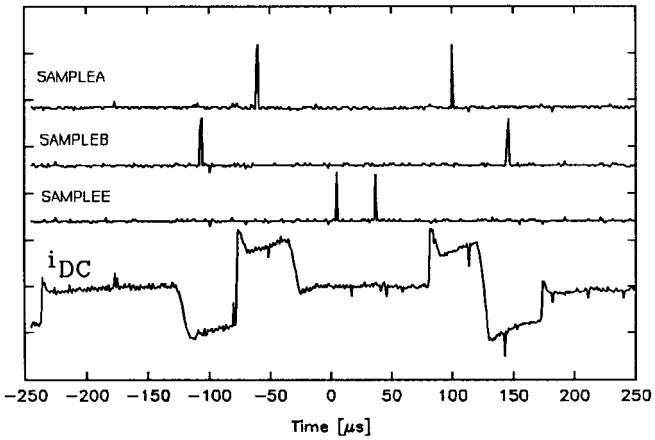


Fig. 16. Measured dc-link current and sample signals from the microcontroller.

times in each switching period, two times the active voltage vectors ($t_{s1} - t_{s4}$) and the zero vector (t_{e1}, t_{e2}). The microcontroller also controls the sampling time of the dc-link current [19] by four compare registers which are synchronized with a CAPCOM timer that controls the modulation. The acquisition of the dc-link current is performed by a four-channel sample–hold circuit, and the integrated A/D converter in the microcontroller converts the sampled currents. Three signals ($SAMPLEA$, $SAMPLEB$, $SAMPLEC$) are necessary for output currents and a fourth channel ($SAMPLEE$) is used to detect the level of the high impedance earth fault, in order to determine how fast the system should be closed down. Three currents are sampled in each half switching period (e.g., i_A, i_B, and $i_{\rm PE}$). After one switching period, the currents (i_1, i_2, i_3) can be calculated according to (7)–(9) at the time instant t_c in the "Current Reconstruction" shown in Fig. 14. $I_{\rm PE}$ is only used for monitoring, and it is the parameter for closing down the system. Fig. 15 shows the practical realization of the complete technique. In some cases, it is possible to use $SAMPLEA$, $SAMPLEB$, or $SAMPLEC$ for earth-current measurement, because only two samples in active vectors are necessary during half a switching period.

The two current-limit detectors are implemented as comparators where the high current detector shuts down the modulator and inverter immediately, while the low earth-current detector generates an error to the microcontroller, which can sample the actual current if it has not done so already. A delay circuit, which takes into account the influence of the cable, is inserted between the zero-vector detector and an AND circuit in order to obtain a reliable detection of the current. A minimum zero-vector time is, therefore, necessary. The zero-vector detector can also be controlled digitally by the microcontroller using the $SAMPLEE$ signal, which is active during the zero vector and the zero-vector current can be monitored continuously.

It is chosen, in this case, to use a microcontroller solution which needs to have a fast A/D converter. It samples the current six times in a switching period. The microcontroller system is also somehow burdened with a number of calculations to do the sampling, but it is a flexible system. If the switching frequency is increased five times or more, a faster A/D converter is necessary or the sampling frequency of the current is reduced with respect to the switching frequency. In many applications, sample frequencies of the current higher

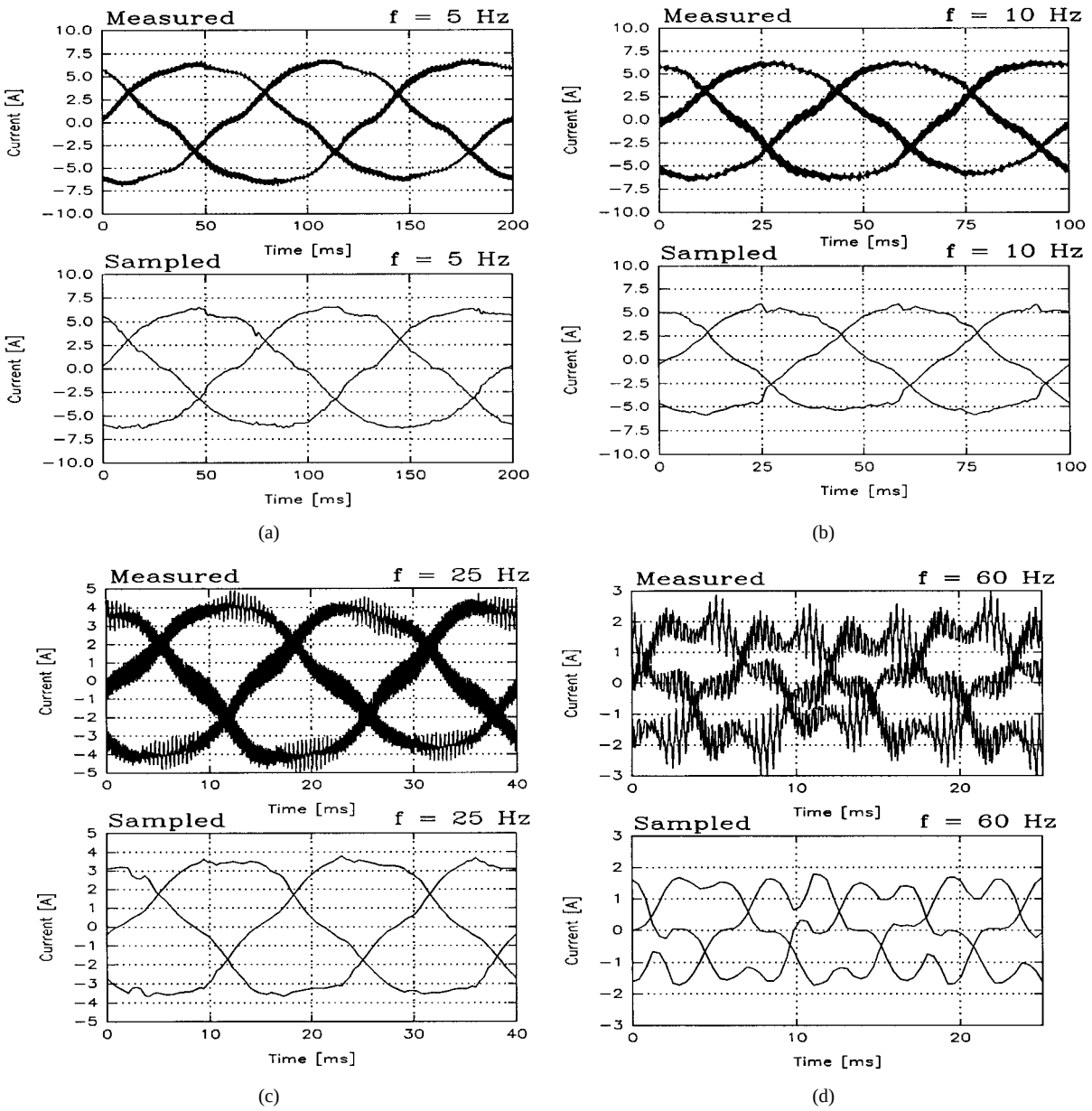


Fig. 17. Measured and estimated (sampled) output currents. (a) $f = 5$ Hz. (b) $f = 10$ Hz. (c) $f = 25$ Hz. (d) $f = 60$ Hz.

than 5 kHz are not necessary. An alternative is an ASIC chip, which has the advantage of performing dedicated hardware functions which can significantly reduce the load of the microcontroller. The disadvantages are higher initial cost and less flexibility. In a final industrial implementation, an ASIC solution would be preferred [22]. Another problem with higher switching frequencies is the load of the inverter when a long cable is used. The charging/discharging current in each switching is almost the same (see Fig. 6). Five times higher switching frequency will give five times higher cable currents, which should be provided by the inverter. A small inverter will get significant extra losses with long cables, because the cable currents are almost equal in the power range of 1–25 kW. The earth current will also be increased. Finally, the real switching frequency in the inverter is normally only one half of the frequency the load meets, because a double-sided modulation strategy is used [23].

A practical problem, which also has to be taken into account in a final design, is the number of necessary windings in the Hall-element sensor in order to use a specific Hall-element in its whole operating area. For small inverters, this results in more than ten windings (in an LEM module), which gives some demands to the manufacturing, and it can be expensive to build. Also, more inductances are introduced in the commutation circuit between the dc-link capacitor and the power transistors.

VII. Test Results

Various test results for a PWM–VS inverter which controls an induction motor are shown. The power rating is 1.5 kVA, $0 \rightarrow 8$ A, $0 \rightarrow 240$ V. The switching frequency is 2.4 kHz. The blanking time is 3.2 μs. A three-phase rectifier diode bridge is used as a supply for the inverter.

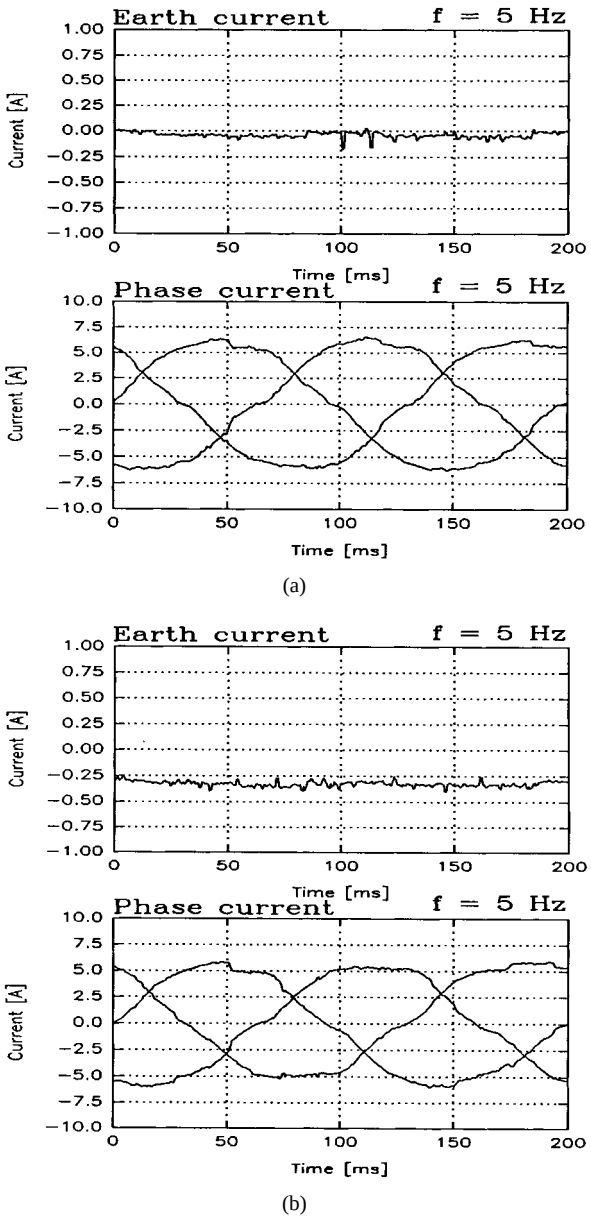


Fig. 18. Detection of earth fault in inverter at 5-Hz operation. (a) Without any fault. (b) With an earth fault.

The used minimum delay time is 10 μs, in order to ensure proper sampling. This can easily be extended to 20 μs or more if very long cables are used. Fig. 16 shows the dc-link current and the three sampling signals.

It can be seen that the two phase currents are sampled at the center of the active vector and the earth current is sampled at the zero vector, when no current normally is present in the dc link.

Fig. 17 shows the comparison between measured and estimated output currents for the three phases.

Fig. 17 shows that it is possible to estimate the output currents correctly at different fundamental frequencies. Small disturbances exist in the currents, due to the adjustment of duty cycles. At 60-Hz operation, the current waveforms (both measured and sampled) are disturbed because of the overmodulation and the 300-Hz component in the dc link. No compensation is done, but the currents are very well recreated.

The final test involves detection of a small earth fault. Fig. 18 shows the estimated currents and the earth-fault current with and without a fault. A resistance of 200 Ω is used to make the earth-fault connection.

Fig. 18 shows it is possible to detect an earth current of 0.25 A by sampling the dc-link current at the zero-voltage vectors. If no faults exist, the sampled current is about zero.

VIII. Conclusion

The output currents in a three-phase PWM–VS inverter can be recreated from the current information in the dc link accurately using a circuit topology presented in this paper. The inverter is protected against all possible faults by using a special winding technique in the dc link with a Hall-effect current sensor. Also, a new and very efficient current-sampling technique is proposed, where true information about the phase current is obtained without any phase shift.

Various problems are solved by adjusting the modulation in the three phases when one active voltage vector is used for a very short time and when the inverter operates in the overmodulation range. All short-circuit possibilities are discussed and it is concluded that the topology is easy to implement. Finally, test results show that the topology works under all operating conditions, and different faults in the inverter can effectively be detected.

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Frede Blaabjerg (S'86–M'91) was born in Erslev, Denmark, in 1963. He received the M.Sc.E.E. degree from Aalborg University, Aalborg, Denmark, in 1987 and the Ph.D. degree from the Institute of Energy Technology, Aalborg University, in 1995.

He was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. He became an Assistant Professor in 1992 at Aalborg University where, in 1996, he became an Associate Professor. His research areas include power electronics, static power converters, ac drives, switched reluctance drives, modeling, characterization of power semiconductor devices, and simulation.

Dr. Blaabjerg is a member of the European Power Electronics and Drives Association and the IEEE Industry Applications Society Industrial Drives Committee. He received the 1995 Angelos Award for his contribution in the areas of modulation technique and control of electric drives and the Annual Teacher Prize from Aalborg University.

John K. Pedersen (M'91) was born in Holstebro, Denmark, in 1959. He received the B.Sc.E.E. degree from Aalborg University, Aalborg, Denmark.

He joined the Institute of Energy Technology, Aalborg University, as a Teaching Assistant in 1983. He was an Assistant Professor from 1984 to 1989 and has been an Associate Professor since 1989. He is also currently the Head of the Institute of Energy Technology. His research areas include power electronics, power converters, and electrical drive systems, including modeling, simulation, and design, with focus on optimized efficiency.

Mr. Pedersen received the 1992 Angelos Award for his contribution in the area of control of induction machines.

Ulrik Jaeger received the B.Sc.E.E. degree from Odense Teknikum, Odense, Denmark, in 1984.

He was with Danfoss A/S, Nordborg, Denmark, from 1984 to 1987. From 1987 to 1988, he was employed at Fyensvaerket (a power station) in Denmark. Since 1988, he has been with the Transmission Division, Danfoss Drives A/S, Graasten, Denmark, as a Research Engineer. His research areas include power components, static converter topologies, and simulation on different levels.

Paul Thoegersen (M'92) was born in Thy, Denmark, in 1959. He received the M.Sc.E.E. degree from Aalborg University, Aalborg, Denmark, in 1984 and the Ph.D. degree from the Institute of Energy Technology, Aalborg University, in 1989.

He was an Assistant Professor at Aalborg University from 1988 to 1991. Since 1991, he has been with the Transmission Division, Danfoss Drives A/S, Graasten, Denmark, as a Research and Development Engineer. His research areas include frequency converters and control and simulation of ac drives.

Dr. Thoegersen is a member of the European Power Electronics and Drives Association and a member of the IEEE Industry Applications, IEEE Power Electronics, and IEEE Industrial Electronics Societies.