



EE213
Digital Integrated Circuits II
Lab1

Please start the lab **as soon as possible** since you need to get familiar with the tools

Deadline: 2022/9/25 24:00





Outline

1. Familiar with Virtual Desktop
   - login
   - Virtuoso
   - Hspice
2. Schematic and Layout Design Part
3. Simulation Part





Login Virtual Desktop

1. Enter the website: vd.shanghaitech.edu.cn
2. Choose to download the client or connect through the web(client is recommended)
3. Open client, add server: vd.shanghaitech.edu.cn
4. Login with your account. User name: [email prefix]
   Password:[email password]
5. Click virtual desktop, then choose ‘centos’, password: [szjcdl@2022]



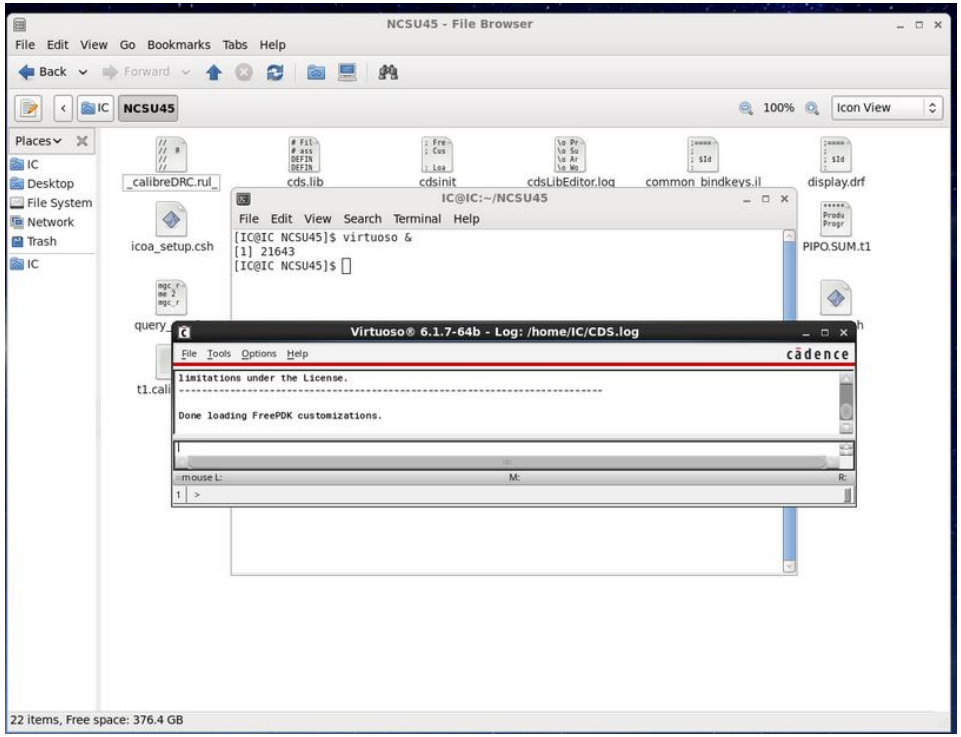


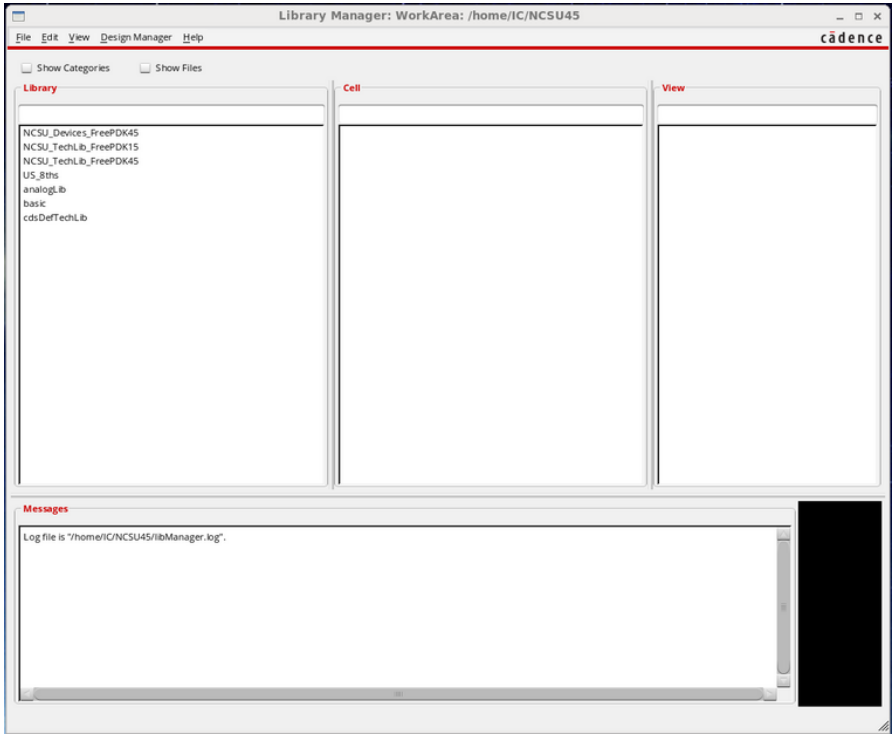
Run Virtuoso

1. Open the folder /Home/EE213
2. Right-click in the blank space >> Open in terminal
3. In terminal, key in: virtuoso &
4. Create libraries for 15nm or 45nm PDK respectively, you can choose any name you want, choose 'Attach to an existing technology libraries' and choose 'FreePDK' corresponding to the library node

Note: Future work will be based on the previous modules you designed

Run Virtuoso in the virtual machine









Run Hspice and check the waveform

1.Open a terminal and enter the directory where your spice files are.

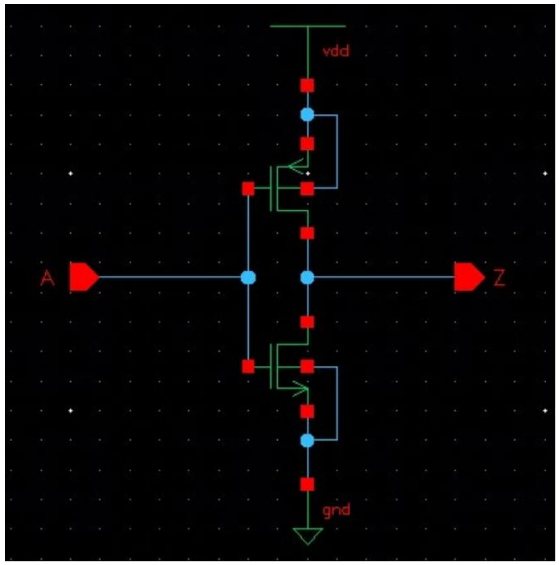
2. Input ‘hspice –i filename.sp –o outfilename(if you want to know more about hsipce, you can only input hspice or find in the Internet)

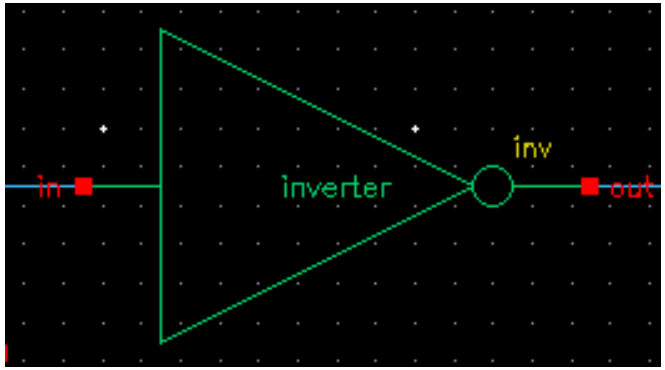
3. After completing the simulation of spice, input ‘wv &’, it will have a GUI for WaveView, you can check .tr0 or .st0 in it.

Task 1.1: A schematic of an inverter and an inverter symbol for 15nm(schematic)

1. Read the tutorial (ade_hspice_tut) to draw a schematic and symbol: http://pan.shanghaitech.edu.cn/cloudservice/outerLink/decode?c3Vnb24xNjYyNzEyOTA3NTg4c3Vnb24=

   (Check the step: 'Create Symbol from Cellview')









Task 1.2: A test schematic of an inverter and export the netlist for 15nm(testbench)

1. Read the tutorial(ade_hspice_tut) to draw a test schematic and generate netlist: http://pan.shanghaitech.edu.cn/cloudservice/outerLink/decode?c3Vnb24xNjYyNzEyOTA3NTg4c3Vnb24=
2. Select Outputs->To Be Plotted-> Select On Design and choose the input/output where you need to watch the wave.
3. Select Simulation-> Netlist->Create to generate the netlist, and save it as an .sp file.

Notice: Don't click the run button! Instead, open the netlist file and modify it if necessary. Then run hspice as page 6 of this ppt shows.

Other details: search the website on your own.

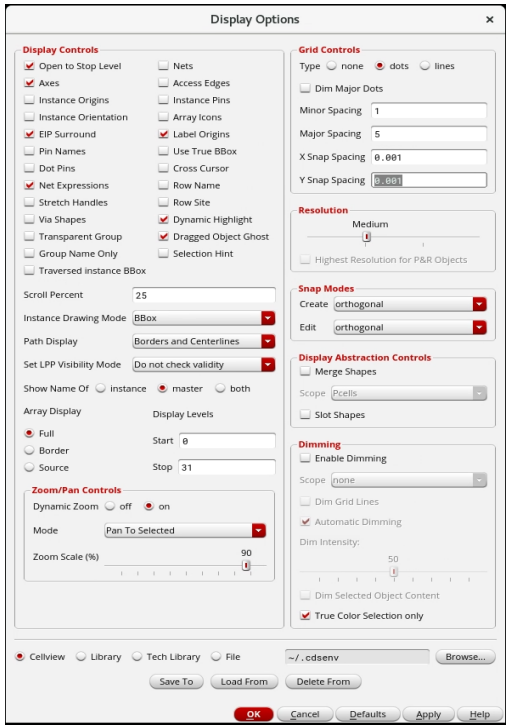




Task 1.3: Create a layout design for 15nm

1. Read the tutorial(layout_tut1) to draw a layout and run DRC check: http://pan.shanghaitech.edu.cn/cloudservice/outerLink/decode?c3Vnb24xNjYyNzEyOTA3NTg4c3Vnb24=
2. Read the tutorial(layout_tut2) to run LVS and extract parasitic(PEX)

Note1: The tutorial (layout_tut2) is nand, you only need to refer the setups of LVS and PEX.
Note2: Before drawing the layout, you should change the value of the nodes. Select Options->Display->Defaults->X nap spacing 0.001, Y nap spacing 0.001.



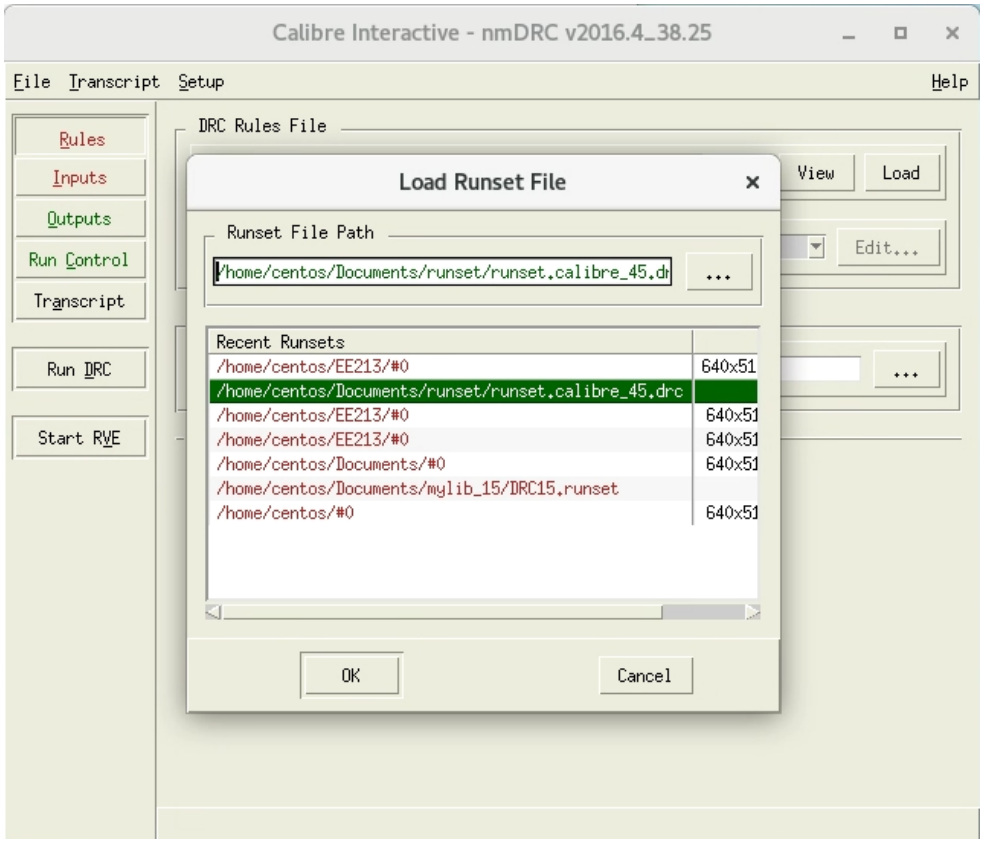
DRC/LVS/PEX rules used in Virtuoso

When run DRC/LVS/PEX of 15nm and 45nm, load the runset file in corresponding directory.

Note: You can find some DRC rule in this website if you need.

15nm: FreePDK Design Rules http://pan.shanghaitech.edu.cn/cloudservice/outerLink/decode?c3Vnb24xNjYyNzEyOTA3NTg4c3Vnb24=

45nm: FreePDK45 | NC State EDA (ncsu.edu)

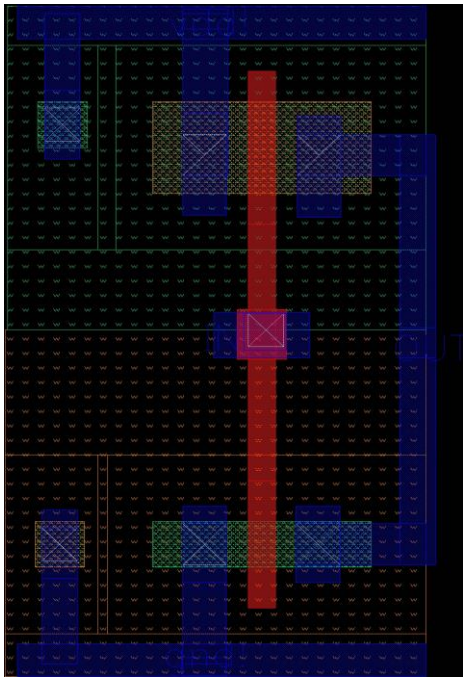


Task 2: Create schematic and layout according to schematic with 45nm PDK

The flow is the same as 15nm PDK:

Task 2.1: a schematic of an inverter, an inverter symbol (schematic)
Task 2.2: a test schematic of an inverter and export the netlist (testbench)
Task 2.3: draw the layout and minimize 45nm inverter size & DRC and LVS pass & PEX with calibre (layout)

Note: You need to draw the layout of the single NMOS/PMOS by yourself. One NMOS will be made of nwell, pimplant, active, contact, metal1 and poly; PMOS will be made of pwell, nimplant, active, contact, metal1 and poly.







Task 3: Simulation according to schematic & layout

Please simulate your netlists in Hspice.
The transistor models used in this lab (You need to include them in your SPICE file):
15nm: /Home/PDK/FreePDK15/hspice/models/fet.inc (you should change '.LIB CGM' to '*.LIB CGM' , 'pfet' to 'pmos' and 'nfet' to 'nmos')
45nm:/Home/PDK/FreePDK45/ncsu_basekit/models/hspice/tram_models/NMOS_VTL ,PMOS_VTL

Task 3.1: Simulation according to your netlist(generated by task1.2 and task 2.2) for Schematic.
Task 3.2: Simulation according to your xxx.pex.netlist for Layout.

Note: In task1.3 and task2.3, you have generated the parasitic parameters in xxx.pex.netlist, xxx.pex.netlist.pex and xxx.pex.netlist.xxx.pxi and you can find them in EE213(or you set path). You should complete the xxx.pex.netlist file to simulate.





Requirements of submission

Your report should cover the images of the following content:

1. The test schematic of the inverter(15nm&45nm).
2. The layout of the inverter (15nm&45nm). Several key DRC rules should be reflected in your diagram(by ruler).
3. Diagrams of DRC, LVS, and PEX pass.
4. The simulation results of schematic and layout (15nm&45nm).

Notice: you should try to minimize the area as much as possible.





Requirements of submission

Your source file package should include the following content:

1. Library files of your design in Virtuoso.
2. Generated netlist with extract parasitic.
3. Hspice simulation output files.





How to submit?

- Upload your report onto Blackboard

- Submit the source file package to this link:
http://pan.shanghaitech.edu.cn/cloudservice/outerLink/decode?c3Vnb24xNjYyNzgzMjk0MTA0c3Vnb24=

Title of your report and package should be:

EE213 Lab1 + your ID + your Name