Submission:

Please submit a PDF version of your answers via Blackboard. A scanning version of the handwriting is allowed, but your scanned image needs to be clear enough.

Rules:

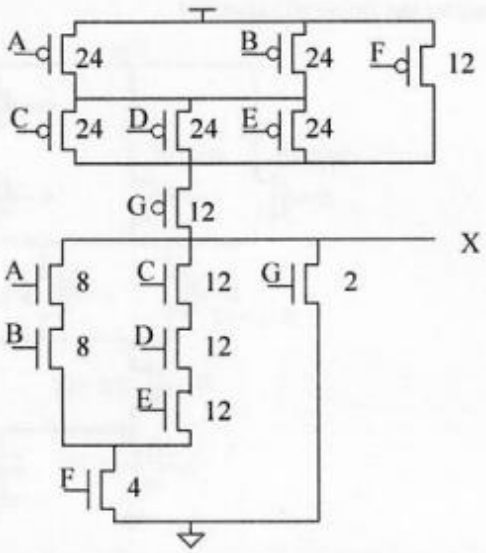
- Please try to work on your own. Discussion is permissible, but identical submissions are unacceptable!
- Please show all intermediate steps: a correct solution without an explanation will get zero credit.
- Please submit on time. Late submission will NOT be accepted.
- Please prepare your submission in English only. No Chinese submission will be accepted.

1. Implement the equation $X = ((\overline{A} + \overline{B})(\overline{C} + \overline{D} + \overline{E}) + \overline{F})\ \overline{G}$ using complementary CMOS. Size the devices so that the output resistance is the same as that of an inverter with an NMOS *W/L* = 2 and PMOS *W/L* = 6. Which input pattern(s) would give the worst and best equivalent pull-up or pull-down resistance? [8 pts]
(Hint: All the input signal should be like A, B, C, D, E and etc….)

1. [E, None, 4.2] Implement the equation $X = ((\overline{A} + \overline{B})(\overline{C} + \overline{D} + \overline{E}) + \overline{F})\,\overline{G}$ using complementary CMOS. Size the devices so that the output resistance is the same as that of an inverter with an NMOS $W/L = 2$ and PMOS $W/L = 6$. Which input pattern(s) would give the worst and best equivalent pull-up or pull-down resistance?

Solution

Rewriting the output expression in the form $X = ((\overline{A} + \overline{B})(\overline{C} + \overline{D} + \overline{E}) + \overline{F})\,\overline{G} = \overline{((AB + CDE)F) + G}$ allows us to build the pulldown network by inspection (parallel devices implement an OR, and series devices implement an AND). The pullup network is the dual of the pulldown network.



The plot shows sizes that meet the requirement - in the worst case, the output resistance of the circuit matches the output resistance of an inverter with NMOS W/L=2 and PMOS W/L=6.

The worst case pull-up resistance occurs whenever a single path exists from the output node to Vdd. Examples of vectors for the worst case are ABCDEFG=1111100 and 0101110. The best case pull-up resistance occurs when ABCDEFG=0000000.

The worst case pull-down resistance occurs whenever a single path exists from the output node to GND. Examples of vectors for the worst case are ABCDEFG=0000001 and 0011110.

The best case pull-down resistance occurs when ABCDEFG=1111111.

2. CMOS Logic (The parameters used in calculation are shared in all sub-questions)[21 pts]
   a) Do the following two circuits (Figure 1) implement the same logic function? If yes, what is that logic function? If no, give Boolean expressions for both circuits. [3 pts]
   b) Assuming we can ignore all second order effects, do these circuits have the same output resistances when driven with the same input patterns? [3 pts]
   c) Assume the transistors have been sized to give a worst case output resistance of 13kΩ for the worst case input pattern. What input patterns(A-E) give the lowest output resistance when the output is low? What is the value of that resistance? [3 pts]
   d) What input patterns(A-E) give the lowest output resistance when the output is high? What is the value of that resistance? [3 pts]
   e) Neglecting parasitics and assuming a load capacitance of 100fF, find the best and the worst case t_{phl} and t_{plh}. [3 pts]
   f) Now consider a few second order effects on propagation delays. Which circuit is optimized for the case when it is known a priori that E will be the last input to arrive and why? How will body effect influence the performance of Circuit A vs. Circuit B? [3 pts]
   g) Consider only Circuit B. Each intermediate node has some parasitic capacitance that must be charged and discharged at each transition. Therefore, the propagation delay is a function of both the initial voltage conditions on the internal nodes and inputs. The initial voltage conditions, however, are determined by the previous inputs. Which set of previous and current inputs will cause the slowest t_{plh}? Which will cause the slowest t_{phl}? [3 pts]

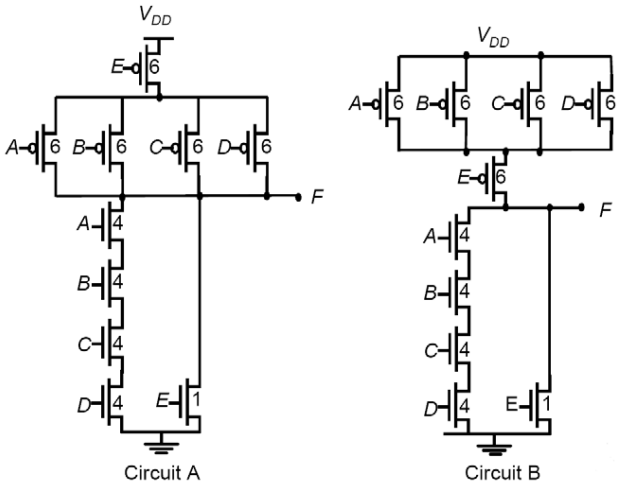


Figure 1. 2 Static CMOS Circuits

a) Do the two circuits in Figure 0.1 implement the same logic function? If yes, what is that logic function? If no, give Boolean expressions for both circuits.

Solution

Yes, they implement the same logic function : $F = (\overline{ABCD + E}) = (\overline{A} + \overline{B} + \overline{C} + \overline{D}).\overline{E}$

b) Assuming we can ignore all second order effects, do these two circuits have the same output resistances when driven with the same input patterns?

Solution

Yes, they do. The pull down networks are identical and the pull up network can be found by inspection to have the same resistances given the same input pattern.

c) Assume the transistors have been sized to give a worst case output resistance of 13 kΩ for the worst-case input pattern. What input patterns (*A–E*) give the lowest output resistance when the output is low? What is the value of that resistance?

Solution

The lowest output resistance is obtained when all inputs (A, B, C, D and E) are equal to 1. In that case, the output resistance is the parallel of the resistance of a NMOS of width 1, with a series of four equal nMOS of width 4. Both combinations have the same resistance, equal to the worst-case output resistance, 13 $k\Omega$. Then the output resistance, in this case, is half this value, 6.5 $k\Omega$.

d) What input patterns (*A–E*) give the lowest output resistance when the output is high? What is the value of that resistance?

Solution

The lowest output resistance is obtained when all inputs are equal to zero. Each of the PMOS have the same width, so all of them have the same resistance. The worst case resistance happens when only one of the inputs (A, B, C or D) is equal to 0 while all the rest are equal to 1. The output resistance in that case is the series of the resistance of two of the PMOS and it is equal to 13 $k\Omega$. Then, each of the pMOS has an output resistance equal to 6.5 $k\Omega$. The output resistance is equal to the series of one of these resistance with the parallel of four of the same resistnaces. Then, the minimum output resistance is 6.5 $k\Omega$ + 6.5 $k\Omega$ /4 = 8.125 $k\Omega$.

e) Neglecting parasitics and assuming a load capacitance of 100 fF, find the best case and worst case t_{plh} and t_{phl}.

Solution

We can use the RC time constant method of $t=0.69*R_{eq}*C_L$. For the worst case, R=13 K for both pull-up and pull-down and the t_{plh} and t_{phl} are both equal to 0.9 ns. For the best case tphl we know that R=6.5 K so t_{phl}=0.45 ns. For the best case t_{plh} we know that R=8.125 K so t_{plh}=0.56 ns.

f) Now consider a few second order effects on the propagation delays. Which circuit is optimized for the case when it is known a priori that E will be the last input to arrive and why? How will body effect influence the performance of Circut A vs. Circut B?

Solution

Circuit B is optimized for the case when ‘E’ will arrive last. The only difference between the two circuits is the pull up network. The nodes between (ABCD) and (E) can use the time before E arrives to charge up to VDD therefore reducing the time required for the overal circuit to charge after E does arrive. Circuit B is also preferable due to the lower influence of body effect. All four parallel devices in Circuit A may experience an increase in threshold voltage and consequent decrease in drive strength due to body effect.

g) For parts g and h, consider only Circuit B. Each intermediate node has some parasitic capacitance that must be charged and discharged at each transition. Therefore, the propagation delay is a function of both the initial voltage conditions on the internal nodes and the inputs. The inital voltage conditions, however, are determined by the previous inputs. Which set of previous and current inputs will cause the slowest t_{plh}? Which will cause the slowest t_{phl}?

Solution

For the worst case low-to-high output transition, all internal caps should initially be discharged to ground which gives a worst case previous input of[ABCDE]=[11110]. Then, the following input should leave all of those capacitances exposed to the output node so [ABCDE]=[11100]. For the high-to-low transition, we should have [ABCDE]=[11100] as the previous input to charge up the internal nodes, then [ABCDE]=[11110] to discharge through a single path only.

3. Consider the complex gate in Figure 2: [12 pts]
   a) Draw the truth table and determine the logic function of the complex gate shown in Fig. 2. [3 pts]
   b) Size the transistors such that the worst-case drive strength for all inputs is the same as a unit inverter (PMOS to NMOS ratio is 2:1). What is logical effort of this gate for each input (A,$\bar{A}$,B,$\bar{B}$)? [4 pts]
   c) Suppose we are only interested in the delay of the falling output transition when input A is pulled high and B is pulled low. Size the transistor M1 and M2 to make the logical effort of this gate for the input A the same as a unit inverter. For transistors M3-M8, use the sizes you found in (b). (5 pts)

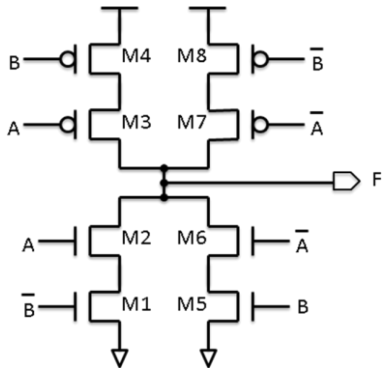


Figure 2.

(a) Draw the truth table and determine the logic function of the complex gate shown in Fig. 2. (10 pts)

Solution:

A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

This is an XNOR gate. (10 pts)

(b) Size the transistors such that the worst-case drive strength for all inputs is the same as a unit inverter (PMOS to NMOS ratio is 2/1). What is logical effort of this gate for each input ($A, \bar{A}, B, \bar{B}$)? (10 pts)

Solution:

M1=M2=M5=M6=2 (1 pts)

M3=M4=M7=M8=4 (1 pts)

$LE_A = (2+4)/3 = 2$ (2 pts)

$LE_B = (2+4)/3 = 2$ (2 pts)

$LE_{\bar{A}} = (2+4)/3 = 2$ (2 pts)

$LE_{\bar{B}} = (2+4)/3 = 2$ (2 pts)

(c) Suppose we are only interested in the delay of the falling output transition when input A is pulled high and input B is pulled low. Size the transistor M1 and M2 to make the logical effort of this gate for the input A the same as a unit inverter. For transistors M3-M8, use the sizes you found in (b). (10 pts)

Solution:

$$LE_A = \left(\frac{\left(\frac{2}{M2}\right) \times (4+M2)}{1 \times 3} \right) = 1 \quad \text{(5 pts)}$$

$\Rightarrow M2 = 8$ (3 pts)

$M2 = M1 = 8$ (2 pts)

4. Consider the circuit below: [16 pts]
   a) What is the logic function implemented by the CMOS transistor network in Fig. 3? Size the NMOS and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS W/L = 4 and PMOS W/L = 8. [4 pts]
   b) What are the input patterns that give the worst case t_{pHL} and t_{pLH}. State clearly what the initial input patterns are and which input(s) has to make a transition in order to achieve this maximum propagation delay. Consider the effect of the capacitances at the internal nodes. [4 pts]
   c) If P(A=1)=0.5, P(B=1)=0.2, P(C=1)=0.3 and P(D=1)=1, determine the power dissipation in the logic gate. Assume V_{dd}=2.5V, C_{out}=30fF and f_{clk}=250MHz. [8 pts]

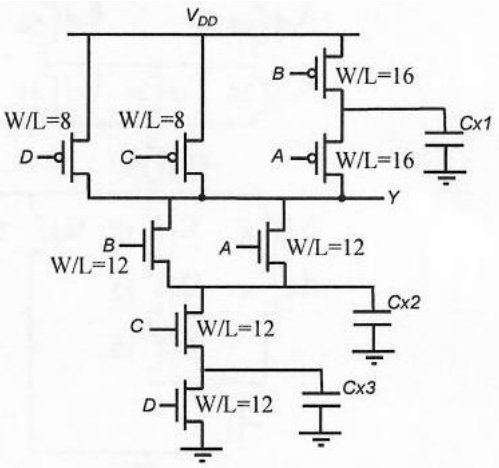


Figure 6.1 CMOS combinational logic gate.

a. What is the logic function implemented by the CMOS transistor network? Size the NMOS and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS $W/L = 4$ and PMOS $W/L = 8$.

Solution

The logic function is : $Y = \overline{(A+B)CD}$. The transistor sizes are given in the figure above.

b. What are the input patterns that give the worst case t_{pHL} and t_{pLH}. State clearly what are the initial input patterns and which input(s) has to make a transition in order to achieve this maximum propagation delay. Consider the effect of the capacitances at the internal nodes.

Solution

The worst case t_{pHL} happens when the internal node capacitances (*Cx2* and *Cx3*) are charged before the high to low transition. The initial states that can cause this are: ABCD=[1010, 1110, 0110]. The final state is one of: ABCD=[1011, 0111].

The worst case t_{pLH} happens when *Cx1* is charged before the low to high transition. The input pattern that can cause this is: ABCD=[0111] =>[0011].

c. If P(A=1)=0.5, P(B=1)=0.2, P(C=1)=0.3 and P(D=1)=1, determine the power dissipation in the logic gate. Assume V_{DD}=2.5V, C_{out}=30fF and f_{clk}=250MHz.

Solution

Since D is always 1, the circuit implements the following function $Y = \overline{(A+B)C}$.

$P_{(A+B)=1} = P_{A=0}.P_B = 0 = 0.5*(1-0.2) = 0.4$,

$P_{(A+B)=0} = 1 - 0.4 = 0.6$,

$P_{Y=0} = P_{(A+B)=1}.P_C = 1 = 0.6*0.3 = 0.18$

$P_{Y=1} = 1 - 0.18 = 0.82$

$P_{Y=0=>1} = 0.18*0.82 = 0.1476$

So $Pdyn = P_{Y=0=>1} C_{out} V_{DD}^2 f_{clk} = (0.1476)(30.10^{-15})(2.5^2)(250.10^6) = 6.92\,\mu W$.

5. Logic effort: [16 pts]

For the circuit shown in Fig. 4, assume $\gamma = 1\ (C_{int} = C_{gate})$. For a static inverter, W_P:W_N = 2:1 gives equivalent pull-up and pull-down resistances. Let "C" be the total gate capacitance of the first inverter.

a) Determine x, y and z for the minimum delay. What's the minimum delay in terms of FO4 delay? [6 pts]
Note: 'x', 'y', 'z' does not represent the size of gate. Its means the gate capacitance of each gate.

b) Assume the 2 other inputs to the 3-input NAND z are at V_{dd}. When the primary input switches from 0 to V_{dd}, what is

i. The total energy drawn from V_{dd}? [5 pts]

ii. The total energy dissipated by heat? [5 pts]

Hint: The 2-input NAND x used as an inverter must be sized for equivalent pull-up and pull-down resistance.

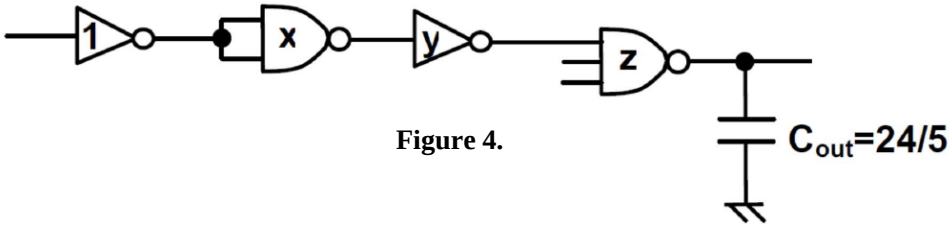
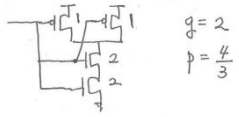


Figure 4.

New NAND2 gate

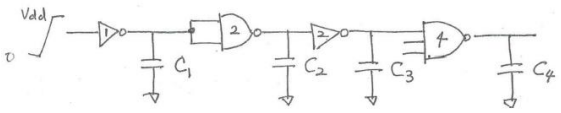


g =	1	2	1	5/3
f =	x	y/x	z/y	24/5 · 1/z
p =	1	4/3	1	3

optimal stage effort $= \sqrt[4]{2 \times \frac{5}{3} \times \frac{24}{5}} = 2$

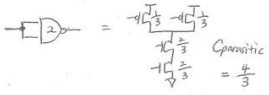
$\therefore x = 2,\ y = 2,\ z = 4$

$D = \underbrace{1 + \frac{4}{3}}_{\text{parasitic delay}} + 1 + 3 + 4 \times 2 = \frac{43}{3} = \frac{43}{15}\ FO4 \simeq \boxed{2.87\ FO4}$



First, we calculate the capacitance (parasitic + load) on each node.

$$\begin{cases} C_1 = 1 + 2 = 3 \\ C_2 = \frac{4}{3} + 2 = \frac{10}{3} \\ C_3 = 2 + 4 = 6 \\ C_4 = \frac{36}{5} + \frac{24}{5} = 12 \end{cases}$$



similarly, $C_{parasitic} = \frac{36}{5}$ for the NAND3 gate

(i) $(C_2 + C_4)\, C V_{dd}^2 = \left(\frac{10}{3} + 12\right) C V_{dd}^2 = \boxed{\frac{46}{3} C V_{dd}^2}$

(ii) $\frac{1}{2}(C_2 + C_4) C V_{dd}^2 + \frac{1}{2}(C_1 + C_3) C V_{dd}^2$

$= \frac{1}{2}(C_1 + C_2 + C_3 + C_4)\, C V_{dd}^2$

$= \frac{1}{2}\left(3 + \frac{10}{3} + 6 + 12\right) C V_{dd}^2 = \boxed{\frac{173}{6} C V_{dd}^2}$

6. Considering the logic network of Fig. 5, this represents the critical path of a complex logic block. Assume that unit C_{gate} = 2fF/μm and C_{int}/C_{gate} = γ = 0.5. All the transistors are long channel for the purpose of calculating logical effort. [14 pts]
   a) What is the total path effort from ***In*** to ***Out***? [5 pts]
   b) To minimize the delay, what should the effective fan-out per stage for this chain of gates be? [4 pts]
   c) Size the gates in this chain to minimize the delay from ***In*** to ***Out***. (Only calculate the input capacitance of the gates; don't bother to provide the actual transistor sizes.) [5 pts]

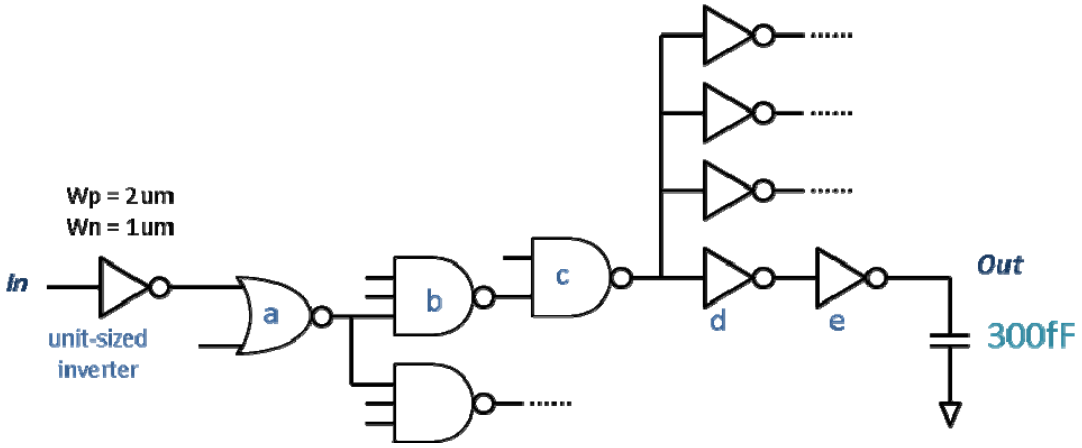


Figure 5.

(a) What is the total path effort from ***In*** to ***Out***? (10 pts)

Solution:

$$\prod LE = 1\times(\frac{5}{3})\times(\frac{5}{3})\times(\frac{4}{3})\times 1\times 1 = \frac{100}{27}$$

$$B = \prod b_i = 1\times 2\times 1\times 4\times 1\times 1 = 8$$ (2 pts for each equation)

$$F = \frac{C_L}{C_{in}} = \frac{300\,fF}{(\frac{2\,fF}{um})(2um+1um)} = 50$$

Path Effort: $PE = (\prod LE)(B)F = \frac{100}{27}\times 8\times 50 = \frac{40000}{27} = 1481.48$ (4 pts)

(b) To minimize the delay, what should the effective fan-out per stage for this chain of gates be? (10 pts)

Solution:

Effective Fan-out: $EF = \sqrt[3]{PE} = \sqrt[3]{1481.48} = 3.38$ (10 pts)

(c) Size the gates in this chain to minimize the delay from ***In*** to ***Out***. (Only calculate the input capacitance of the gates; don't bother to provide the actual transistor sizes.) (10 pts)

Solution:

Since $EF = (f_x)(b_x)(LE_x) = 3.38$ for each stage and $f_x = \frac{C_{out,x}}{C_{in,x}}$

We can calculate the input capacitance of each stage as follows:

$$C_{in,e} = C_{out,e}\frac{(b_e)(LE_e)}{EF} = 300\frac{1\times 1}{3.38} = 88.76$$

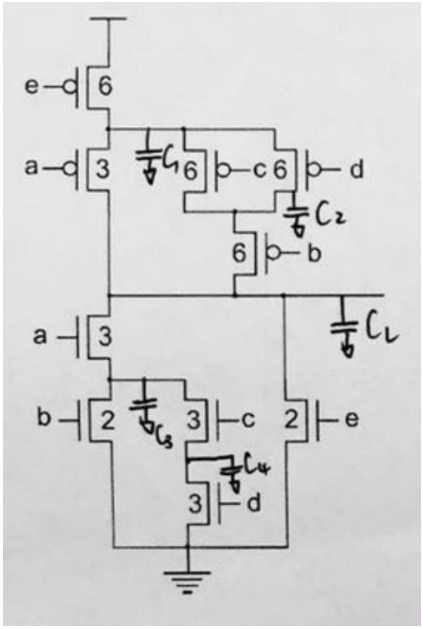
$$C_{in,d} = C_{out,d}\frac{(b_d)(LE_d)}{EF} = 88.76\frac{1\times 1}{3.38} = 26.26$$

$$C_{in,c} = C_{out,c}\frac{(b_c)(LE_c)}{EF} = 26.26\frac{4\times\frac{4}{3}}{3.38} = 41.44$$ (2 pts for each stage)

$$C_{in,b} = C_{out,b}\frac{(b_b)(LE_b)}{EF} = 41.44\frac{1\times\frac{5}{3}}{3.38} = 20.43$$

$$C_{in,a} = C_{out,a}\frac{(b_a)(LE_a)}{EF} = 20.43\frac{2\times\frac{5}{3}}{3.38} = 20.15$$

7. Static Complementary CMOS gates: [13pts]
   a) Use the Elmore delay approximation to find the worst-case rise and fall delays at the output for Figure 6. The gate sizes of the transistors are given in the figure. Use the assumption that the diffusion capacitance is equal to the gate capacitance, and that a minimum sized transistor has gate and diffusion capacitance equal to C (C= Cgs = Cgd = Csb = Cdb). The resistance of an NMOS transistor with unit width is R and the resistance of a PMOS transistor with width 2 is also R. Also assume NO sharing of diffusion regions. (Hint: off-path capacitances can contribute to delay.) [8 pts]
   b) After that, please find the logical efforts for the inputs, a, b, c, d and e as well. [5 pts]



Note:
1. Consider Miller Effect on Cgs and Cgd. A capacitor experiencing identical but opposite voltage swings at both its terminals can be replaced by a capacitor to ground, whose value is two times the original value.
2. For Cgs and Cgd, only consider the contributions of channel capacitances, do not consider overlap capacitances.

For the worst-case rise:
Initially, to discharge c3 and c4, we set a = 1 and c = 1, to discharge c2 and c1, we set b = 0 and d = 0. To make sure the output is low, e = 1. Then e -> 1.
C1 = Cdb_e + Csb_a + Csb_c + Csb_d + 2 * Cgd_e + 2 * Cgs_d = 21C + 2 * 12C
C2 = Cdb_c + Cdb_d + Csb_b + 2 * Cgs_b + 2 * Cgd_d = 18C + 2 * 12C
C3 = Csb_a + Cdb_b + Cdb_c + 2 * Cgs_a + 2 * Cgd_c = 8C + 2 * 6C
C4 = Csb_c + Cdb_d + 2 * Cgs_c = 6C + 2 * 3C
CL = Cdb_a + Cdb_e + Cdb_a + Cdb_b + 2 * Cgd_a + 2 * Cgd_b = 14C + 2 * 9C
tpLH = 0.69 * (Rep * (C1 + C2 + C3 + C4 + CL) + Rdp * (C2 + C3 + C4 + CL) + Rbp * (C3 + C4 + CL))

For the worst-case fall: the final state of (abcde) is 10110, to discharge C2,C3,C4,CL
C2 = Cdb_c + Cdb_d + Csb_b + 2 * Cgs_b = 18C + 12C
C3 = Csb_a + Cdb_b + Cdb_c + 2 * Cgs_a + 2 * Cgd_c = 8C + 2 * 6C
C4 = Csb_c + Cdb_d + 2 * Cgs_c +2 * Cgd_d= 6C + 2 * 3C + 2*3C

CL = Cdb_a + Cdb_e + Cdb_a + Cdb_b + 2 * Cgd_a + 2 * Cgd_b = 14C + 2 * 9C

tpHL = 0.69 * (Rdn * (C2 + C3 + C4 + CL) + Rcn * (C2 + C3 + CL) + Ran * (C2 + CL))

(2) The equivalent size inverter is 2:1,

$$g_a = \frac{6}{3} = 2, g_b = \frac{8}{3}, g_c = \frac{9}{3} = 3, g_a = \frac{9}{3} = 3, g_e = \frac{8}{3}$$