Submission:

Please submit a PDF version of your answers via Blackboard. A scanning version of the handwriting is allowed, but your scanned image needs to be clear enough.

Rules:

- Please try to work on your own. Discussion is permissible, but identical submissions are unacceptable!
- Please show all intermediate steps: a correct solution without an explanation will get zero credit.
- Please submit on time. Late submission will NOT be accepted.
- Please prepare your submission in English only. No Chinese submission will be accepted.

1. Consider scaling a CMOS technology by S>1. In order to maintain compatibility with existing system components, you decide to use constant voltage scaling. [12 pts]
   a) In traditional constant voltage scaling, transistor widths scale inversely with S, $W \propto 1/S$. To avoid the power increases associated with constant voltage scaling, however, you decide to change the scaling factor for *W*. What should this new scaling factor be to maintain approximately constant power? Assume long-channel devices (i.e., neglect velocity saturation). [5 pts]
   b) How does delay scale under this new methodology? [5 pts]
   c) Assuming short-channel devices (i.e., velocity saturation), how would transistor widths have to scale to maintain the constant power requirement? [2 pts

[M, None, 3.3.5] Consider scaling a CMOS technology by S > 1. In order to maintain compatibility with existing system components, you decide to use constant voltage scaling.

a. In traditional constant voltage scaling, transistor widths scale inversely with S, $W \propto 1/S$. To avoid the power increases associated with constant voltage scaling, however, you decide to change the scaling factor for *W*. What should this new scaling factor be to maintain approximately constant power. Assume long-channel devices (i.e., neglect velocity saturation).

Solution

We know that: $P \propto CV_{DD}^2 f$ and $f \propto \frac{1}{t_P} \propto \frac{I_{Dsat}}{CV_{DD}}$, so

$$P \propto I_{Dsat} V \propto k' \frac{W}{L}(V - V_t)^2 V \propto (s)\frac{(W)}{\left(\frac{1}{s}\right)}$$

To keep power constant we need to scale $W \propto \frac{1}{s^2}$. which means redesigning gates with W a factor of 1/s smaller.

b. How does delay scale under this new methodology?

Solution

$$t_P \propto \frac{CV}{k'\frac{W}{L}V^2} \propto \frac{WL\frac{\varepsilon}{t}}{k'\frac{W}{L}V} \propto \frac{\left(\frac{1}{s^2}\right)\left(\frac{1}{s}\right)\frac{1}{1/s}}{s\frac{1/s^2}{1/s}}$$

so $t_P \propto 1/s^2$.

c. Assuming short-channel devices (i.e., velocity saturation), how would transistor widths have to scale to maintain the constant power requirement?

Solution

$P \propto I_{SAT} V_{DD} \propto V_{DD} W C_{ox}(V_{gs} - V_t)\upsilon_{max} \propto W(s)$, so $W \propto \frac{1}{s}$.
This means that no changes need to be made.

2. Elmore Delay [12 pts]

a) A RC network is shown in Fig. 1. Calculate the Elmore delay from ***In*** to ***Out1*** and from ***In*** to ***Out2***. Which one is critical path? [4 pts]

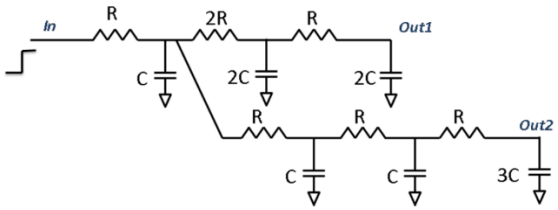


Figure 1. RC Network.

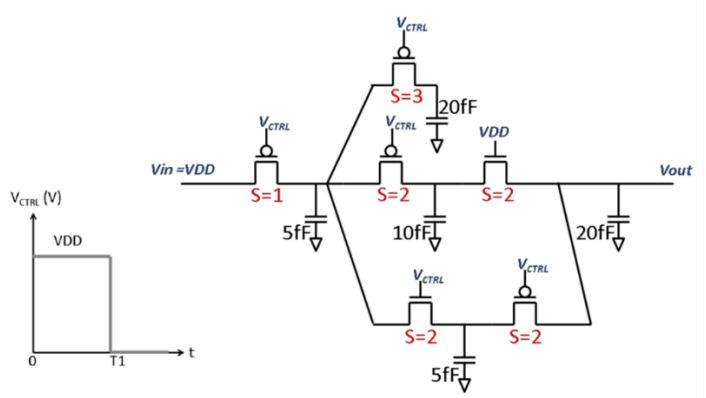


Figure 2. Pass-Transistor Logic Network.

Consider the circuit in Figure 2, we will use an equivalent resistor-capacitor model and Elmore delay to estimate propagation delay of the circuit.

The size of the transistors is indicated as S. (S=1 means the minimum size, $W=W_{min}$; S=2 means $W=2xW_{min}$, etc.) Assume the following parameters for the minimum-size NMOS and PMOS transistors, S=1: R_{eqNMOS}=10kΩ, R_{eqPMOS}=20kΩ, $C_{gs}=C_{gd}$=0.5fF; $C_{db}=C_{sb}$=1fF. Ignore overlap capacitances and feed-through from the gates of the switching transistors to the circuit nodes. Assume all nodes (except V_{in}) are initially at 0V. A voltage waveform V_{CTRL} shown in Fig.2 is applied to the circuit.

b) Draw the equivalent R-C circuit after t=T1 including all relevant resistors and capacitors and indicate their values. [4 pts]

c) From the equivalent model, calculate the delay between t=T1 and the time when $V_{out}=V_{DD}/2$ (Assume V_{DD} is much larger than V_T, i.e. $V_{DD}>>V_T$). [4 pts]

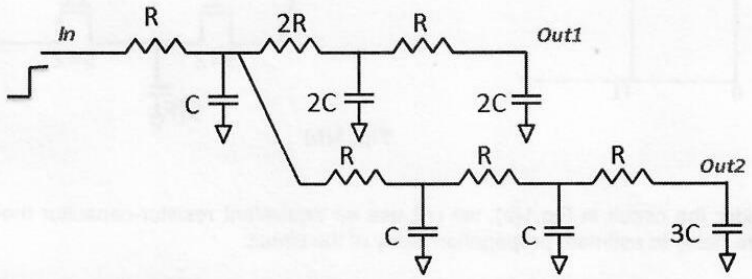


Fig. 1(a) RC Network

(b) A RC network is shown in Fig. 1(a). Calculate the Elmore delay from ***In*** to ***Out1*** and from ***In*** to ***Out2***. Which one is critical path? (10 pts)

Solution:

(1) From ***In*** to ***Out1***:

$$\tau_{in\_out1} = [RC + (R+2R)\cdot 2C + (R+2R+R)\cdot 2C] + [R\cdot(C+C+3C)] = 20RC$$

From ***In*** to ***Out2***:

$$\tau_{in\_out2} = [R\cdot C + (R+R)C + (R+R+R)\cdot C + (R+R+R+R)\cdot 3C] + [R\cdot(C+2C+2C)] = 22RC$$

The Elmore delay from ***In*** to ***Out1***is 20RC and the Elmore delay from ***In*** to ***Out2***is 22RC. So the critical path is from ***In*** to ***Out2***.

Note: Elmore Delay is just a time constant for this network. If you want to calculate the propagation delay:

$$Td_{in\_out1} = 0.69 * \tau_{in\_out1}$$

$$Td_{in\_out2} = 0.69 * \tau_{in\_out2}$$

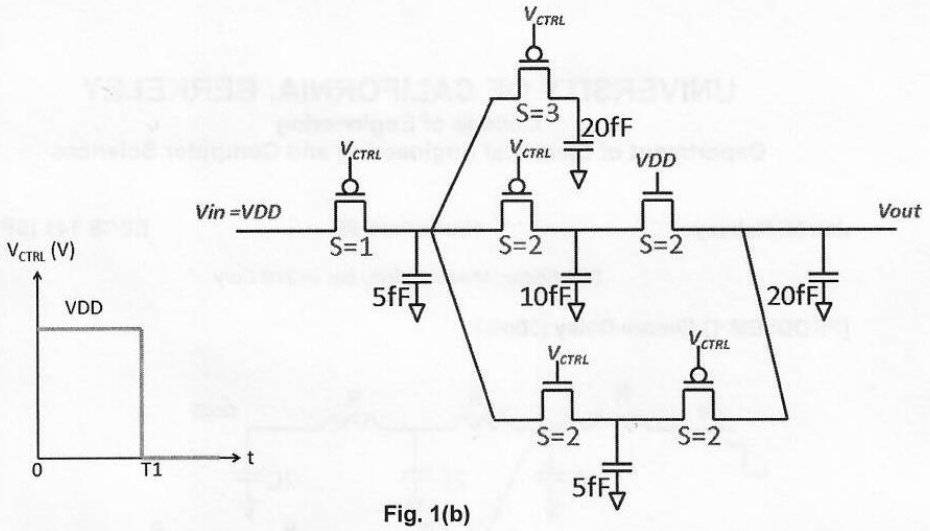


Fig. 1(b)

Consider the circuit in Fig.1(b), we will use an equivalent resistor-capacitor model and Elmore delay to estimate propagation delay of the circuit.

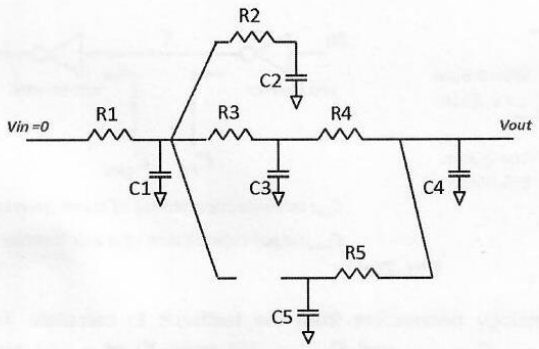
The size of the transistors is indicated as S. (S=1 means the minimum size, $W=W_{min}$; S=2 means $W=2xW_{min}$, etc.) Assume the following parameters for the minimum-size NMOS and PMOS transistors, S=1: $R_{eqNMOS}=10k\Omega$, $R_{eqPMOS}=20k\Omega$, $C_{gs}=C_{gd}=0.5fF$; $C_{db}=C_{sb}=1fF$. Ignore overlap capacitances and feed-through from the gates of the switching transistors to the circuit nodes.

Assume all nodes (except Vin) are initially at 0V. A voltage waveform V_{CTRL} shown in Fig.1(b) is applied to the circuit.

(c) Draw the equivalent R-C circuit after t=T1 including all relevant resistors and capacitors and indicate their values. (10 pts)

Solution:

(1) After t=T1, the equivalent R-C circuit is :



Component values:

$R1=R_{eqPMOS}=20k\Omega$
$C1=5fF+6C_{gs}+8C_{db}=5fF+3fF+8fF=16fF$
$R2=R_{eqPMOS}/3=6.67k\Omega$
$C2=20fF+3C_{gs}+3C_{db}=20fF+1.5fF+3fF=24.5fF$
$R3=R_{eqPMOS}/2=10k\Omega$
$C3=10fF+4C_{gs}+4C_{db}=16fF$
$R4=R_{eqNMOS}/2=5k\Omega$
$C4=20fF+4C_{gs}+4C_{db}=20fF+2fF+4fF=26fF$
$R5=R_{eqPMOS}/2=10k\Omega$
$C5=5fF+2C_{gs}+4C_{db}=10fF$

(d) From the equivalent model, calculate the delay between t=T1 and the time when Vout=VDD/2 (Assume VDD is much larger than V_T, i.e. VDD>>V_T). (10 pts)

Solution:

The equivalent circuit satisfies the conditions for an RC tree (see pg. 153). Therefore we can use Eq. 4.13 to find the equivalent time-constant:

$$\tau_{vout} = R1 \cdot C1 + R1 \cdot C2 + (R1 + R3) \cdot C3 + (R1 + R3 + R4) \cdot C4 + (R1 + R3 + R4) \cdot C5 = 2.55ns$$

The propagation delay is:

$$T_{pLH} = 0.69 \cdot \tau_{vout} = 1.76ns$$

3. Both resistance and capacitance increase with wire length L, so the RC delay of a wire increases with L^2, as shown in Fig.3. By splitting the wire into N segments and inserting a repeater (an inverter or buffer) to actively drive each wire segment, the delay can be reduced, as shown in Fig.4. [10 pts]

Suppose a unit inverter has resistance R_{ref}, diffusion capacitance C_{iref} and gate capacitance $\frac{C_{iref}}{\gamma}$. A wire has resistance r_w and capacitance c_w per unit length. Considering inserting repeaters of S times unit size.

Figure 3.

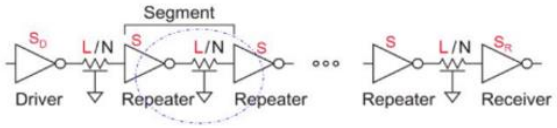
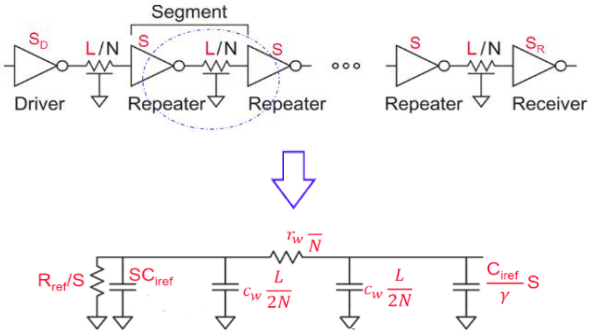


Figure 4.

a) Given the size of the driver and receiver S_D and S_R, derive the Elmore delay expression of the repeated wire in Fig4. [6 pts]

b) According to a), derive the optimal S and N respectively to optimize the Elmore delay. [4 pts]



a) Given the size of the driver and receiver S_D and S_R, derive the Elmore delay expression of the repeated wire in Fig. 11.

Solution:

The Elmore delay of the segment of Fig. 12:

$$\tau_{segment} = SC_{iref}\frac{R_{ref}}{S} + c_w\frac{L}{2N}\frac{R_{ref}}{S} + c_w\frac{L}{2N}\left(\frac{R_{ref}}{S} + r_w\frac{L}{N}\right) + \frac{C_{iref}}{\gamma}S\left(\frac{R_{ref}}{S} + r_w\frac{L}{N}\right)$$

$$= \frac{R_{ref}}{S}\left(SC_{iref} + c_w\frac{L}{N} + \frac{C_{iref}}{\gamma}S\right) + r_w\frac{L}{N}\left(c_w\frac{L}{2N} + \frac{C_{iref}}{\gamma}S\right)$$

The Elmore delay of the repeated wire in Fig. 11:

$$\tau = N\,\tau_{segment}$$

b) According to a), derive the optimal S and N respectively to minimize the Elmore delay.

Solution:

By differentiating τ with respect to S and N, you can get the optimal S and N.

$$S = \sqrt{\frac{\gamma c_w R_{ref}}{C_{iref} r_w}}$$

$$\frac{L}{N} = \sqrt{\frac{2(1+\gamma)C_{iref}R_{ref}}{\gamma c_w r_w}}$$

4. [16pts]

a) Find the final value of the voltage VOUT for the various switch logics as shown in Fig. 5. Assume that VTN=|VTP|=0.3V, that and the output capacitor, CL, is initially discharged. Ignore sub-threshold conduction and body effect. All middle nodes are discharged initially. [7 pts]

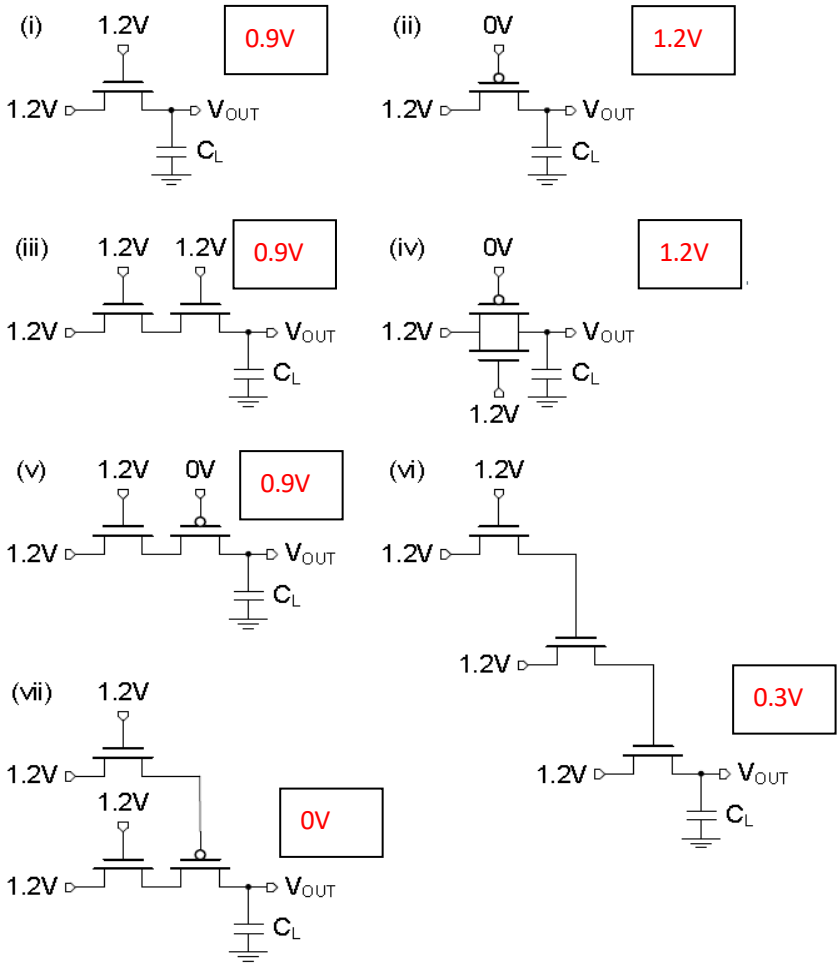


Figure 5.

b) Find the final value when the input is high, V_{IN}=1.2V.After the output reaches its final value, a 1.2V to 0 step is applied to the input, V_{IN}. Determine the energy consumed in the transistors, $E_{1->0}$, from Fig.6 during the transition. The load capacitor C_L is 10fF. Ignore any other parasitic capacitors except C_L. [4 pts]

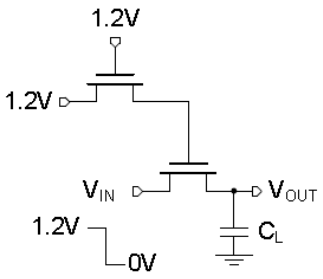


Figure 6.

Find the final value when the input is high, V_{IN}=1.2V.

VDD-2*VTN=0.6V

After the output reaches its final value, a 1.2V to 0 step is applied to the input, V_{IN}. Determine the energy consumed in the transistors, $E_{1->0}$, from Fig.2.(b) during the transition. The load capacitor C_L is 10fF. Ignore any other parasitic capacitors except C_L.

Because stored Energy is totally dissipated in the transistor,

E(diss) = E(stored)

E1->0 = ½* CL * $(VDD-2*VTN)^2$=0.5*(10f)*$(1.2-0.6)^2$=1.8fJ

c) For Fig. 7, initially output voltage, VOUT, is discharged (VOUT=0). Find the energy dissipated in the transistor during the first 0→1 transition. Then, after the output reaches its final value, a 1.2V to 0 step is applied to the input, followed by the second 0 to 1.2V step. Find the energy dissipated in the transistor in the first 1→0 transition. The load capacitor C_L is 10fF. [5 pts]

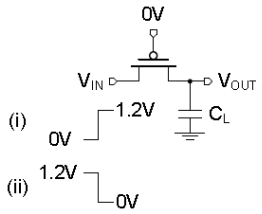


Figure 7.

Initially output voltage, V_{OUT}, is discharged, V_{OUT}=0. Find the energy dissipated in the transistor during the first 0→ 1 transition, First $E_{0->1}$.

E(diss) = E(supply)-E(stored) = CL*VDD^2 - ½*CL*VDD^2

First E0->1 = ½* CL * $(VDD)^2$= 0.5*(10f)*$(1.2)^2$= 7.2fJ

Then, after the output reaches its final value, a 1.2V to 0 step is applied to the input, followed by the second 0 to 1.2V step. Find the energy dissipated in the transistor in the first 1 → 0 transition, First $E_{1->0}$,and the second 0→ 1 transition, Second $E_{0->1}$. The load capacitor C_L is 10fF.

There is still remained Energy in the C_L because final V_{OUT} is 0.3V.

First E1->0 = E(supply)-E(remained)

= ½* CL * (VDD^2-VTP^2) =0.5*(10f)*(1.2^2-0.3^2) =6.75fJ

Second E0->1 = E(supply)-E(stored)

= CL*VDD*(VDD-VTP) - ½* CL * (VDD^2-VTP^2)

= ½* CL * (VDD^2-2*VDD*VTP+VTP^2)

= ½* CL * $(VDD-VTP)^2$ =0.5*(10f)*$(1.2-0.3)^2$ =4.05fJ

5. An NMOS transistor is used to charge a large capacitor, as shown in Fig. 8. V_{DSAT}=0.63V, V_{TN0}=0.43V, $\gamma = 0.4V^{1/2}$. [12 pts]

a) Determine the t_{pLH} (the transition time from V_{OL} to $(V_{OH}+V_{OL})/2$, V_{OH} means the maximum value of V_{out}, while V_{OL} means the minimum value of V_{out}) of this circuit and assume an ideal step from 0 to 2.5V at the input node. [5 pts]

b) Assume that a resistor R_S of 5 kΩ is used to discharge the capacitance to ground. Determine t_{pHL}. [2 pts]

c) According to b), determine how much energy is taken from the supply during the charging of the capacitor? How much of this is dissipated in M1? How much is dissipated in the pull-down resistance during discharging? How does this change when R_S is reduced to 1 kΩ. [3 pts]

d) Replace the NMOS transistor by a PMOS, and size it that k_p is equal to the k_n of the original NMOS. Will the resulting structure be faster? Explain why or why not. [2 pts]

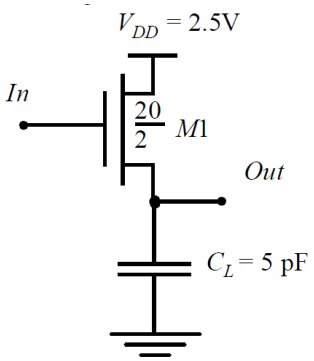


Figure 8.

a. Determine the t_{pLH} of this circuit, assuming an ideal step from 0 to 2.5V at the input node.

Solutions

To determine the rise time, an average current has to be calculated between the start of the transistion with V_O=0V and midpoint of the transition.

At the start of the transistion: V_O=V_{OL}=0V, M1 is velocity saturated and I_{Dsat}=1.46mA. To find the votlage swing, V_{OH} must be calculated using the body effect:

$$V_{gs} = 2.5V - V_{OH} = V_{tn} + \gamma(\sqrt{|0.6 + V_{OH}|} - \sqrt{0.6})$$

V_{OH}=1.76V. The midpoint is thus,

$$\frac{V_{OH} - V_{OL}}{2} = 0.88V$$

and the threshold voltage at the midpoint is: $V_T(V_{sb}$=0.88V)=0.607V.

Using this threshold voltage, V_{GT}=1.013V, V_{DS}=1.62V, and V_{DSat}=0.63V, thus, the transistor M1 is still velocity saturated, giving I_{DSat}= 0. 554 mA.

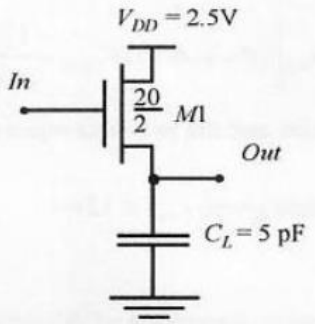
Finding the average current between V_0= 0V and V_0= 0.88V gives: $I_{average}$= **1. 007 mA**

$$t_p = \frac{C_L \Delta V}{I_{average}} = \frac{5pF \times 0.88V}{\mathbf{1.007\ mA}} = \mathbf{4.37}n\text{sec}$$

b. Assume that a resistor R_S of 5 kΩ is used to discharge the capacitance to ground. Determine t_{pHL}.

Solution

t_{pHL}=0.69*$R_L C_L$=0.69*5kΩ*5pF=17.25ns



c. Determine how much energy is taken from the supply during the charging of the capacitor. How much of this is dissipated in M1. How much is dissipated in the pull-down resistance during discharge? How does this change when R_S is reduced to 1 kΩ.

Solution

ΔQ_{VDD}=$C_L\Delta V$=5pF*1.76V=8.8pC

ΔE_{VDD}=ΔQ_{VDD}*V_{dd}=8.8pC*2.5V=22pC

Half the energy is dissipated in the transistor M1, while the other half is dissipated in the restistor R_s. The energy dissipated is independent of R_s.

d. The NMOS transistor is replaced by a PMOS device, sized so that k_p is equal to the k_n of the original NMOS. Will the resulting structure be faster? Explain why or why not.

Solution

If a PMOS device replaces the NMOS device, body effect will not exist and the PMOS device will be faster.

6. Sizing a chain of inverters. [16 pts]
   a) In order to drive a large capacitance (C_L = 20 pF) from a minimum size gate (with input capacitance C_i = 10fF), you decide to introduce a two-staged buffer as shown in Figure 9. Assume that the propagation delay of a minimum size inverter is 70 ps. Also assume that the input capacitance of a gate is proportional to its size. Determine the sizing of the two additional buffer stages that will minimize the propagation delay. We assume γ=1. [4 pts]
   b) If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case? [4 pts]
   c) Describe the advantages and disadvantages of the methods shown in (a) and (b). [4 pts]
   d) Determine a closed form expression for the power consumption in the circuit. Consider only gate capacitances in your analysis. What is the power consumption for a supply voltage of 2.5V and an activity factor of 1? [4 pts]

   HINT: For simplification, you may need to ignore self-loading sometimes.

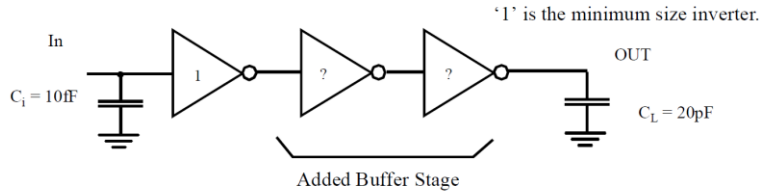


Figure 9.

7. Sizing a chain of inverters.

a. In order to drive a large capacitance (C_L = 20 pF) from a minimum size gate (with input capacitance C_i = 10fF), you decide to introduce a two-staged buffer as shown in Figure 5.12. Assume that the propagation delay of a minimum size inverter is 70 ps. Also assume that the input capacitance of a gate is proportional to its size. Determine the sizing of the two additional buffer stages that will minimize the propagation delay.

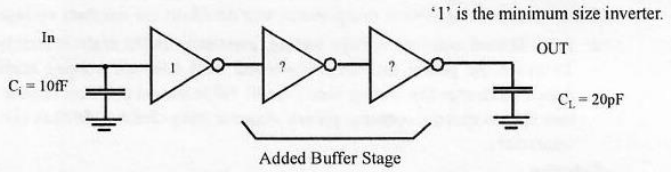


Figure 5.12 Buffer insertion for driving large loads.

Solution

Minimum delay occurs when the delay through each buffer is the same. This can be achieved by sizing the buffer as f, f^2, respectively
where $f = \sqrt[N]{F} = \sqrt[3]{2000} = 12.6$, so ($\gamma$=0)

$$t_p = Nt_{p0}(1 + f/\gamma) = 3 \cdot 70ps \cdot (1 + 12.6) = 2.8ns$$

b. If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case?

Solution

From the text, we know that the minimum delay occurs when f = e. Therefore,

$$N = \frac{\ln(2000)}{\ln(f)} = 7.6$$

$$f = e^{\frac{\ln(2000)}{7}} = 2.96$$

$$t_{delay} = 7 \times 3.96 \times 70\text{ps} = 1.9ns$$

c. Describe the advantages and disadvantages of the methods shown in (a) and (b).

Solution

Solution (b) is faster but it consumes much more area than (a).

d. Determine a closed form expression for the power consumption in the circuit. Consider only gate capacitances in your analysis. What is the power consumption for a supply voltage of 2.5V and an activity factor of 1?

Solution

The power consumption is determined as follows

$$P = C_{tot}V_{dd}^2 \frac{1}{T} \alpha$$

$$P = C_l V_{dd}^2 \frac{1}{T} \alpha \sum_{k=0}^{3} f^k = C_l V_{dd}^2 \frac{1}{T} \alpha \left(\frac{f^4 - 1}{f - 1}\right) = 136\left(\frac{1}{T}\right) \text{ pWatts}$$

7. The inverter below operates with V_{DD}=0.4V and is composed of $|V_t|$ = 0.5V devices. The devices have identical I_0 and n. V_T=26mV, λ_n=0.06, λ_p=0.1 and n=1.5. [12 pts]
   a) Calculate the switching threshold (V_M) of this inverter. [4 pts]
   b) Calculate V_{IL} and V_{IH} of the inverter. [8 pts]

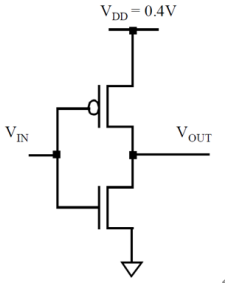


Figure 10.

The inverter below operates with V_{DD}=0.4V and is composed of |Vt| = 0.5V devices. The devices have identical I_0 and n.

a. Calculate the switching threshold (V_M) of this inverter.

Solution

The subthreshold I-V relation is given by $I_D = I_o e^{(V_{GS}-V_t)/(nV_T)}(1+\lambda V_{DS})$, assuming V_{DS} > 50mV. To calculate the switching voltage, we need to find where V_{in}=V_{out} occurs. So equating the absolute values of the currents for the two transistors we get:

$$I_o e^{V_{in}/(nV_T)}(1+\lambda_n V_{out}) = I_o e^{(V_{DD}-V_{in})/(nV_T)}(1+\lambda_p(V_{DD}-V_{out}))$$

Considering V_{in}=V_{out} and doing some cancellations we get:

$$\ln[(1+\lambda_n V_{in})/(1+\lambda_p(V_{in}-V_{DD}))] = 1/((n\cdot V_T)(V_{DD}-V_{in}-V_{in}))$$

after massaging the last equation we have:

$$V_{DD}/2 - nV_T/2 \cdot \ln[(1+\lambda_n V_{in})/(1+\lambda_p(V_{DD}-V_{in}))] = V_{in}$$

Iterating this expression with V_{DD}=0.4V, V_T=26mV, λ_n=0.06, λ_p=0.1 and n=1.5 we get V_{in}=0.2V. So we have a switching threshold of $V_{DD}/2$=0.2V.

b. Calculate V_{IL} and V_{IH} of the inverter.

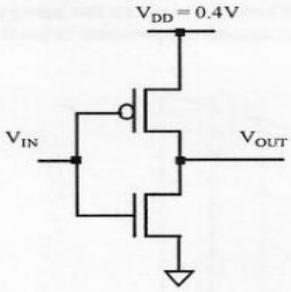


Figure 5.11 Inverter in Weak Inversion Regime

Solution

To calculate the noise margins we need to calculate the slope of the VTC at V_M=$V_{DD}/2$. Equating the currents we get:

$$I_o e^{V_{in}/(nV_T)}(1+\lambda_n V_{out}) = I_o e^{(V_{DD}-V_{out})/(nV_T)}(1+\lambda_p(V_{DD}-V_{out}))$$

and cancelling out I_o, and differentiating both sides with respect to V_{in} we get:

$$\frac{\partial}{\partial V_{in}}(e^{V_{in}/(nV_T)}(1+\lambda_n V_{out})) = \frac{\partial}{\partial V_{in}} e^{(V_{in}-V_{DD})/(nV_T)}(1+\lambda_p(V_{out}-V_{DD}))$$

$$e^{V_{in}/(nV_T)}(1+\lambda_n V_{out})/nV_T + e^{V_{in}/(nV_T)}\lambda_n\frac{\partial V_{out}}{\partial V_{in}} =$$

$$= -e^{(V_{DD}-V_{in})/(nV_T)}(1+\lambda_p(V_{DD}-V_{out}))/nV_T - e^{(V_{DD}-V_{in})/(nV_T)}\lambda_p\frac{\partial V_{out}}{\partial V_{in}}$$

manipulating this expression we get:

$$(e^{(V_{DD}-V_{in})/(nV_T)}\lambda_p + e^{V_{in}/(nV_T)}\lambda_n)\frac{\partial V_{out}}{\partial V_{in}} =$$

$$= e^{V_{in}/(nV_T)}(1+\lambda_n V_{out})/nV_T + e^{(V_{DD}-V_{in})/(nV_T)}(1+\lambda_p(V_{DD}-V_{out}))/nV_T$$

plugging in V_{out}=V_{in}=$V_{DD}/2$ we reach:

$$-e^{(V_{DD}/2)/(nV_T)}(\lambda_p+\lambda_n)\frac{\partial V_{out}}{\partial V_{in}} = e^{(V_{DD}/2)/(nV_T)}(2+(\lambda_p+\lambda_n)V_{DD}/2)/(nV_T)$$

Finally:

$$\left.\frac{\partial V_{out}}{\partial V_{in}}\right|_{Vin=Vout=V_{DD}/2} = -(2+(\lambda_p+\lambda_n)V_{DD}/2)/(nV_T)/(\lambda_p+\lambda_n)$$

Using the values V_{DD}=0.4V, V_T=26mV, λ_n=0.06, λ_p=0.1 and n=1.5 we obtain:

$$g = \frac{\partial V_{out}}{\partial V_{in}} = -325.6$$

This value is much more that we would expect from an MOS inverter (which has g~-30). However we should keep in mind that in the subthreshold regime MOS devices behave essentially as bipolar devices and can yield such values of gain.

We know that V_{IL}=V_M+(V_{DD}-V_M)/g and V_{IH}=V_M-V_M/g from the text (eq 5.7). Using these equations and the results that we got we have: V_{IL}=0.1994V and V_{IH}=0.2006V.

Also NM_H=NM_L=0.1994V

8. Elmore Delay

Refer to the slides of Topic 02. Show that for the tree shown in Fig .11, the formula written below is true. That is, prove the correctness of the formula of Elmore Delay. [10 pts]

$$\tau_{D5} = R_1(C_1 + C_2 + C_3 + C_4 + C_5) + R_3(C_3 + C_4 + C_5) + R_5C_5$$

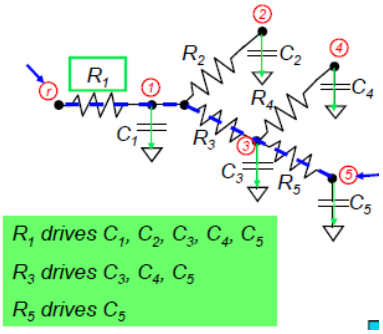
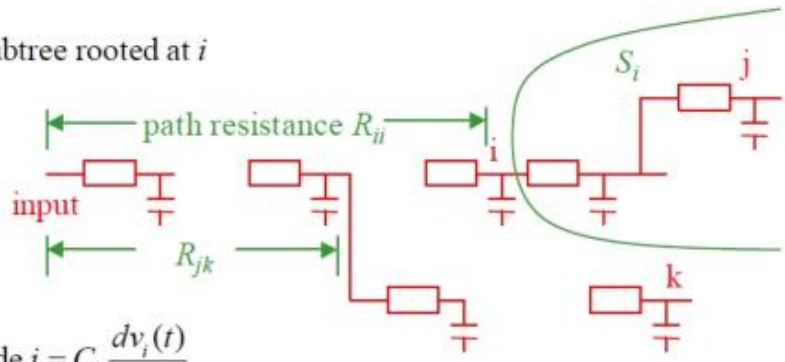


Figure 11.

P_i : path from input to node i ; s_i :subtree rooted at i

R_{jk} : resistance of common path $P_j \cap P_k$ from input to j & k



Theorem : Elmore delay to node i

$$T_{D_i} = \sum_k R_{ki} C_k$$

Proof : The current to cap. of node $i = C_i \dfrac{dv_i(t)}{dt}$

$$1 - v_i(t) = \text{The voltage drop on } P_i = \sum_{k \in P_i} R_k \cdot (\text{current to all cap's in } S_i)$$

$$= \sum_k (\text{current to cap } k) \cdot (\text{common path res. between } P_i \text{ and } P_k)$$

$$= \sum_k C_k \frac{dv_k(t)}{dt} \cdot R_{ki} = \sum_k R_{ki} C_k \frac{dv_k(t)}{dt}$$

$$T_{D_i} = \int_0^\infty v'_i(t) t \cdot dt = v_i(t) \cdot t \,|_0^\infty - \int_0^\infty v_i(t) dt$$

$$= \lim_{T \to \infty} [v_i(T) \cdot T - \int_0^T v_i(t) dt] = \lim_{T \to \infty} (v_i(T) - 1) \cdot T + \int_0^\infty (1 - v_i(t)) dt$$

- We shall show later on that $\lim_{T \to \infty} (1 - v_i(T)) \cdot T = 0$
  i.e. 1-$v_i(T)$ goes to 0 at a much faster rate than 1/T when $T \to \infty$

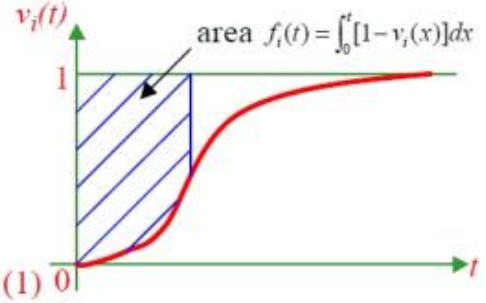
- Let $f_i(t) = \int_0^t [1 - v_i(x)] dx$

$$f_i(t) = \int_0^t \sum_k R_{ki} C_k \frac{dv_k(x)}{dx} dx$$

$$= \sum_k R_{ki} C_k v_k(t)$$

$$= \sum_k R_{ki} C_k - \sum_k R_{ki} C_k [1 - v_k(t)]$$

$$f_i(\infty) = \sum_k R_{ki} C_k$$



$$\therefore T_{D_i} = \lim_{T \to \infty} (1 - v_i(T)) T + \int_0^\infty [1 - v_i(t)] dt$$

$$= f_i(\infty) = \sum_k R_{ki} C_k$$