EE213 Lab3

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Assignment#1：Schematic and Pre-simulation:

Half Adder:

1.a.1 Explain your design of half adder briefly.

The truth table of a half adder is shown as Table 1. We can find that $C_{out} = A \cdot B$ and $S = A \oplus B$. Figure 1 shows the design of a half adder based on NAND2-gate.

Table 1 The Truth Table of a Half Adder

A	B	C_{out}	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

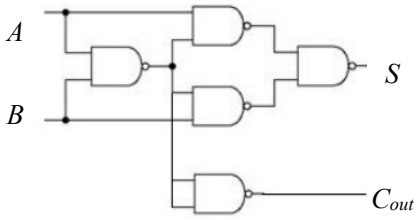

Figure 1 Design of Half Adder Based on NAND2 Gate

The process of realizing XOR with NAND gate is as follows.

$$
\begin{aligned}
S &= \overline{\overline{A \cdot \overline{AB}} \cdot \overline{B \cdot \overline{AB}}} \\
&= A \cdot \overline{AB} + B \cdot \overline{AB} \\
&= A(\overline{A} + \overline{B}) + B(\overline{A} + \overline{B}) \qquad C_{out} = \overline{\overline{AB}} = AB \\
&= A\overline{A} + A\overline{B} + B\overline{A} + B\overline{B} \\
&= A\overline{B} + B\overline{A}
\end{aligned}
$$

1.a.2 Schematic of your half adder.

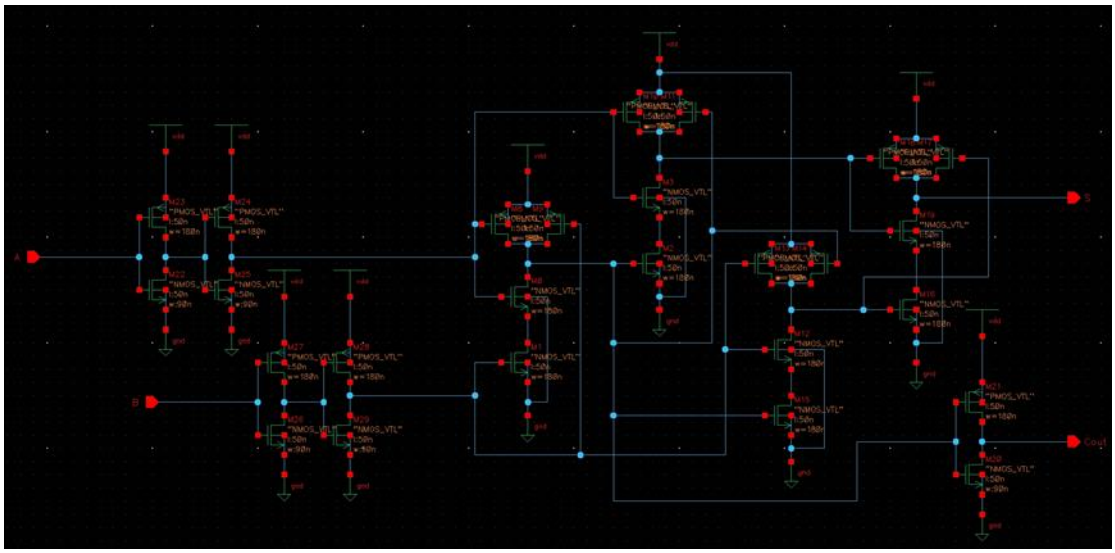

Figure 2 Schematic of 45nm Half Adder

1.a.3 Give some bullet points explaining how you optimized your design.

I mainly optimize my design though sizing. For inverters, I set the width ratio of PMOS & NMOS as 2:1, thus, the width of NMOS in inverters is 90nm and the width of PMOS in inverters is 180nm. Similarly, the width of NMOS and the width of PMOS in NANDs is both 180nm to achieve the equivalent R_{eq} of an inverter.

1.a.4 Show the input and output waveforms of the input test cases.

The I/O waveforms of the test cases for half adder is shown as Figure 3. It is corresponding to the truth table, showing it is right.

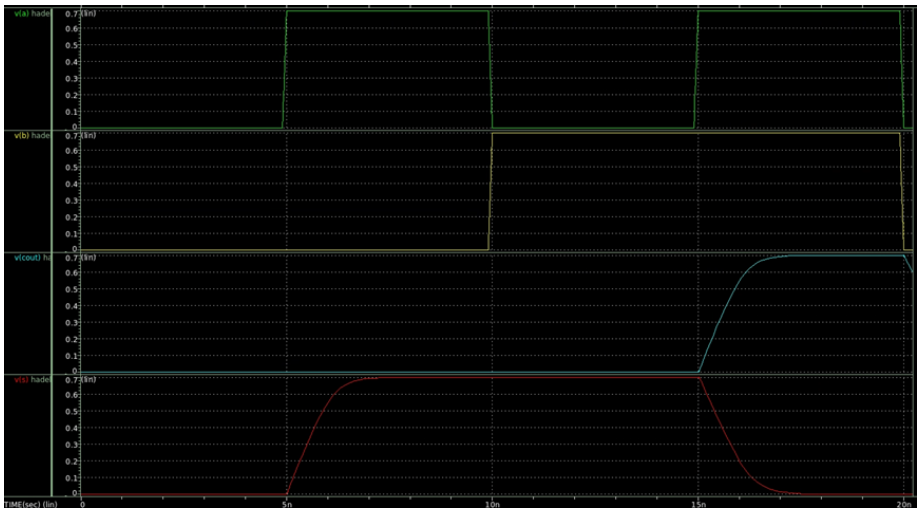

Figure 3 Waveforms of the 45nm Half Adder Test Cases(Schematic)

1.a.5 Show the worst case delay and its corresponding input/output waveforms for VDD! = 0.7V.

The worst delay of half adder is shown as Figure 4. The delay of C_{out} is 0.6441 ns and the delay of S is 0.7359 ns. So the worst delay for this case is 0.7359ns.

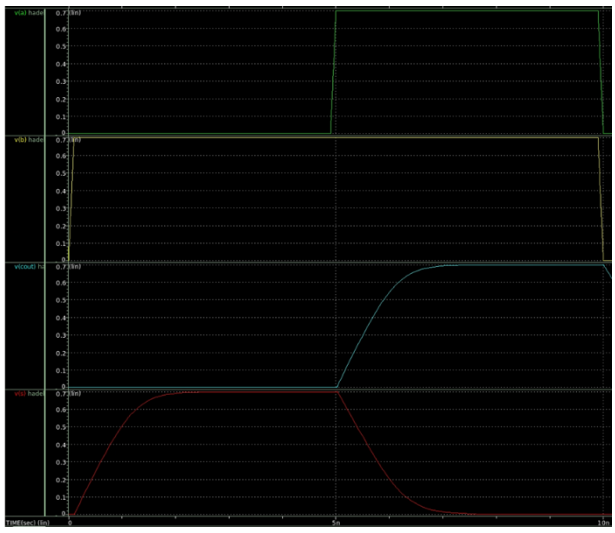

Figure 4 The Worst Delay Waveform of 45nm Half Adder(Schematic)

1.a.6 Give the power consumption at the maximum operating frequency for VDD! = 0.7V

After hspice simulation, the power_at_max is $1.627*10^{-4}$J shown in power.mt0.

Full Adder:

1.b.1 Explain your design of half adder and full adder briefly.

The truth table of a full adder is shown as Table 2. The design of mirror full adder is shown as Figure 5 which is from EE213-Topic5-Page21 by Prof. Pingqiang Zhou.The structure is highly symmetrical, which makes it easier to implement.The equation for calculating S is already shown on Figure 5.

Table 2 The Truth Table of a Full Adder

A	B	C_{in}	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	**1**	**0**	**1**	**0**
1	**1**	**1**	**1**	**1**

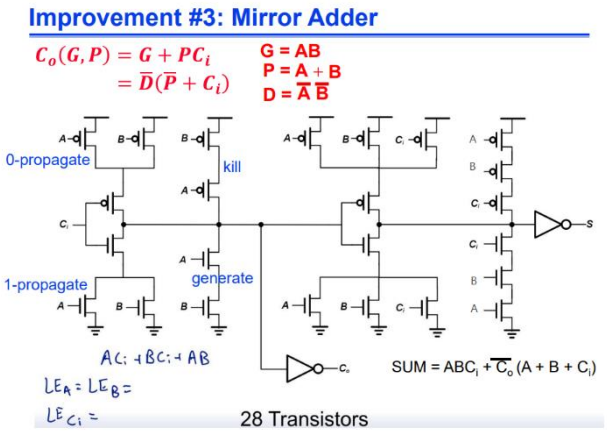

Figure 5 Design of Full Adder(Mirror)

1.b.2 Schematic of your half adder and full adder.

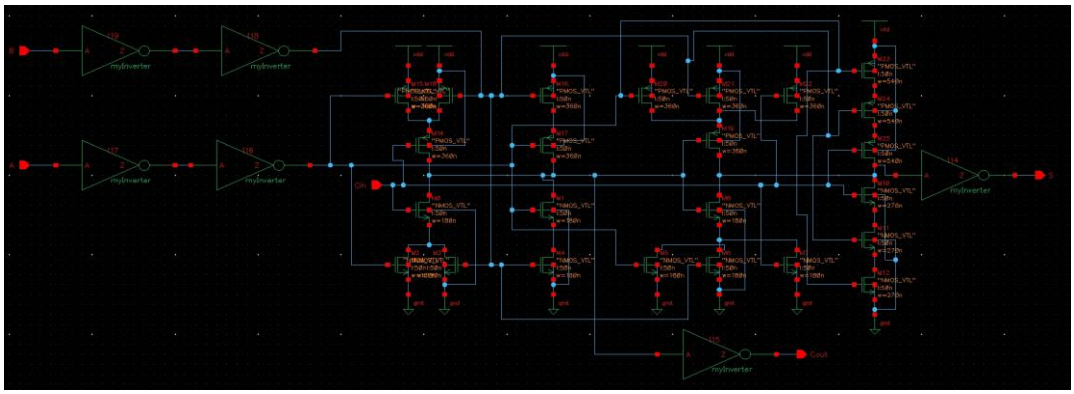

Figure 6 Schematic of 45nm Full Adder

1.b.3 Give some bullet points explaining how you optimized your design.

I also use sizing in full adder. The width ratio of an inverter is still 2:1. To achieve the same *Req* as it, my sizing ratio is shown on Figure 6 with green color.

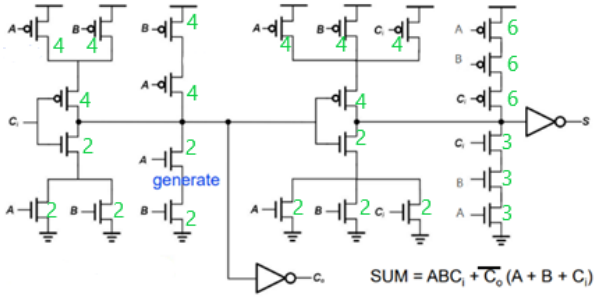

Figure 7 Sizing Parameters for Mirror Full Adder

1.b.4 Show the input and output waveforms of the input test cases.

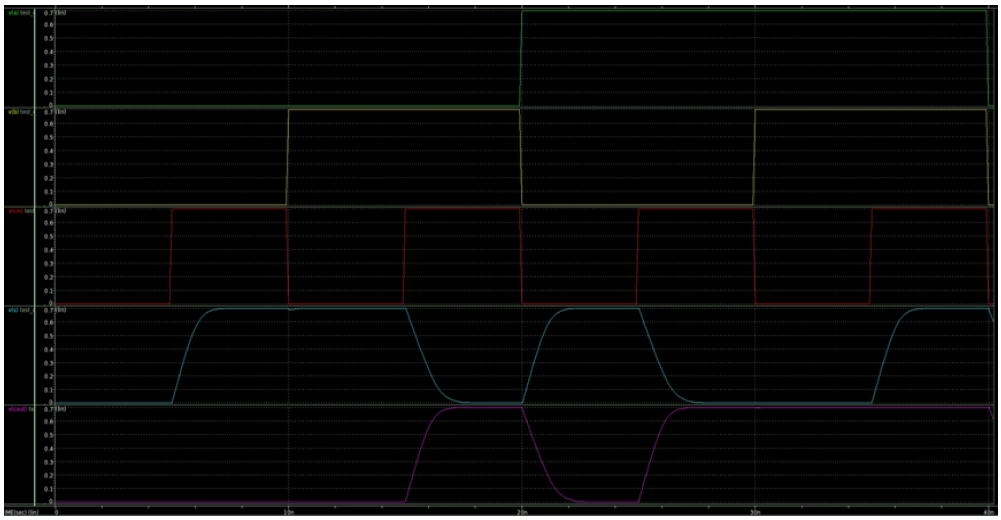

Figure 8 Waveforms of the 45nm Full Adder Test Cases(Schematic)

1.b.5 Show the worst case delay and its corresponding input/output waveforms for VDD! = 0.7V.

The worst delay of full adder is shown as Figure 9. The delay of C_{out} is 0.8287 ns and the delay of S is 0.6955 ns. So the worst delay for this case is 0.8287ns.

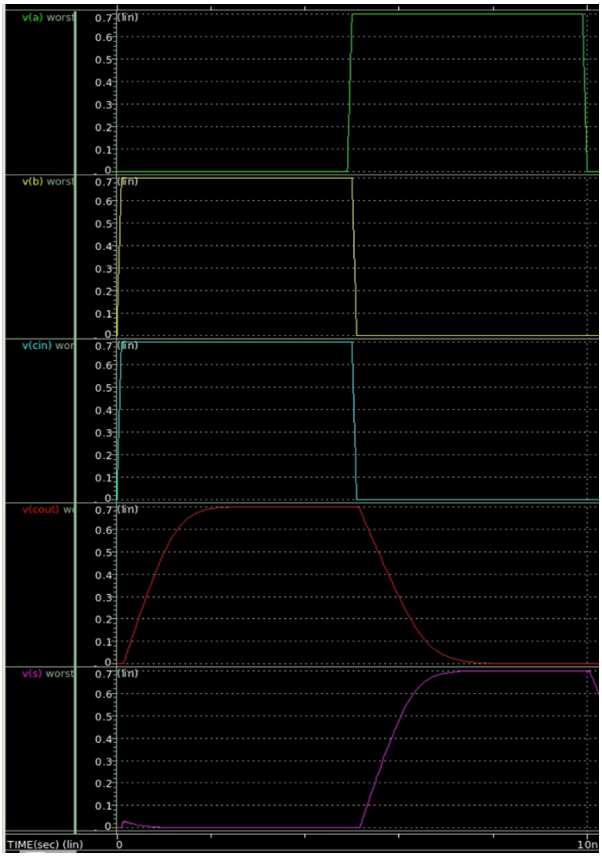

Figure 9 The Worst Delay Waveform of 45nm Full Adder(Schematic)

1.b.6 Give the power consumption at the maximum operating frequency for VDD! = 0.7V

After hspice simulation, the power_at_max is $2.697*10^{-4}$J shown in power.mt0.

Assignment#2：Layout and Post-simulation:

Half Adder:

2.a.1 Layout (with the area information) of your half adder.

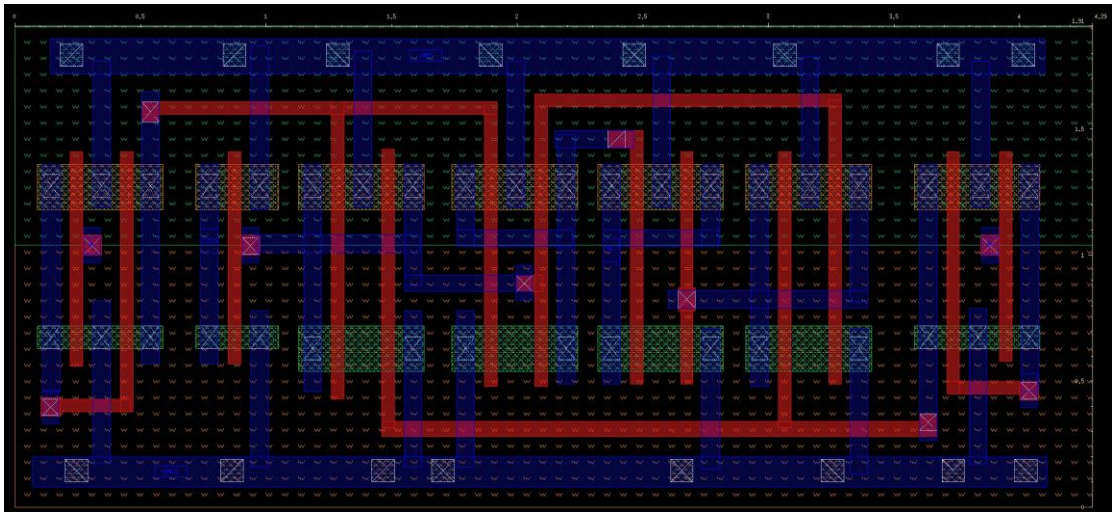

Figure 10 Layout of 45nm Half Adder

2.a.2 LVS, DRC and PEX screenshots showing no violations.

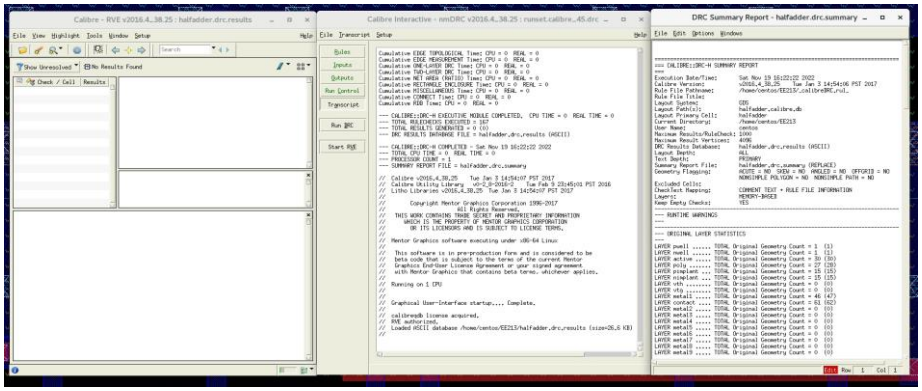

Figure 11 DRC Pass for 45nm Half Adder

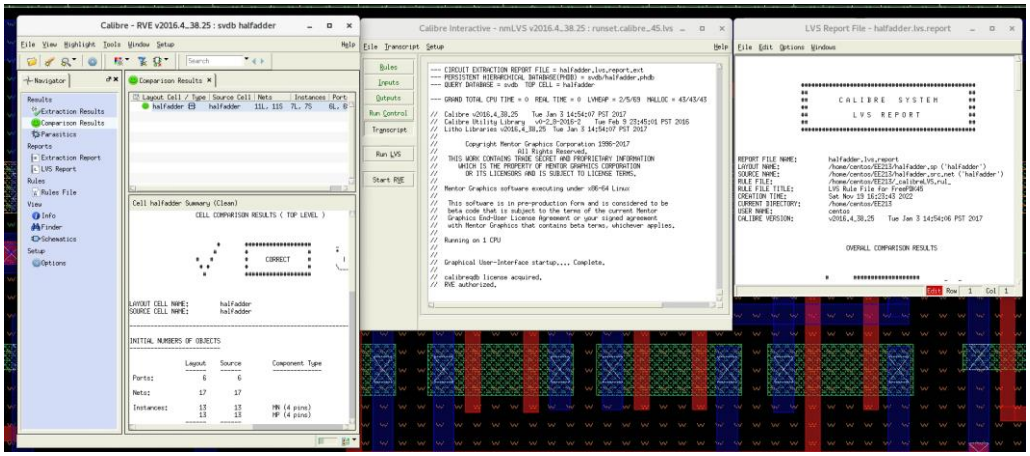

Figure 12 LVS Pass for 45nm Half Adder

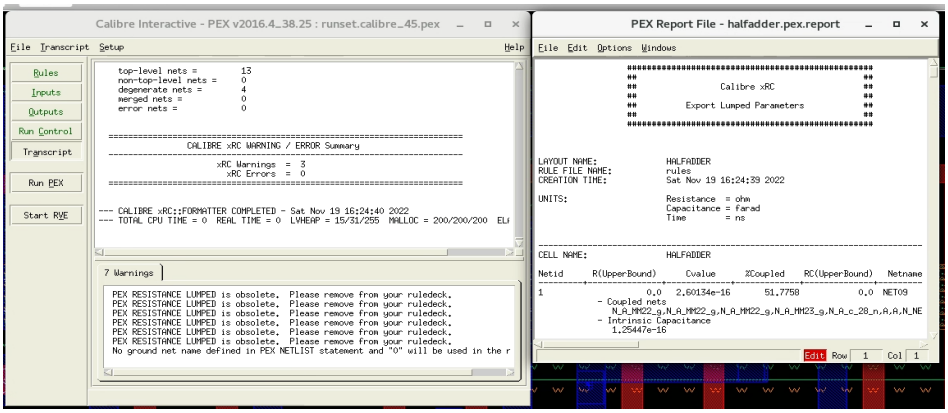

Figure 13 PEX Pass for 45nm Half Adder

2.a.3 Show the input and output waveforms of input test cases.

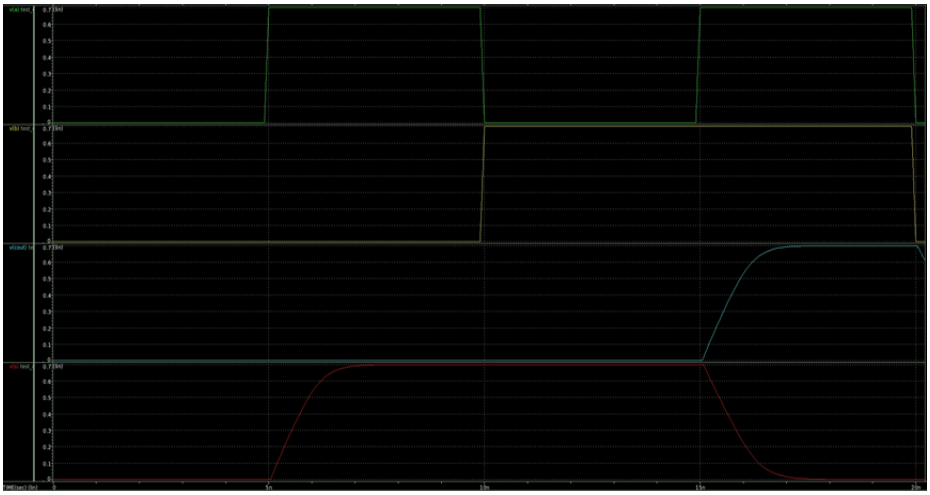

Figure 14 Waveforms of the 45nm Half Adder Test Cases(Layout)

2.a.4 Show the worst case delay and its corresponding input/output waveforms for VDD! = 0.7V.

The worst delay of half adder is shown as Figure 15. The delay of Cout is 0.6763 ns and the delay of S is 0.7821 ns. So the worst delay for this case is 0.7821ns.

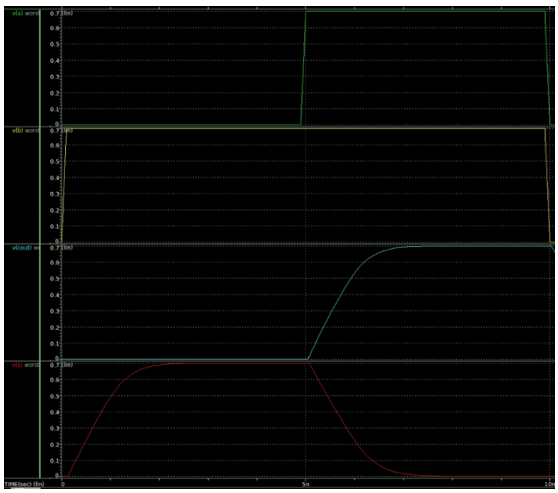

Figure 15 The Worst Delay Waveform of 45nm Half Adder(Layout)

2.a.5 Give the power consumption at the maximum operating frequency for VDD! = 0.7V.

After hspice simulation, the power_at_max is $3.134*10^{-4}$J shown in power.mt0.

Full Adder:

2.b.1 Layout (with the area information) of your and full adder.

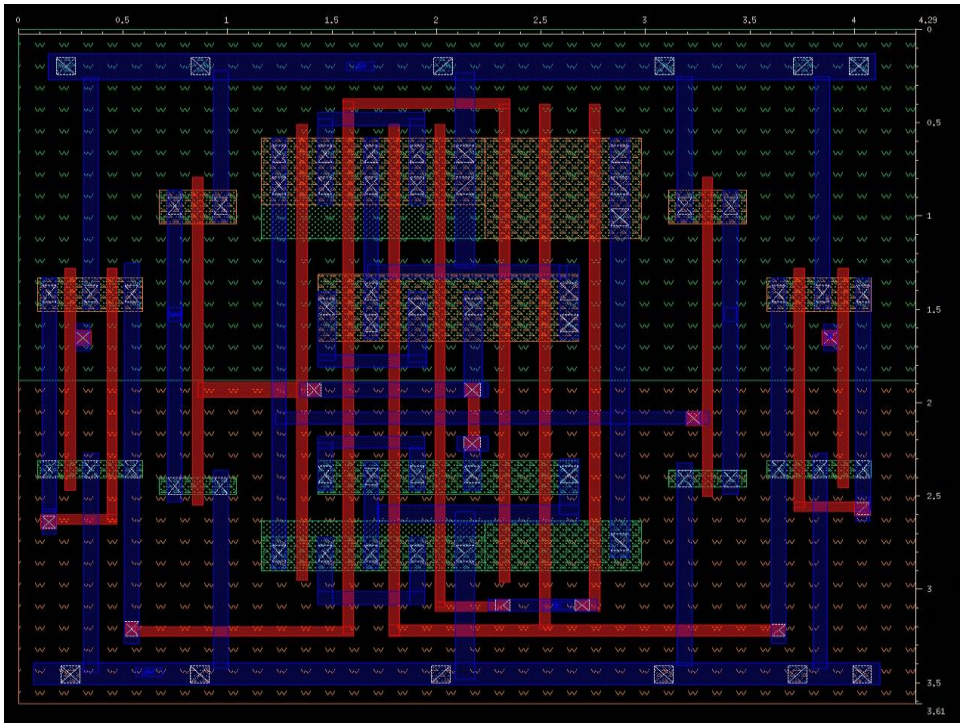

Figure 16 Layout of 45nm Full Adder

2.b.2 LVS, DRC and PEX screenshots showing no violations.

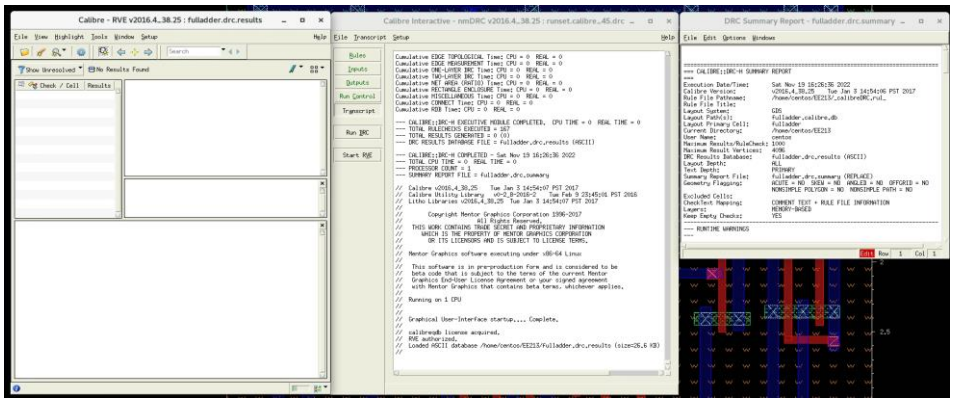

Figure 17 DRC Pass for 45nm Full Adder

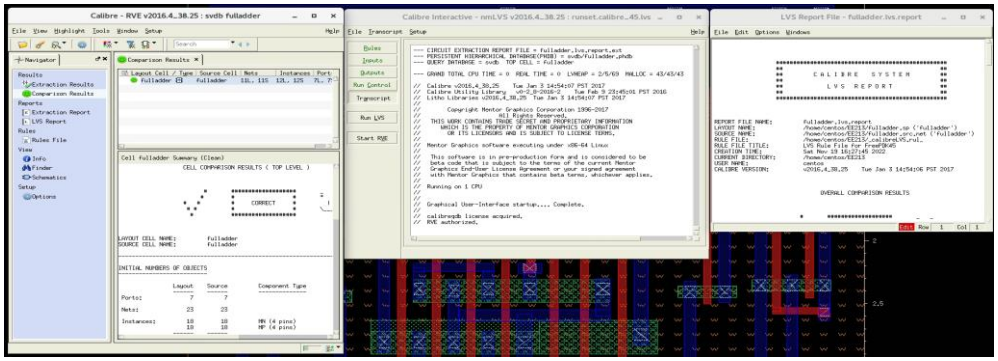

Figure 18 LVS Pass for 45nm Full Adder

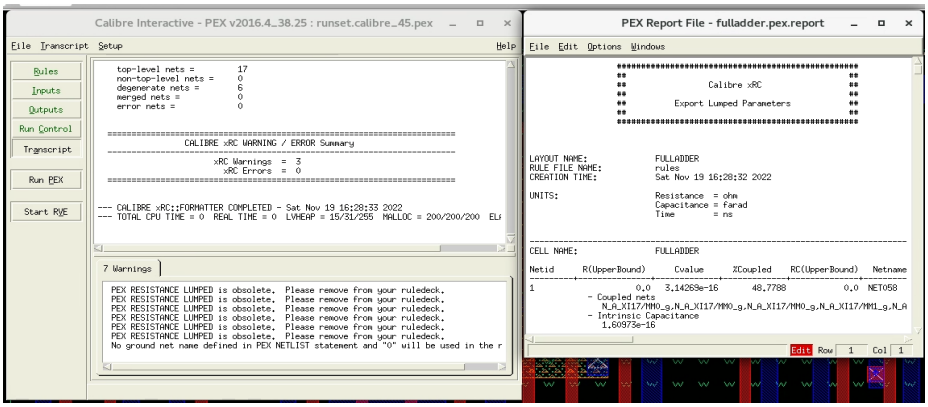

Figure 19 PEX Pass for 45nm Full Adder

2.b.3 Show the input and output waveforms of input test cases.

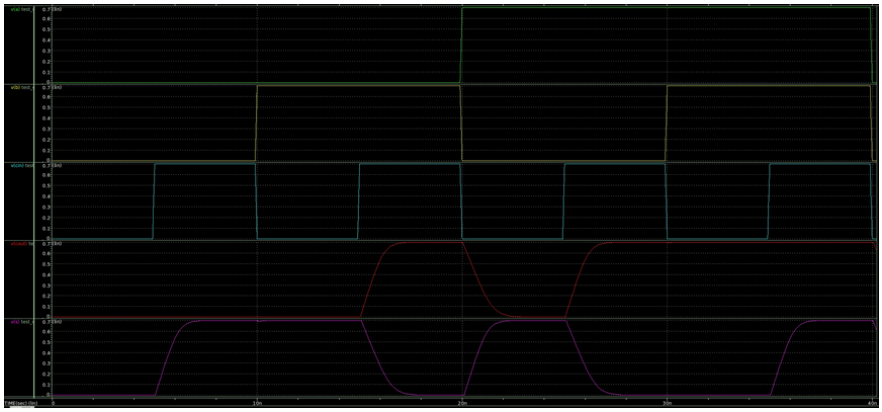

Figure 20 Waveforms of the 45nm Full Adder Test Cases(Layout)

2.b.4 Show the worst case delay and its corresponding input/output waveforms for VDD! = 0.7V.

The worst delay of full adder is shown as Figure 21. The delay of Cout is 0.8837 ns and the delay of S is 0.7914 ns. So the worst delay for this case is 0.8837ns.

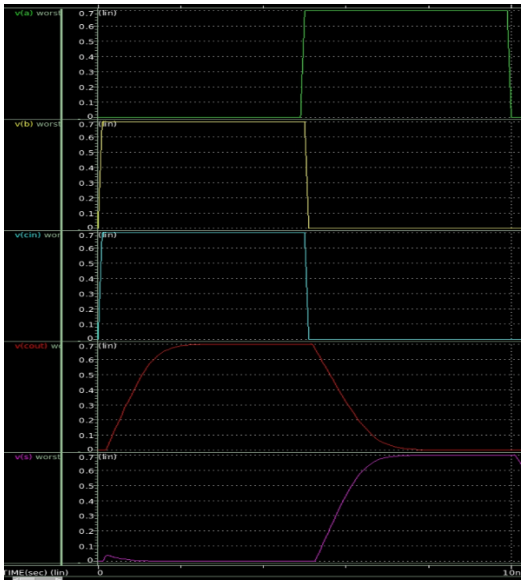

Figure 21 The Worst Delay Waveform of 45nm Full Adder(Layout)

2.b.5 Give the power consumption at the maximum operating frequency for VDD! = 0.7V.

After hspice simulation, the power_at_max is $2.667*10^{-4}$J shown in power.mt0.