EE213 2022Fall Lab1

2022231102 倪兆君

A. The test schematic of the inverter(15nm&45nm).

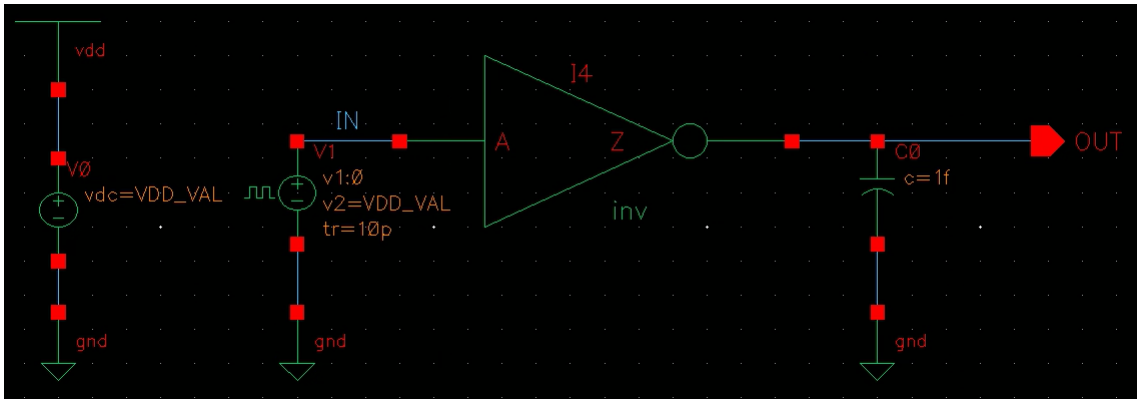

Figure 1 test schematic of the 15nm inverter

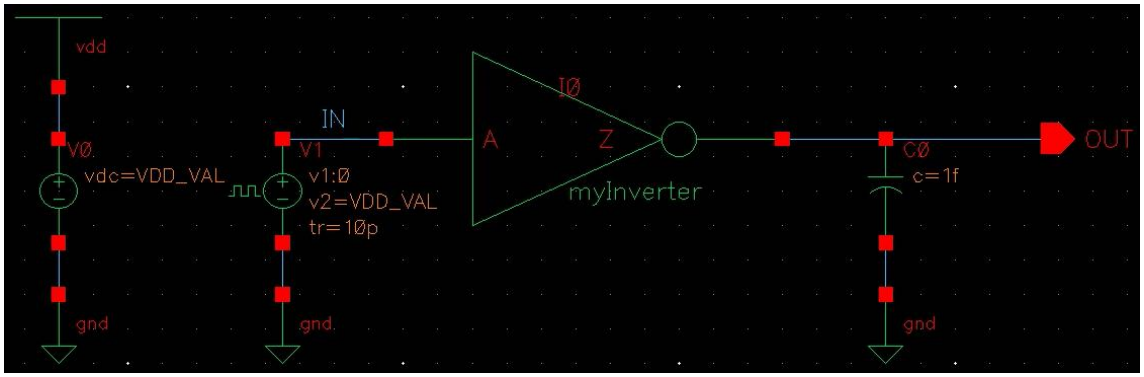

Figure 2 test schematic of the 45nm inverter

B. The layout of the inverter(15nm&45nm).

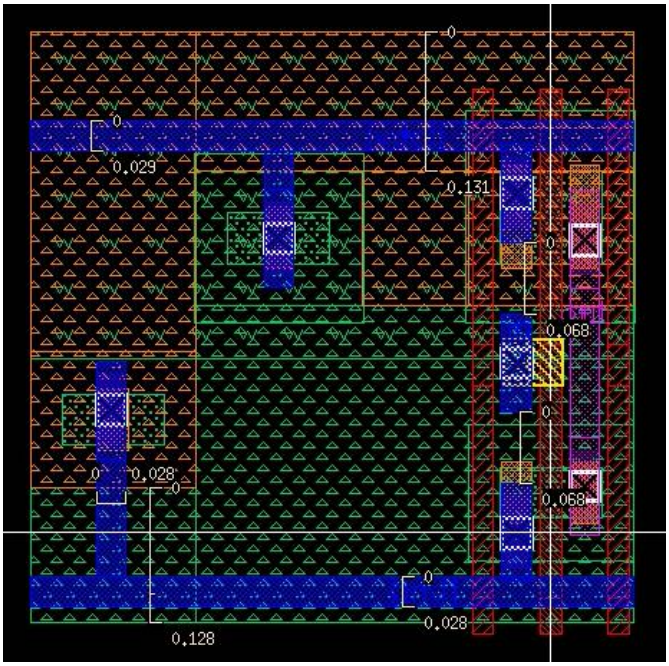

Figure 3 layout of the 15nm inverter

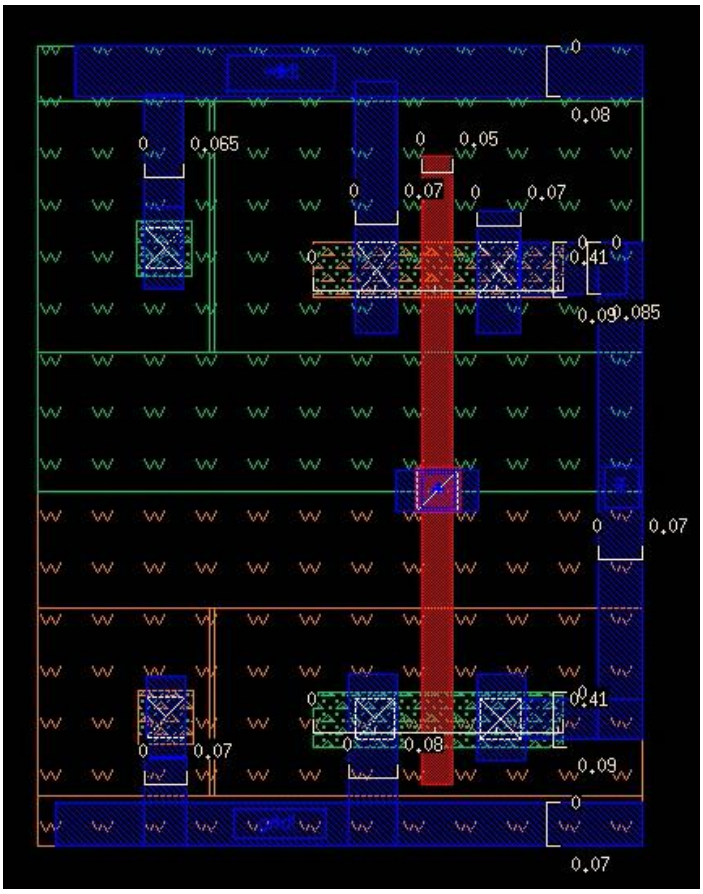

Figure 4 layout of the 45nm inverter

C. Diagrams of DRC, LVS & PEX pass.

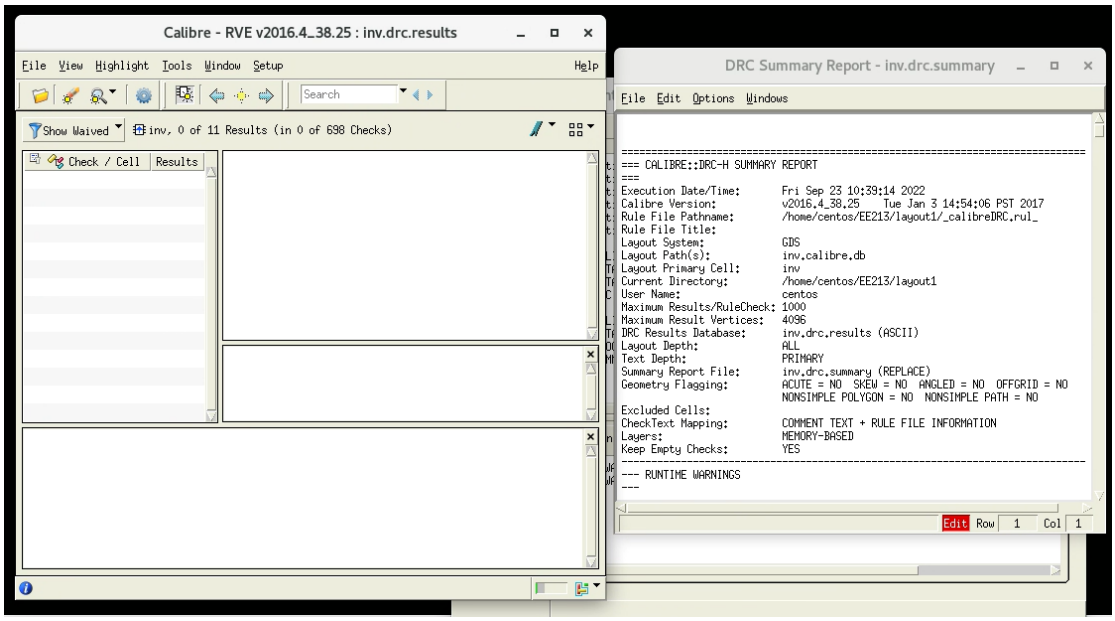

Figure 5 DRC pass of 15nm inverter layout

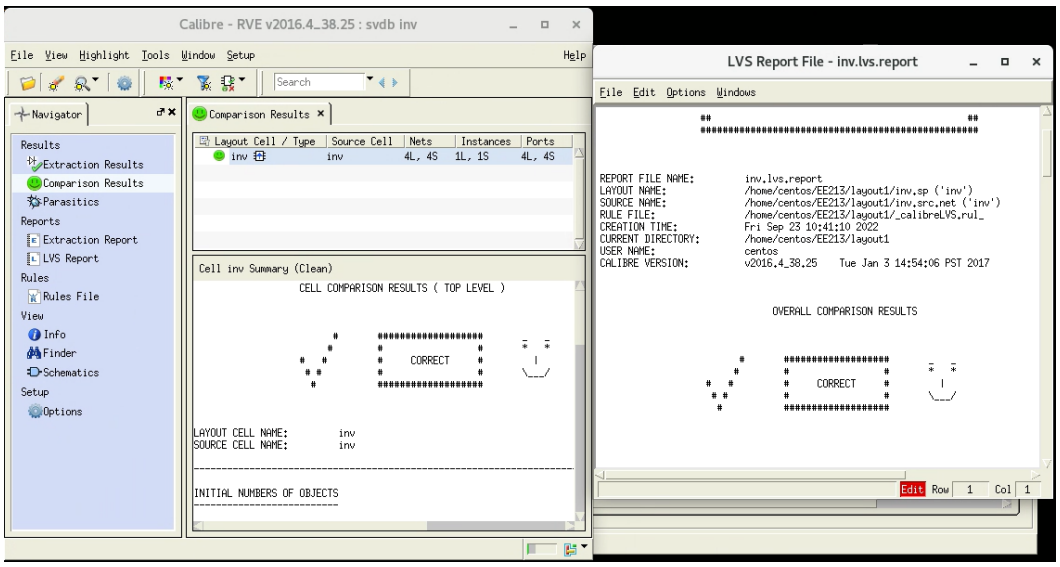

Figure 6 LVS pass of the 15nm inverter layout

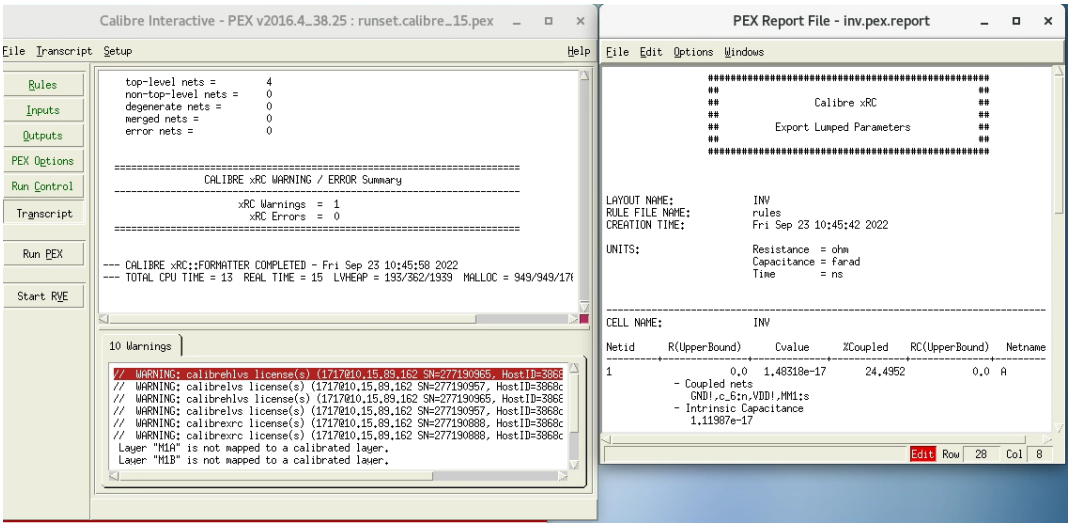

Figure 7 PEX pass of the 15nm inverter layout

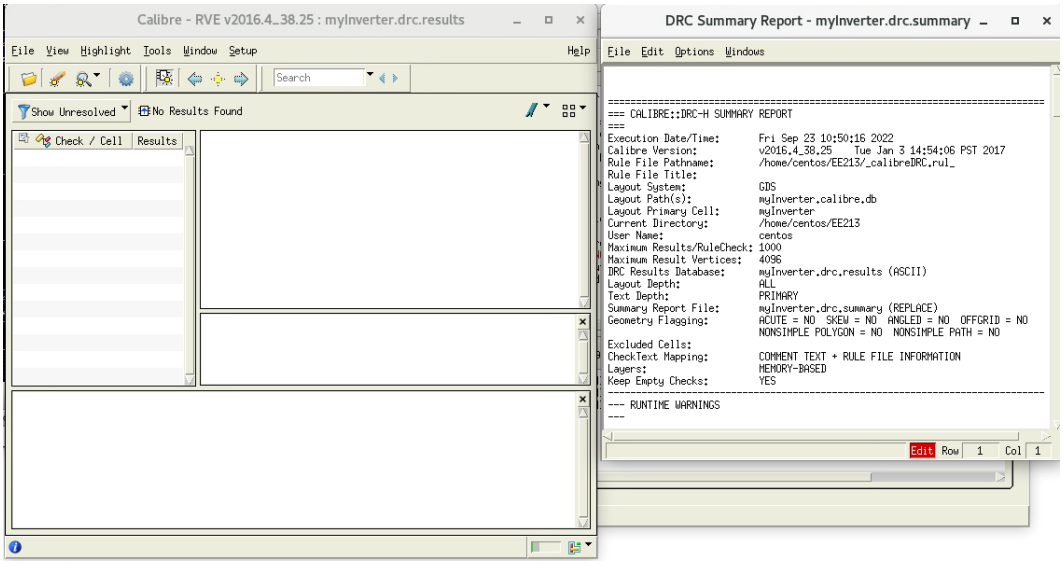

Figure 8 DRC pass of the 45nm inverter layout

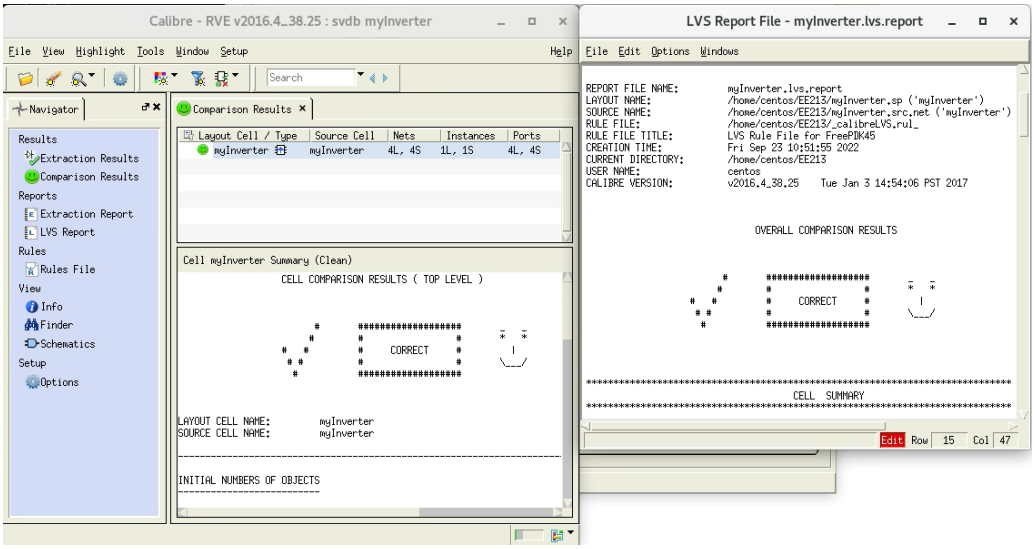

Figure 9 LVS pass of the 45nm inverter layout

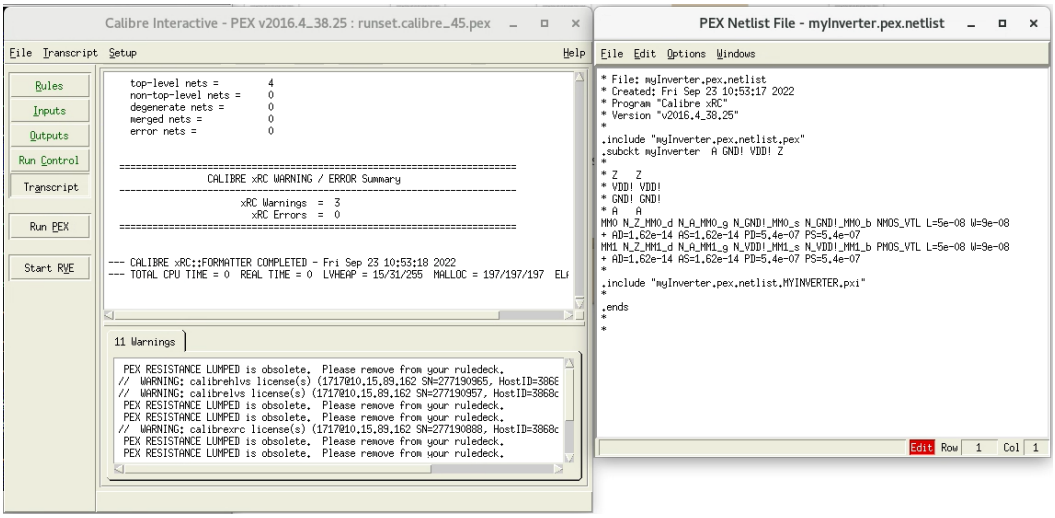

Figure 10 PEX pass of the 45nm inverter layout

D. The simulation results of schematic and layout(15nm&45nm).

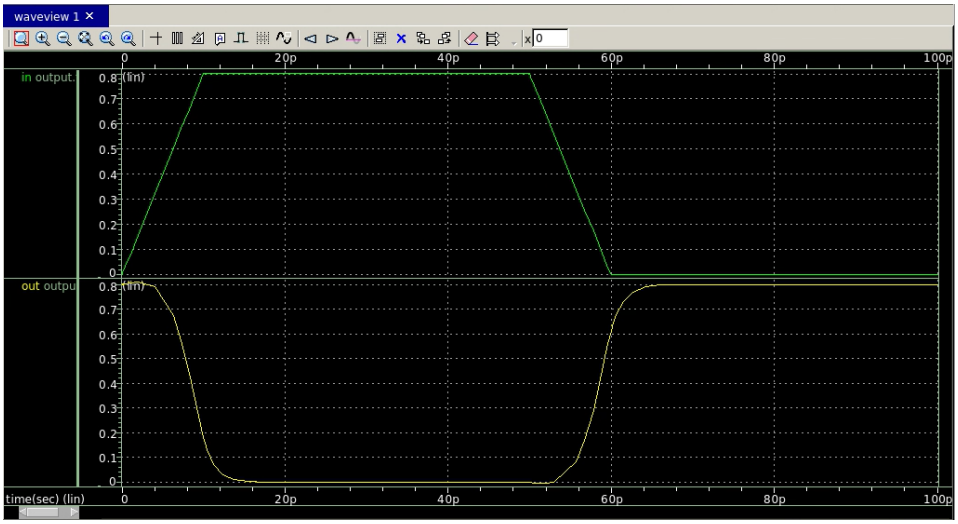

Figure 11 simulation of the 15nm inverter schematic

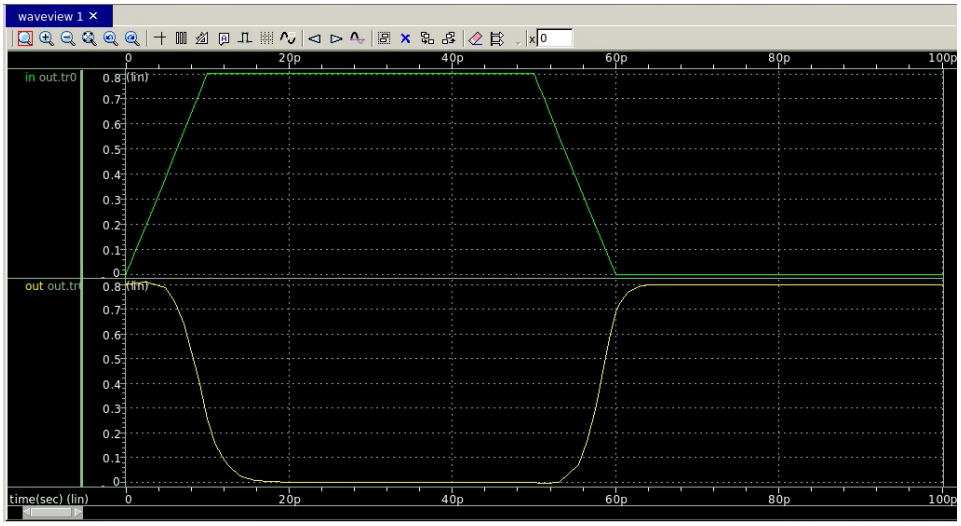

Figure 12 simulation of the 15nm inverter layout

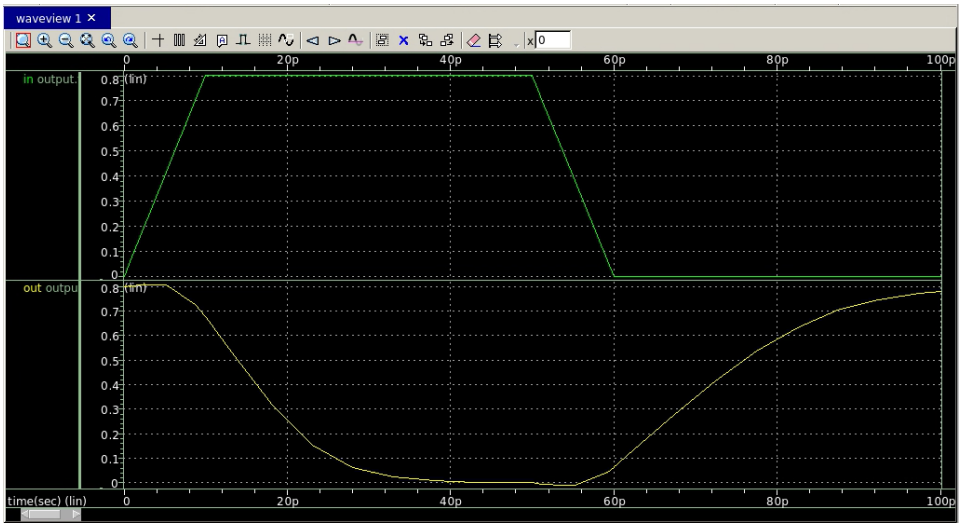

Figure 13 simulation of the 45nm inverter schematic

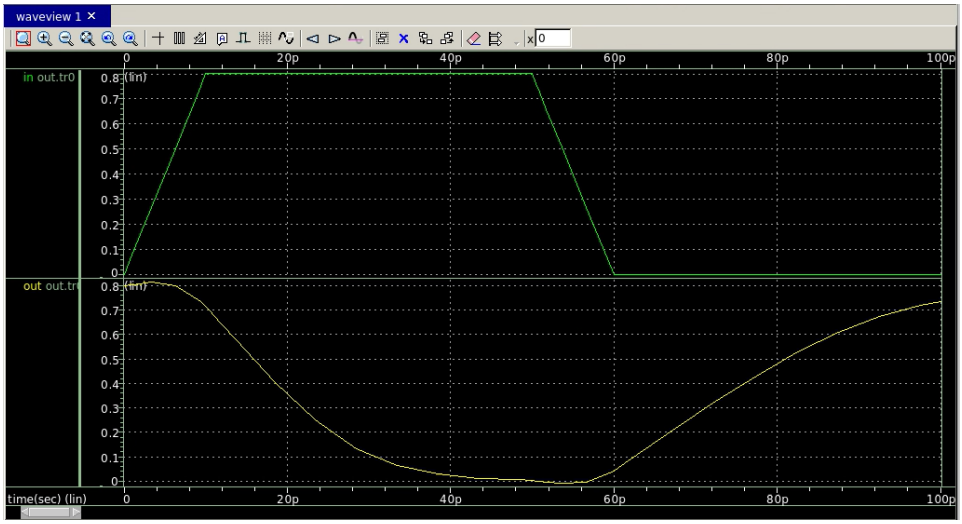

Figure 14 simulation of the 45nm inverter layout