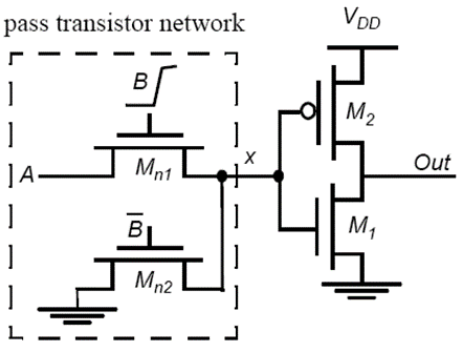
Submission:

Please submit a PDF version of your answers via Blackboard. A scanning image of the handwriting is allowed, but your submission needs to be clear enough.

Rules:

- Please try to work on your own. Discussion is permissible, but identical submissions are unacceptable!
- Please show all intermediate steps: a correct solution without an explanation will get zero credit.
- Please submit on time. Late submission will NOT be accepted.
- Please prepare your submission in English only. No Chinese submission will be accepted.

1. Consider the circuit in Figure 1. Assume the inverter switches ideally at $V_{DD}/2$, neglect body effect, channel length modulation and all parasitic capacitance throughout this problem. [10 pts]
   a) What is the logic function performed by this circuit? [2 pts]
   b) Explain why this circuit has non-zero static dissipation. [3 pts]
   c) Use only just 1 transistor to change the circuit so that there will not be any static power dissipation. Explain how you choose the size of the transistor. [2 pts]
   d) Implement the same circuit using transmission gates. [3 pts]



$V_{DD} = 2.5V$
$(W/L)_2 = 1.5um/0.25um$
$(W/L)_1 = 0.5um/0.25um$
$(W/L)_{ni} = 0.5um/0.25um$

$k_n' = 115uA/V^2$, $kp' = -30uA/V^2$
$V_{tN} = 0.43V$, $V_{tP} = -0.4V$

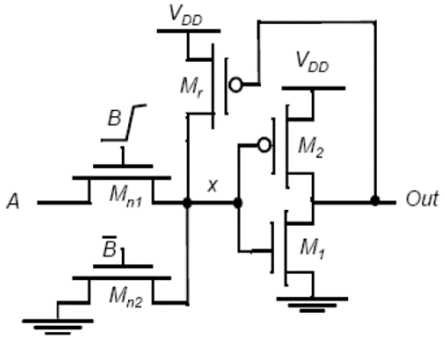
Fig. 1

Solution：

a) The circuit is a NAND gate.

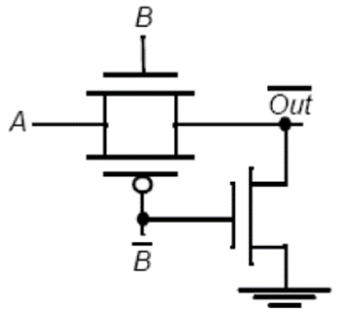
b) When $A=B=V_{DD}$, the voltage at node x is $V_x=V_{DD}-V_{Tn}$. This causes static power dissipation at the inverter the pass transistor network is driving.

c) The modified circuit is shown in the following figure.



The size of Mr should be chosen so that when one of the inputs A or B equals 0, either Mn1 or Mn2, would able to pull node X to $V_{DD}/2$ or less.

d) The circuit is shown below.



2. Consider a 1T DRAM cell whose cell node capacitance (Cs) is 25fF. Junction capacitance of each cell is 0.5fF. Assume the metal resistance and capacitance of the bitline are negligible. The supply voltage (Vdd) is 2V and the voltage stored in the DRAM cell is either 0V or 2V. The bitline is precharged to 0.5Vdd during the read process. [10 pts]

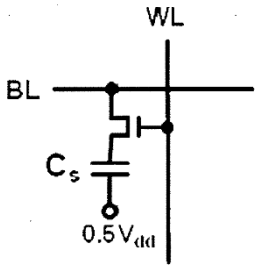


Fig. 2

a) What is the change in bitline voltage during read when there are N number of cells attached to the bitline? [6 pts]

cell data = V_{dd} case

$$\rightarrow \quad C_s \cdot (V_{dd} - 0.5V_{dd}) + \frac{V_{dd}}{2} \cdot N \cdot 0.5f$$

$$= C_s (V' - 0.5V_{dd}) + V' N \cdot 0.5f$$

$$\Delta V = V' - \frac{V_{dd}}{2}$$

$$= \frac{C_s}{C_s + N \cdot 0.5f} = \frac{50}{50 + N}$$

b) What is the maximum number of cells per bitline we can have if the bitline voltage swing during read has to be at least 200mV? [4 pts]

$$\frac{50}{50+N} \geq 200mV$$

$$\therefore \quad N \leq 200$$

1. For this problem, you should use the velocity saturated transistor model. You can assume that all transistors have a channel length of 100nm and the following parameters (unless otherwise mentioned): [20 pts]

NMOS:
V_{Tn} = 0.2V, μ_n = 400 cm^2/(V·s), C_{ox} = 1.125 μF/cm^2, v_{sat} = 1e7 cm/s, L=100nm, γ=λ=0
PMOS:
$|V_{Tp}|$ = 0.2V, μ_p = 200 cm^2/(V·s), C_{ox} = 1.125 μF/cm^2, v_{sat} = 1e7 cm/s, L=100nm, γ =λ=0

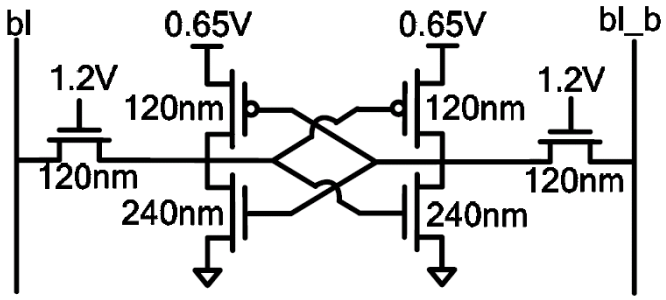
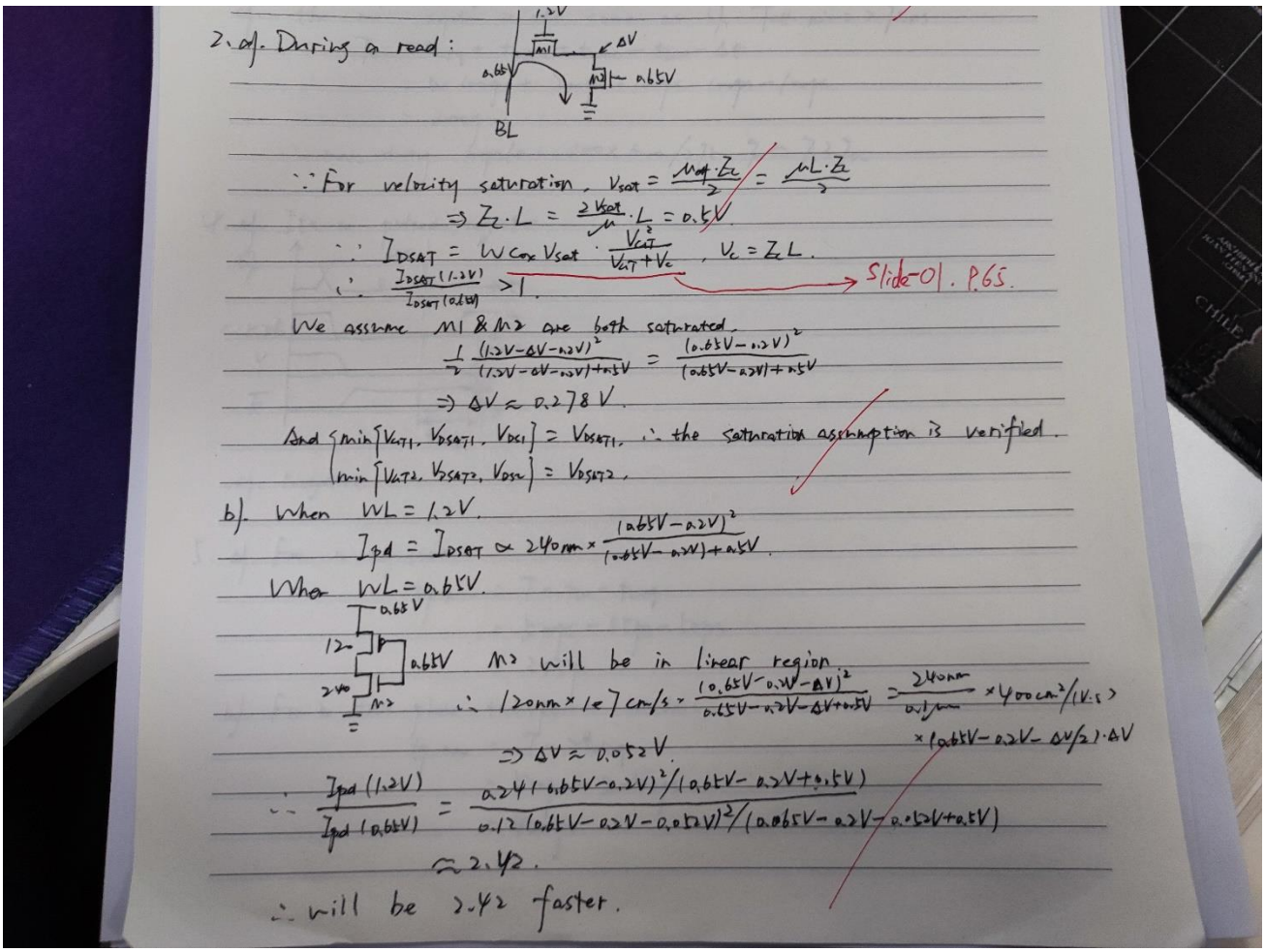


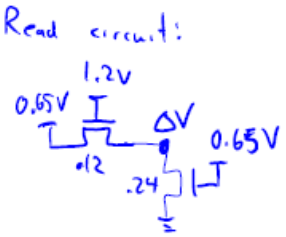
Fig.3

a) Shown below is an SRAM cell during a read, where the power supply of the SRAM has been reduced to 0.65V while the VDD of the wordline is 1.2V. Note that the bitlines have also been precharged to 0.65V. With the device sizing shown below, what is the read ΔV? (Hint: How much larger is I_{DSAT} for a transistor with V_{GS} = 1.2V than with V_{GS} = 0.65V?) [10 pts]

b) Assuming that in your answer to part a) you calculated that the pull-down device is saturated, how much faster does the SRAM cell pull down the bitline when the wordline is driven to 1.2V compared to if the wordline was driven to only 0.65V? (Note that most of the credit on this problem will be given for finding the right regions of operation and setting up the equations.) [10 pts]



Origin solution from Berkeley



$E_c L = \frac{2v_{sat}}{\mu} L = 0.5V \quad V_{TN} = 0.2V$

$\frac{I_{DSAT}\,(V_{GS}=1.2V)}{I_{DSAT}\,(V_{GS}=0.65V)} = \frac{(1.2V-0.2V)^2/(1.2V-0.2V+0.5V)}{(0.65V-0.2V)^2/(0.65V-0.2V+0.5V)} \approx 3.13$

So, even though access device is half as wide, its current would be higher than the pull-down device if $\Delta V \approx 0$. So, lets guess that both are in sat:

$\frac{1}{2}\frac{(1.2V-\Delta V-0.2V)^2}{(1.2V-\Delta V-0.2V)+0.5V} = \frac{(0.65V-0.2V)^2}{(0.65-0.2V)+0.5V} \rightarrow \boxed{\Delta V \approx 278mV}$

Check our guess:

$V_{GT\,access} = 1.2V - 278mV - 200mV = 722mV \quad V_{DSAT_a} = \frac{722mV \cdot 500mV}{722mV + 500mV} \approx 295mV$

$V_{DS\,access} = 0.65V - 278mV = 372mV$

access saturated ✓

$V_{GT\,pd} = 0.65V - 0.2V = 450mV$

$V_{DS\,pd} = 278mV \quad V_{DSAT_{pd}} = \frac{0.45V \cdot 0.5V}{0.45V + 0.5V} \approx 237mV$

pull down saturated ✓

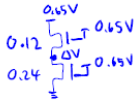
b)

When $WL = 1.2V$:

$I_{pulldown} = I_{DSAT}$ of the pull-down device

$I_{pulldown} \propto 0.24 \cdot \frac{(0.65V-0.2V)^2}{(0.65V-0.2V)+0.5V}$

When $WL = 0.65V$:



pull-down much bigger, so it should be in linear region.

Solve for ΔV:

$0.12\mu m \cdot 1e7\,cm/s \cdot \frac{(0.65V-0.2V-\Delta V)^2}{0.65V-0.2V-\Delta V+0.5V} = \frac{0.24\mu m}{0.1\mu m} \cdot 400 cm^2/Vsec\,(0.65V-0.2V-\Delta V/2)\Delta V$

$\hookrightarrow \Delta V \approx 52mV$

So, $\frac{I_{pd}(WL=1.2V)}{I_{pd}(WL=0.65V)} = \frac{0.24\,(0.65V-0.2V)^2/(0.65V-0.2V+0.5V)}{0.12\,(0.65V-0.2V-0.052V)^2/(0.65V-0.2V-0.052V+0.5V)}$

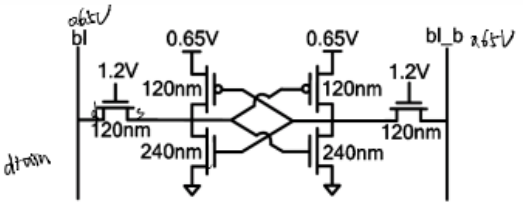
$\boxed{\frac{I_{pd}(WL=1.2V)}{I_{pd}(WL=0.65V)} \approx 2.417}$

Another solution

2. For this problem, you should use the velocity saturated transistor model. You can assume that all transistors have a channel length of 100nm and the following parameters (unless otherwise mentioned): [20 pts]

NMOS:
$V_{Tn} = 0.2V$, $\mu_n = 400\ cm^2/(V\cdot s)$, $C_{ox} = 1.125\ \mu F/cm^2$, $v_{sat} = 1e7\ cm/s$, L=100nm, $\gamma=\lambda=0$ $V_T=V_{Tn}$

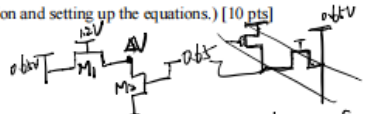
PMOS:
$|V_{Tp}| = 0.2V$, $\mu_p = 200\ cm^2/(V\cdot s)$, $C_{ox} = 1.125\ \mu F/cm^2$, $v_{sat} = 1e7\ cm/s$, L=100nm, $\gamma=\lambda=0$



a) Shown below is an SRAM cell during a read, where the power supply of the SRAM has been reduced to 0.65V while the VDD of the wordline is 1.2V. Note that the bitlines have also been precharged to 0.65V. With the device sizing shown below, what is the read ΔV? (Hint: How much larger is I_{DSAT} for a transistor with V_{GS} = 1.2V than with V_{GS} = 0.65V?) [10 pts]

b) Assuming that in your answer to part a) you calculated that the pull-down device is saturated, how much faster does the SRAM cell pull down the bitline when the wordline is driven to 1.2V compared to if the wordline was driven to only 0.65V? (Note that most of the credit on this problem will be given for finding the right regions of operation and setting up the equations.) [10 pts]

a)



Assume M_1 is in velocity saturation.
M_2 is in linear saturation.

The simplified circuit is shown above. Current through M_1, M_2 equals to each other.
Hence, we obtain the current equations:

$$k_n' \frac{W_1}{L}\left[(V_{DD}-\Delta V-V_{Tn})V_{DSAT_n}-\frac{1}{2}V_{DSAT_n}^2\right]=k_n'\frac{W_2}{L}\left[(V_{DD}-V_{Tn})\Delta V-\frac{\Delta V^2}{2}\right]$$ ← In textbook, equation (12.2).

where $V_{DSAT} \approx \frac{L v_{sat}}{\mu_n} = \frac{100nm \cdot 1e7\ cm/s}{400\ cm^2/(V\cdot s)} = 0.25V$ in the simplified analysis method for a velocity saturation case.

In textbook, equation (3.3).

$\begin{cases} V_{DD1} = 1.2V \\ V_{DD2} = 0.65V \end{cases}$

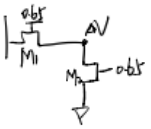
Solve out $\Delta V = 0.2405V$ or $\Delta V = 0.1V$

Since ΔV is smaller than 0.65V, $\Delta V = 0.1205V$.

For M_1, $Min(V_{GS}, V_{DS}, V_{DSAT}) = V_{DSAT} = 0.25V$
It's in the saturation region.
For M_2, $V_{GS}-V_{DS} = 0.65-0.1205 > V_T = 0.2V$.
$Min(V_{GS}, V_{DS}, V_{DSAT}) = V_{DS} = 0.2405V$. So it's in linear region.

b) When Wordline = 1.2V in part (a), M_1 is velocity saturated, M_2 is in linear region. $I_a = k_n' \frac{W_2}{L}\left[(V_{DD}-V_{Tn})\Delta V-\frac{\Delta V^2}{2}\right]$

Change WL to 0.65V, it becomes:



For M_2, $V_{GS}-V_{DS} = 0.65-\Delta V$ can not ensure the relationship with $V_T = 0.2V$.
Assume it is in the linear region.

$I_{DSAT1} = I_{linear2}$

$$k_n' \frac{W_1}{L}\left[(V_{DD}-V_T-\Delta V)(V_{DD}-\Delta V)-\frac{1}{2}(V_{DD}-\Delta V)^2\right]$$
$$= k_n' \frac{W_2}{L}\left[(V_{DD}-V_T)\Delta V-\frac{1}{2}\Delta V^2\right]$$
$$\Rightarrow \Delta V = 0.07156V$$

For M_2, $V_{GS}-V_{DS} = 0.65-0.07156 > V_T = 0.2V$.
$Min(V_{GS}, V_{DS}, V_{DSAT}) = V_{DS} = 0.07156V$. It's in linear region.

$$I_b = k_n' \frac{W_2}{L}\left[(V_{DD}-V_T)\Delta V_2-\frac{1}{2}\Delta V_2^2\right]$$
$$\frac{I_a}{I_b} = \frac{(V_{DD}-V_T)\Delta V_1-\frac{1}{2}\Delta V_1^2}{(V_{DD}-V_T)\Delta V_2-\frac{1}{2}\Delta V_2^2} = 2.54$$

Therefore, WL=1.2V condition is 2.54x faster than WL=0.65V.

3. This problem examines sources of skew and jitter. [12 pts]
   a) A balanced clock distribution scheme is shown in Figure 4. For each source of variation in Table 1, identify if it contributes to skew or jitter. [6 pts]

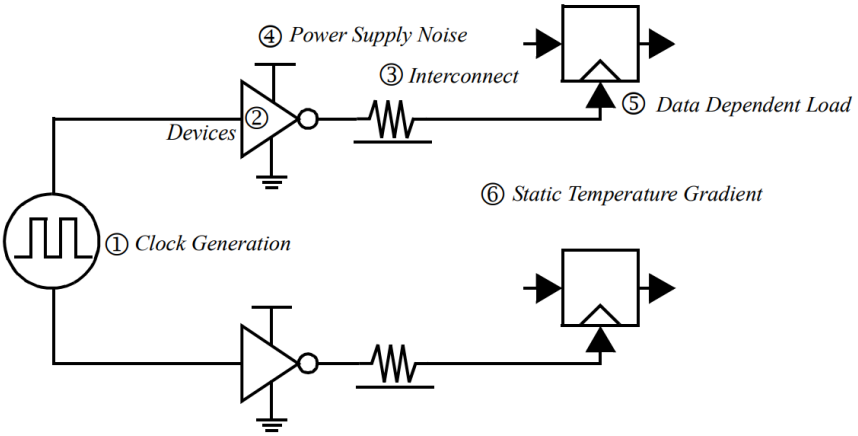


Fig. 4 Sources of Skew and Jitter in Clock Distribution.

1) Uncertainty in the clock generation circuit	Skew	(Jitter)
2) Process variation in devices	(Skew)	Jitter
3) Interconnect variation	(Skew)	Jitter
4) Power Supply Noise	Skew	(Jitter)
5) Data Dependent Load Capacitance	Skew	(Jitter)
6) Static Temperature Gradient	(Skew)	Jitter

Table 1

   b) Consider a Gated Clock implementation where the clock to various logical modules can be individually turned off as shown in Figure 5. (i.e., Enable1,..., EnableN can take on different values on a cycle by cycle basis). Which approach (A or B) results in lower jitter at the output of the input clock driver? (hint: consider gate capacitance) Explain. [6 pts]

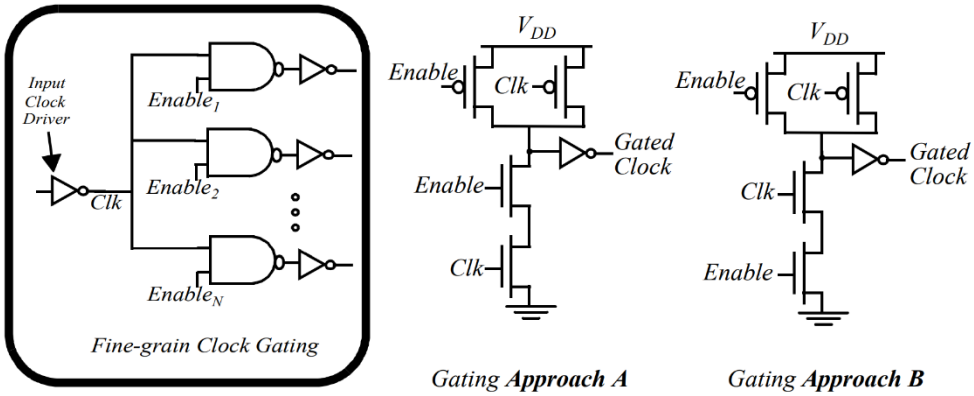


Fig. 5 Jitter in clock gating

Solution: Approach A results in lower jitter. For Approach A, the capacitance seen by CLK is independent of data (the Enable signals) to first order.

4. Sequential Logic:
   a) What type of clocking element (latch, register, or pulsed register) is the circuit given below? [3 pts]

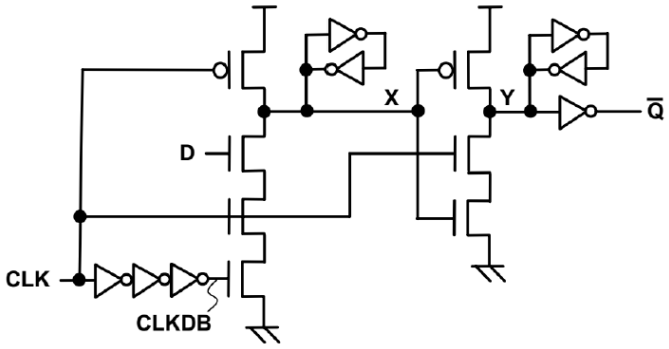


Fig. 6

Solution: Pulsed register

   b) Complete the timing diagrams of signals CLKDB, Y, and $\bar{Q}$ when D and CLK switch simultaneously. In the timing diagram, clearly show the hold time using double-headed arrows. Assume that initially, Y is Vdd and is at zero. [10 pts]

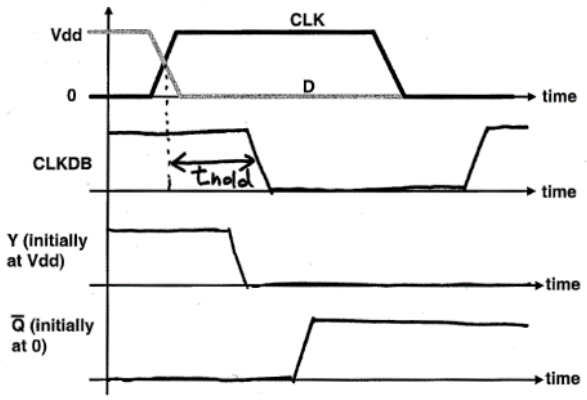


Fig. 7

   c) Is the setup time positive or negative? [3 pts]

Solution: negative

5. Determine the minimum clock period at which the circuit in Figure 8 will operate correctly for each of the following logic delays. Assume there is zero clock skew and that the latch delays are accounted for in the propagation delay Δ's. [12pts]
   a) Δ1=300ps; Δ2=400ps; Δ3=200ps; Δ4=350ps. [4pts]
   b) Δ1=300ps; Δ2=400ps; Δ3=400ps; Δ4=550ps. [4pts]
   c) Δ1=300ps; Δ2=900ps; Δ3=200ps; Δ4=350ps. [4pts]

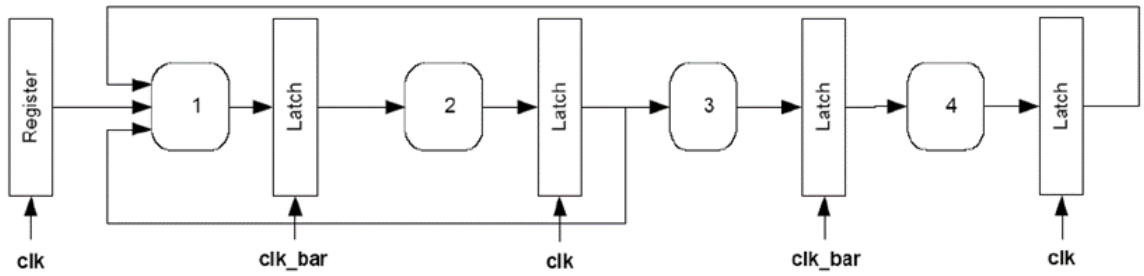


Fig. 8

Solution:

a) The minimum clock period is: 300 + 400 = 700 ps.
b) The minimum clock period is: ((300 + 400) + (400 + 550))/2 = 825 ps.
c) The minimum clock period is: 300 + 900 = 1200 ps.

6. Consider the simple state machine shown in Figure 9. A, B, and C represent combinational logic blocks with the following properties: [20 pts]

tminA = 200 psec; tmaxA = 1 nsec;
tminB = 300 psec; tmaxB = 2 nsec;
tminC = 100 psec; tmaxC = 0.5 nsec;

The L-units represent positive latches clocked by ϕ . L has a setup time of 150 psec and a delay of 250 psec ($t_{d\text{-}q}$ when latch is transparent). $T_{c\text{-}q}$ is 100 psec and thold is 100 psec. The clock ϕ has a period T and is high for a duration of T_{on}. The duty cycle of the clock hence equals 100 T_{on}/T %. [20 pts]

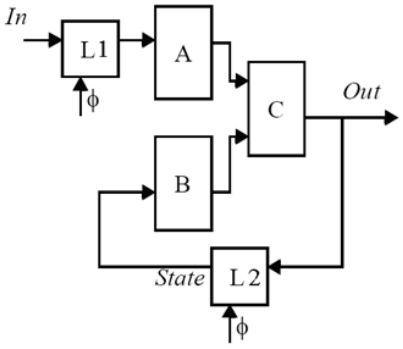


Fig. 9

a) Determine the conditions on the clock necessary to avoid the occurrence of races. [6 pts]
b) Determine the absolute minimum clock period for this circuit to work correctly as well as the maximum duty cycle. [7 pts]
c) Suppose that due to some sloppy clock-network routing, the clock signal at L1 arrives 100ps earlier than the clock signal at L2. Calculate the absolute minimum clock period for this circuit to work properly as well as the maximum duty cycle. [7 pts]

Solution:

a) Determine the conditions on the clock necessary to avoid the occurrence of races.

Race conditions occur when clock pulses are so short that input transitions meant to be latched in the next clock cycle “race” through fast-paths and appear at the output of the pipeline stage, causing data to arrive ahead of schedule. In the case of latches, what we are concerned about is the period where the latches are transparent. Race conditions put an upper bound on the transparent period (Ton). The condition to prevent race conditions is hence

$$Ton + thold \leq tc\text{-}q + tminA + tminC$$

$$Ton < 100ps + 200ps + 100ps - 100ps = 300ps$$

This requirement stems from the fact that we would like our fast path logic to reach the receiving latch after the hold time. This way, there will never be any spurious transitions within the t-setup to t-hold regions of the falling edge, thus ensuring proper values being latched.

$$Ton, min = tc\text{-}q$$

b) Determine the absolute minimum clock period for this circuit to work correctly as well as the maximum duty cycle.

There are two cases we should consider. First is if the signal happens to be launched while the latches are transparent and keeps on looping around the loop while the latches are transparent. This is the ideal case since latches are meant to be traffic lights and it would be best if we saw green all the time. For this case,

Tclk,min = td-q + tlogic,max (assuming that the latches stay transparent for a long enough period) = 2.75 ns

The other case is if the signal arrives when the latch is latched, in this case we need to meet tsetup requirements. For this case,

Tclk,min = tc-q + tlogic,max + tsetup = 2.75 ns

We would take the max of the two but they are the same in this case.
The maximum duty cycle for this case is 100*300/2750 % = 11 %

c) Suppose that due to some sloppy clock-network routing, the clock signal at L1 arrives 100ps earlier than the clock signal at L2. Calculate the absolute minimum clock period for this circuit to work properly as well as the maximum duty cycle.

This is a case of positive clock skew between L1 and L2 however since L1 is not in the critical path of the circuit, the minimum clock period remains the same as part (b). However Ton is affected by this positive skew because the input is now launched 100ps earlier into the stage. The new constraint on Ton is:

$Ton \leq tc\text{-}q + tminA + tminC - thold - \delta = 100ps + 200ps + 100ps – 100ps – 100ps= 200ps$

Hence, the maximum duty cycle is reduced to 100*600/2750 % = 7.3 %