Submission:

Please submit a PDF version of your answers via Blackboard. A scanning version of the handwriting is allowed, but your scanned image needs to be clear enough.

Rules:

- Please try to work on your own. Discussion is permissible, but identical submissions are unacceptable!
- Please show all intermediate steps: a correct solution without an explanation will get zero credit.
- Please submit on time. Late submission will NOT be accepted.
- Please prepare your submission in English only. No Chinese submission will be accepted.

1. Figure 1 shows NMOS and PMOS devices with drains, sources, and gate ports annotated. Determine the mode of operation (saturation, linear, or cutoff) and drain current I_D for each of the biasing configurations given below. Use the following transistor data: Assume $(W/L) = 1$. [12 pts]
   NMOS: $k'_n = 115\mu A/V^2$, $V_{T0} = 0.43$ V, $\lambda = 0.06$ V^{-1},
   PMOS: $k'_p = 30\ \mu A/V^2$, $V_{T0} = -0.4$ V, $\lambda = -0.1$ V^{-1}.
   a) NMOS: $V_{GS} = 2.5$ V, $V_{DS} = 2.5$ V. PMOS: $V_{GS} = -0.5$ V, $V_{DS} = -1.25$ V. [4 pts]
   b) NMOS: $V_{GS} = 3.3$ V, $V_{DS} = 2.2$ V. PMOS: $V_{GS} = -2.5$ V, $V_{DS} = -1.8$ V. [4 pts]
   c) NMOS: $V_{GS} = 0.6$ V, $V_{DS} = 0.1$ V. PMOS: $V_{GS} = -2.5$ V, $V_{DS} = -0.7$ V. [4 pts]

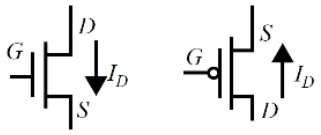

Figure 1. NMOS and PMOS devices.

(a) NMOS:

$V_{GS} = 2.5V, V_{DS} = 2.5V, V_{GS} > V_{T0}, V_{GS} - V_{T0} < V_{DS}$, saturation

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_{T0})^2(1 + \lambda V_{DS})$$

$$= \frac{115\times10^{-6}}{2}\times1\times(2.5-0.43)^2(1+0.06\times2.5) = 2.833\times10^{-4}A$$

$$= 283.3\mu A$$

PMOS: $V_{GS} = -0.5V, V_{DS} = -1.25V, |V_{GS}| > |V_{T0}|, V_{GS} - V_{T0} > V_{DS}$ saturation

$$I_D = \frac{k'_p}{2}\frac{W}{L}(V_{GS} - V_{T0})^2(1 + \lambda V_{DS})$$

$$= \frac{30}{2}\times1\times(-0.5-(-0.4))^2(1+(-0.1)\times(-1.25))$$

$$= 0.169\mu A$$

(b): NMOS: $V_{GS} = 3.3V, V_{DS} = 2.2V, V_{GS} > V_{T0}, V_{GS} - V_{T0} > V_{DS}$, linear

$I_D = k_n' \frac{W}{L}\left[(V_{GS} - V_{T0})V_{DS} - \frac{1}{2}V_{DS}^2\right]$

$=115\times 1\times\left[(3.3\text{-}0.43)\times 2.2 - \frac{1}{2}\times 2.2^2\right]=447.81\mu A$

PMOS: $V_{GS} = -2.5V, V_{DS} = -1.8V, |V_{GS}| > |V_{T0}|, V_{GS} - V_{T0} < V_{DS}$， linear

$I_D = k_p' \frac{W}{L}\left[(V_{GS} - V_{T0})V_{DS} - \frac{1}{2}V_{DS}^2\right]$

$=30\times 1\times\left[(-2.5+0.4)\times(-1.8) - \frac{1}{2}\times(-1.8)^2\right]=64.8\mu A$

(c):NMOS: $V_{GS} = 0.6V, V_{DS} = 0.1V, V_{GS} > V_{T0}, V_{GS} - V_{T0} > V_{DS}$， linear

$I_D = k_n' \frac{W}{L}\left[(V_{GS} - V_{T0})V_{DS} - \frac{1}{2}V_{DS}^2\right]$

$=115\times 1\times\left[(0.6\text{-}0.43)\times 0.1 - \frac{1}{2}\times 0.1^2\right]=1.38\mu A$

PMOS: $V_{GS} = -2.5V, V_{DS} = -0.7V, |V_{GS}| > |V_{T0}|, V_{GS} - V_{T0} < V_{DS}$， linear

$I_D = k_p' \frac{W}{L}\left[(V_{GS} - V_{T0})V_{DS} - \frac{1}{2}V_{DS}^2\right]$

$=30\times 1\times\left[(-2.5+0.4)\times(-0.7) - \frac{1}{2}\times(-0.7)^2\right]=36.75\mu A$

2. The data from five measurements made on a short channel NMOS device is shown in the Table 1 below.

Given that $V_{DSAT} = 0.6V$ and $k' = 100uA$, calculate V_{T0}, γ, λ, $2|\phi_F|$, and $\frac{W}{L}$. [10 pts]

Measurement Number	V_{GS}	V_{DS}	V_{BS}	I_D
1	2.5 V	1.8 V	0	1812 μA
2	2 V	1.8 V	0	1297μA
3	2 V	2.5 V	0	1361 μA
4	2 V	1.8 V	-1 V	1146 μA
5	2 V	1.8 V	-2 V	1039 μA

Table 1. Measured Data for Short Channel NMOS

(Hint: add the channel length modulation term for short channel device)

for a short channel NMOS transistor：

$$I_D = \mathrm{k}' \frac{W}{L}(V_{GT}V_{\min} - \frac{V_{\min}^2}{2})(1+\lambda V_{DS}) \ ,$$

when，$V_{\min} = \min(V_{GT}, V_{DS}, V_{DSAT}), V_{GT} = V_{GS} - V_T$

First，the operation region should be determined。

Supposed that these were to be in saturation，V_T should be：$V_{GT} = V_{GS} - V_T < V_{DSAT}$

$$V_{GT} = V_{GS} - V_T < V_{DSAT}$$

$\therefore 2 - V_T < 0.6 \Rightarrow V_T > 1.4$，this assumption is not reasonable.

We can assume that all data are taken in velocity saturation，then check this assumption。
In velocity saturation：

$$I_D = \mathrm{k}' \frac{W}{L}((V_{GS} - V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2})(1+\lambda V_{DS})$$

Group 1 and 2：

$$I_D = \mathrm{k}' \frac{W}{L}[(2.5 - V_{T0}) \times 0.6 - \frac{0.6^2}{2}](1 + \lambda \times 1.8) = 1812$$

$$I_D = \mathrm{k}' \frac{W}{L}[(2 - V_{T0}) \times 0.6 - \frac{0.6^2}{2}](1 + \lambda \times 1.8) = 1297$$

$$\frac{1812}{1297} = \frac{(2.5 - V_{T0}) \times 0.6 - \frac{0.6^2}{2}}{(2 - V_{T0}) \times 0.6 - \frac{0.6^2}{2}} \Rightarrow V_{T0} = 0.44V$$

$V_{T0} < 1.4V$, so 1,2,3 are in velocity saturation.

Group 2 and 3：

$$\frac{1297}{1361}=\frac{1+\lambda\times1.8}{1+\lambda\times2.5}\Rightarrow\lambda=0.08V^{-1}$$

Then we can get: $\frac{W}{L}=15$

Group 2 and 4: $$\frac{1297}{1146}=\frac{(2-0.44)\times0.6-\frac{0.6^2}{2}}{(2-V_T)\times0.6-\frac{0.6^2}{2}}\Rightarrow V_T=0.587V$$

Group 2 and 5: $$\frac{1297}{1039}=\frac{(2-0.44)\times0.6-\frac{0.6^2}{2}}{(2-V_T)\times0.6-\frac{0.6^2}{2}}\Rightarrow V_T=0.692V$$

All of the values satisfy : $V_{T0}<1.4V$, so the data in the table were taken in velocity saturation.

$$V_T=V_{T0}+\gamma(\sqrt{|-2\phi_F+V_{SB}|}-\sqrt{|-2\phi_F|})$$

$$\text{since: } V_T=0.587V,\ V_T=0.692V,\ V_{T0}=0.44V,$$

$$\Rightarrow|2\phi_F|=0.6\text{V},\gamma=0.3V^{1/2}$$

3. Short-channel effects: [8 pts]

a) Please demonstrate the current model IDSAT for a short-channel device in the condition of Velocity Saturation. (Notice: write down detailed derivation) [5 pts]

b) Based on the result of a) and the function of drain current in saturation, describe the most important differences between short-channel and long-channel devices. [3 pts]

Solution:

(a) assuming the following two-region piecewise empirical model for the velocity versus electric field for electron in the inversion layer：

$$v=\frac{\mu_n E}{1+E/E_C}, E \le E_C \qquad (1)$$
$$= v_{sat}, \quad E > E_C$$

Where E is the lateral electric field and E_C is the critical field at which the carriers are velocity saturated and is equal to $2v_{sat}/\mu_n$, μ_n is the mobility of electron.

To derive the current equation we first write the current at any point x along the channel as:

$$I_D = I(x) = WC_{OX}(V_G^{'} - V(x))v(x) \qquad (2)$$

Where W is the device width，

C_{OX} is the gate capacitance per unit area，

V(x) is the potential difference between minority-carrier quasi-Fermi potential and equilibrium Fermi potential in the bulk at point x，

$v(x)$ is the velocity of carriers at point x.

$V_G^{'}$ is the gate-source voltage minus the extrapolated threshold votage.

From the velocity field model in (1) we can express the lateral electric field E(x) as:

$$E(x) = \frac{I_D}{W\mu_n C_{OX}(V_G^{'} - V(x)) - I_D/E_C} = \frac{dV(x)}{dx} \qquad (3)$$

By integrating from x=0 to x=L and $V(x)=V_S$ to $V(x)=V_D$ we arrive at:

$$I_D = \frac{W\mu_n C_{OX}(V_G^{'} - V_{DS}/2)V_{DS}}{L(1+V_{DS}/E_C L)}, V_{DS} \le V_{DSAT} \qquad (4)$$

We define the saturation voltage to be the drain voltage at which the carriers at the drain become velocity saturated. It corresponds to the point at which the lateral electric field at the drain end of the channel becomes equal to the critical field E_C. Substituting the above condition into (3) we get:

$$I_D = \frac{W\mu_n C_{OX}(V_G^{'} - V_{DSAT})E_C}{2} = v_{sat}WC_{OX}(V_{GS} - V_T - V_{DSAT}) \qquad (5)$$

(When E(x)=E_c, V(x)=V_{DSAT}, and $\upsilon_{sat}=\mu_n E_c/2$)

By equating (4)、(5) we can solve for V_{DSAT}:

$$V_{DSAT} = \frac{E_C L V_G^{'}}{E_C L + V_G^{'}} = \frac{E_C L (V_{GS} - V_T)}{E_C L + (V_{GS} - V_T)}$$

(b) The most important differences between short-channel and long channel devices is that it's easy for short-channel devices to reach in E_C and operate in saturation.

4. The circuit shown below is known as the source follower configuration. It achieves a DC level shift between the input and the output. The value of this shift is determined by the current I_0. Assume $\gamma = 0$, $2|\phi_F| = 0.6V$, $V_{T0} = 0.43V$, $k_n{}' = 115uA/V^2$ and $\lambda = 0$. Suppose we want the nominal level shift between V_i and V_o to be 0.6V in the circuit in Fig.2. Neglecting the backgate effect, calculate the width of M2 to provide this level of shift. (Hint:

first relate V_i to V_o in terms of I_o) [8 pts]

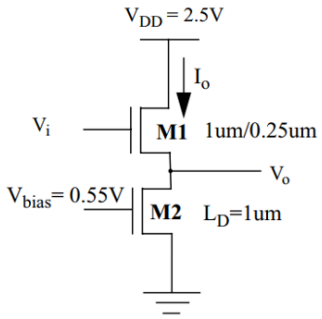

Figure 2. Source follower configuration

Solution

The level shift of 0.6 tells us that V_{GS1}=0.6 so V_{GT1}=0.17. This means that **M1** must be in the saturation region (not velocity saturated). Thus,

$\frac{k'_n \cdot \frac{W}{L}}{2} \cdot (V_{GS} - V_T)^2 = I_D$, and I_D=6.647μ A.

For **M2**, V_{GT}=0.12, so **M2** also is in the saturation region (not velocity saturated). Using the same equation as above and solving for W/L gives **W/L = 8.**

5. Table 2 shows a set of measurements performed on a newly fabricated MOSFET by an EE student. We would like to obtain more information about their parameters. You are convinced that these measurements are correct and a few assumptions will get you the information that you need. [20 pts]

   Hint: refer to Page 104 of *Digital Integrated Circuits-A Design Perspective (2nd Ed)*.

Table 2. Measurements of a MOSFET.

Measurement Number	V_{GS}	V_{DS}	V_{SB}	I_D	Operation Region
1	-0.4 V	-0.8 V	0	-12.05 µA	
2	0.4 V	-0.8 V	0	0	
3	-0.8 V	-0.8 V	0	-88.98 µA	
4	-0.5 V	-0.8 V	0	-26.42 µA	
5	-0.4 V	-0.8 V	-0.5 V	-7.17 µA	
6	-0.8 V	-0.55 V	0	-76.45 µA	
7	-0.8 V	-0.25 V	0	-53.21 µA	

You may assume that velocity saturation voltage $|V'_{DSAT}| = 0.4$ V and $|2\phi_F| = 0.6$ V.

a) Is the measured transistor a PMOS or an NMOS device? Explain your answer. [5 pts]

b) From measurement above, determine the following parameters: V_{T0}, γ, λ. [7 pts]
(Hint: you can start with Measurement 1 and 4 and assume the operation mode.)

c) Complete the missing column in the table above using the values you obtained so far. [8 pts]

Solution:

(a) This is a PMOS device. Negative VGS and VDS and negative ID are your biggest hint.

(b) We select data points 1 and 4 from the above table. We start with the assumption that the transistor is in the saturation region for these points. Use the saturation current model and solve for V_{T0}.

Substituting numeric values from the above table gives V_{T0}=-0.192V.

Note: Check whether the assumption for region of operation is correct.

$$\frac{I_{D1}}{I_{D2}} = \frac{\frac{1}{2}k'\left(\frac{W}{L}\right)(V_{SG1} - |V_{T0}|)^2(1 + \lambda V_{SD1})}{\frac{1}{2}k'\left(\frac{W}{L}\right)(V_{SG4} - |V_{T0}|)^2(1 + \lambda V_{SD4})} = \frac{(V_{SG1} - |V_{T0}|)^2}{(V_{SG4} - |V_{T0}|)^2}$$

Using the same methodology as in V_{T0} extraction above, we can find V_T by using data point 5 that corresponds to V_{SB}= –0.5V. By repeating the above calculations for data points 1 and 5 we get V_T = –0.2395V.

Now we can use the threshold formula to calculate γ parameter.

$$|V_T| = |V_{T0}| + \gamma(\sqrt{V_{SB} + |2\phi F|}) - \sqrt{|2\phi F|}$$

Substitution of numerical values gives $\gamma = -0.104\nu^{\frac{1}{2}}$

Parameter λ is extracted by picking two points with the same V_{GS} but different V_{DS}. We choose data points 3 and 6. Using the velocity saturation current model, we can solve for λ

$$\frac{I_{D3}}{I_{D6}} = \frac{1+\lambda V_{DS3}}{1+\lambda V_{DS6}}$$

Data values in the table give $\lambda = -1.025v^{-1}$

(c) **Sol:** Since VDSAT is given and we have determined VT, we can simply use the Vmin formula (since this is a PMOS, we use Vmax instead) to determine mode of operation.

Vmax	VGT	VDS	VDSAT
Mode	saturated	linear	velocity-sataturated

Table below summarizes operational modes.

Measurement Number	V_{GT} [V]	V_{DS} [V]	V_{DSAT} [V]	Operation Region
1	-0.2	-0.8	-0.4	Saturation
2	--	--	--	I_D=0 → Off
3	-0.6	-0.8	-0.4	Vel-Saturation
4	-0.3	-0.8	-0.4	Saturation
5	-0.15	-0.8	-0.4	Saturation
6	-0.6	-0.5	-0.4	Vel-Saturation
7	-0.6	-0.2	-0.4	Linear

*use VT instead of VT0 (body bias)

6. Use the following table for the purpose of capacitance calculation. [12 pts]

Parameter	C_{ox} [fF/um^2]	C_o [fF/um^2]
NMOS	15	0.27
PMOS	14	0.25

Assume $|V_T| = 0.2V$ for both NMOS and PMOS, and treat velocity saturation as saturation.

a) What is the t_{ox} of the NMOS transistor? [4 pts]

b) Consider a PMOS biased with $V_G = V_D = V_S = V_B = 0V$. Assume $W = 480nm$, $L = 120nm$, $L_D = L_S = 240nm$. Calculate the Gate-to-Channel capacitance(C_{GC}) and the Gate-to-Source capacitance(C_{GS}). [4 pts]

c) Consider a NMOS biased with $V_G = V_D = 0.8V$, $V_S = V_B = 0V$. Assume $W = 240nm$, $L = 120nm$, $L_D = L_S = 240nm$. Calculate the Gate-to-Channel capacitance(C_{GC}) and the Gate-to-Source capacitance(C_{GS}). [4 pts]

a)

Sol: By definition, $C_{ox} = \varepsilon_{ox} / t_{ox} \rightarrow t_{ox} = \varepsilon_{ox} / C_{ox}$
where ε_{ox} is the physical constant ($\varepsilon_{ox} = 3.5 \times 10^{-13}$ F/cm)

t_{ox} = 2.33nm

b)

Sol: PMOS with zero bias → mode of operation is cut-off

(B1) Gate-to-Channel capacitance (C_{GC})
$C_{GC} = WLC_{ox} = 0.48\mu m \times 0.12\mu m \times 14fF/\mu m^2 = 0.81fF$
C_{GC} = 0.81fF

(B2) Gate-to-Source capacitance (C_{GS})
$C_{GS} = C_{GCS} + C_{GSO}$

Cutoff mode:
$C_{GCS} = 0$
$C_{GSO} = WC_o = 0.48\mu m \times 0.25fF/\mu m = 0.12$ fF
C_{GS} = 0.12fF

c)

Sol: NMOS bias → mode of operation is velocity-saturation

(C1) Gate-to-Channel capacitance (C_{GC})
$C_{GC} = 2/3WLC_{ox} = 2/3 \times 0.24\mu m \times 0.12\mu m \times 15fF/\mu m^2 = 0.288fF$
C_{GC} = 0.29fF

(C2) Gate-to-Source capacitance (C_{GS})
$C_{GS} = C_{GCS} + C_{GSO}$

Velocity saturation:
$C_{GCS} = C_{GC} = 0.29fF$
$C_{GSO} = WC_o = 0.24\mu m \times 0.27fF/\mu m = 0.065fF$
C_{GS} = 0.35fF

7. Short Channel MOS [15pts]

For the short-channel device shown in Fig.3, given that $V_{dd} = 2.5\,V, V_{t0} = 0.4\,V, \gamma = 0.1\,V^{0.5}$, velocity saturation voltage $V'_{dsat} = 1\,\mathrm{V}, 2\phi_F = 0.6\,V$.

(a) Determine the different operation modes of the device while V_o is changed from 0 to V_{dd}. [10 pts]

(b) Derive the condition for V_o at the boundary of each operation mode. You do NOT need to calculate the actual value of V_o. [5 pts]

Hint: Threshold voltage $\mathrm{V}_t = \mathrm{V}_{t0} + \gamma(\sqrt{2\emptyset_F + \mathrm{V}_{SB}} - \sqrt{2\emptyset_F})$.

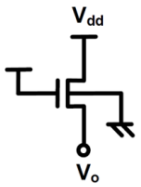

Figure 3. Short Channel MOS

Solution:

When $0<\mathrm{V_o}<1.1\mathrm{V}$, velocity saturation mode

When $1.1\mathrm{V}<\mathrm{V_o}<2\mathrm{V}$, saturation mode

When $2\mathrm{V}<\mathrm{V_o}<2.5\mathrm{V}$, off

From velocity saturation mode to saturation mode, $\mathrm{V_o} \approx 1.1\mathrm{V}$

$\mathrm{V_{gs}}\text{-}\mathrm{V_t} = \mathrm{V_{DSAT}}$, hence, $2.5\text{-}0.4\text{-}\gamma\,(\sqrt{2\phi_F + V_o} - \sqrt{2\phi_F})\text{-}\,V_o = 1\mathrm{V}$

From saturation mode to off, $\mathrm{V_o} \approx 2\mathrm{V}$

$V_o = \mathrm{V_g}\text{-}\mathrm{V_t}$, hence, $2.5\text{-}0.4\text{-}\gamma\,(\sqrt{2\phi_F + V_o} - \sqrt{2\phi_F}) = V_o$

8. An NMOS device is plugged into the test configuration shown below in Figure 4. The input $V_{in} = 2V$. The current source draws a constant current of 50 μA. R is a variable resistor that can assume values between 10 kΩ and 30 kΩ. Transistor M1 experiences short channel effects and has following transistor parameters: $k' = 110 * 10^{-6}V/A^2$, $V_T = 0.4V$, and $V_{DSAT} = 0.6V$. The transistor has a W/L = 2.5μ/0.25μ. For simplicity, body effect and channel length modulation can be neglected. i.e λ=0, γ=0. [15 pts]
   a) When R =10 kΩ, find the operation region of the transistor, and the values of V_D and V_S. [5 pts]
   b) When R= 30 kΩ, again determine the operation region, V_D and V_S. [5 pts]
   c) For the case of R = 10 kΩ, would V_S increase or decrease if λ≠0. Explain qualitatively. [5 pts]

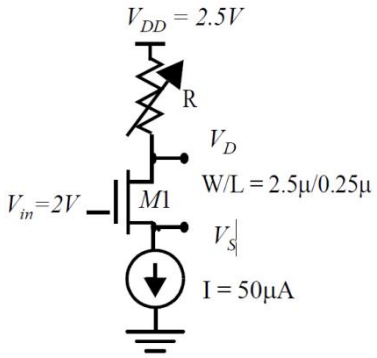

Figure 4. Test configuration for the NMOS device.

a) When R=10k, $V_D=V_{DD}$-IR, so V_D=2V, assume the device is in saturation (needs to be verified eventually.).

$$I_D = \frac{k'}{2}\frac{W}{L}(V_{GS} - V_t)^2 = 50\mu A$$

So V_{GS}-V_T=0.3v, V_{GS}=0.7v, Vs=1.3v.

$$V_{min} = \min(V_{GS} - V_T, V_{DSAT}, V_{DS}) = \min(0.3, 0.6, 0.7) = V_{GS} - V_T$$

So saturation verified.

b) V_D=2.5v-1.5v=1v, assume linear region.

$$I_D = k'\frac{W}{L}((V_{GS} - V_t)V_{DS} - V_{DS}^2) = 50\mu A$$

So Vs=0.93v.

$$V_{min} = \min(V_{GS} - V_T, V_{DSAT}, V_{DS}) = V_{DS}$$

So linear verified.

c) Increase. V_D is fixed. $(1+\lambda V_{DS})$ term would try to increase the current more than available 50μA. Thus, V_{GS} needs to reduce by increasing Vs

9. [BONUS] Short Channel MOS [10 pts]

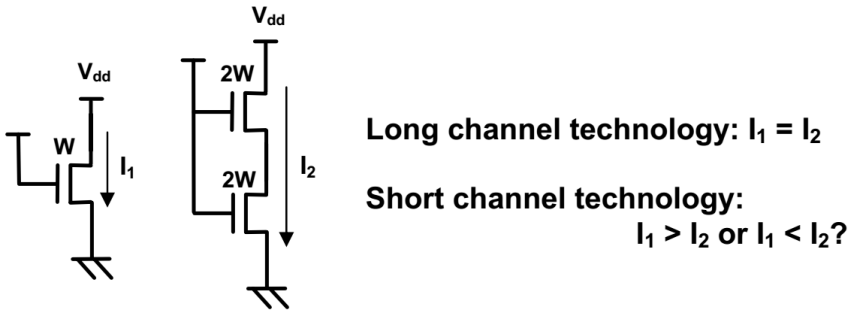

Figure 5. The circuit of long channel/ short channel technology.

In a long channel technology (without velocity saturation), assume a 2-stack with NMOS widths of 2W has the same current as a single NMOS with a width of W (i.e., $I_1 = I_2$). In a short channel technology with velocity saturation, which of the following is true?

a) $I_1 > I_2$

b) $I_1 < I_2$

Explain your answer.

Hint: Current of a velocity saturated device does not decrease as much as a long channel device when V_{ds} is reduced. Load line analysis can be helpful in figuring out the stack current.