EE213 Lab2

2022231102 Zhaojun Ni

Assignment #1 Static Device Characteristics

1) I_{DS}-V_{DS} & coefficient of channel length modulation

a) I_{DS}-V_{DS} Curve

45nm case: Shown as Figure1.

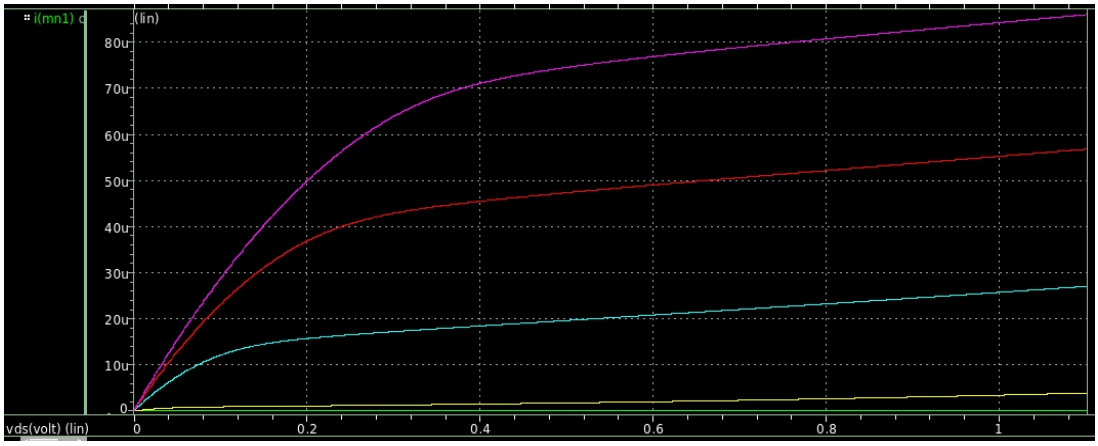


Figure 1 I_{DS}-V_{DS} Curve of 45nm NMOS

7nm case: Shown as Figure2.

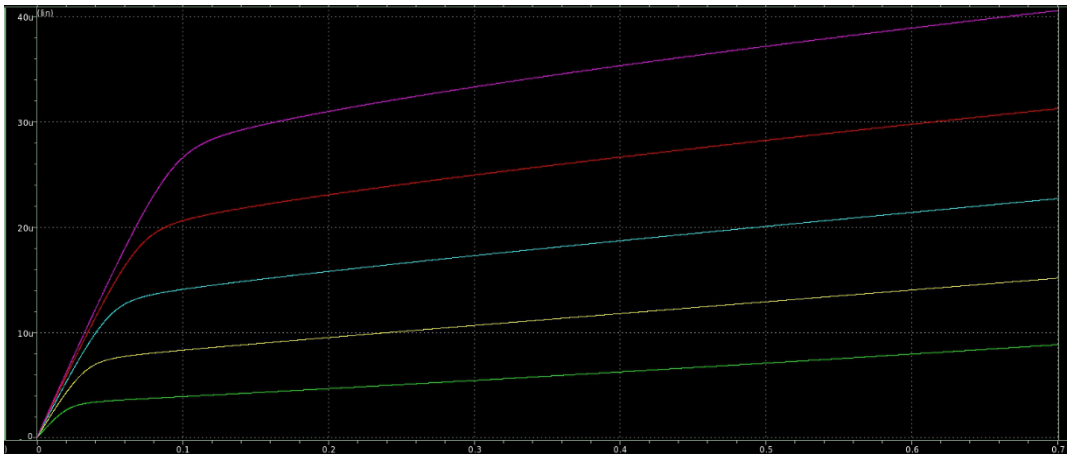


Figure 2 I_{DS}-V_{DS} Curve of 7nm NMOS

b) coefficient of channel length modulation

Then I will describe how to calculate λ for NMOS. As we all know, the calculation formula of the modified saturation current is: (Equation 1.1)

$$I_{DS} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS}) \tag{1.1}$$

Given the fixed V_{GS}, we can measure the I_{DS} values of two points with different V_{DS} values (but on the curve with the same color), substitute then into equation1.1 and then divide.

I use a cursor in Custom WaveView to measure the values, and get the following result.

45nm case: When V_{GS}=0.9V,V_{DS}=1.0V,I_{DS}=84.2μA, when V_{GS}=0.9V,V_{DS}=1.1V,I_{DS}=86μA.

$$\frac{86}{84.2}=\frac{1+1.1\lambda}{1+1.0\lambda}$$

By solving the above equation, get λ=0.272.

7nm case: When V_{GS}=0.5V,V_{DS}=0.6V,I_{DS}=38.9μA, when V_{GS}=0.5V,V_{DS}=0.7V,I_{DS}=40.5μA.

$$\frac{40.5}{38.9}=\frac{1+0.7\lambda}{1+0.6\lambda}$$

By solving the above equation, get λ=0.546.

However, when I try to use another fixed V_{GS} to calculate λ, I find them different greatly. Since λ may be the function of V_{GS} and it is not a constant for a certain MOSFET, I draw a table for different λ-V_{GS} pairs for 45nm & 7nm NMOS as shown as Table 1 & Table 2.

Table 1 The Relationship between λ&V_{GS} for 45nm NMOS

V_{GS}(V)	I_{DS}(μA) V_{DS}=1.0V	I_{DS}(μA) V_{DS}=1.1V	λ
0.1	0	0	N/A
0.3	3.45	3.91	-4.000
0.5	25.8	27	0.870
0.7	55.3	56.8	0.372
0.9	84.2	86	0.272

Table 2 The Relationship between λ&V_{GS} for 7nm NMOS

V_{GS}(V)	I_{DS}(μA) V_{DS}=1.0V	I_{DS}(μA) V_{DS}=1.1V	λ
0.3	7.95	8.84	3.410
0.35	14	15.2	1.765
0.4	21.4	22.7	0.956
0.45	29.8	31.2	0.654
0.5	38.9	40.5	0.546

2) I_{DS}-V_{GS} & subthreshold slope & V_{TH} & body coefficient & DIBL

a) I_{DS}-V_{GS} Curve (V_{DS}=Vdd,V_{BS}=0V)

Note: for the convenience of slope calculation in the next step, the ordinate(I_{DS}) is the logarithmic coordinate!

45nm case: Shown as Figure3.

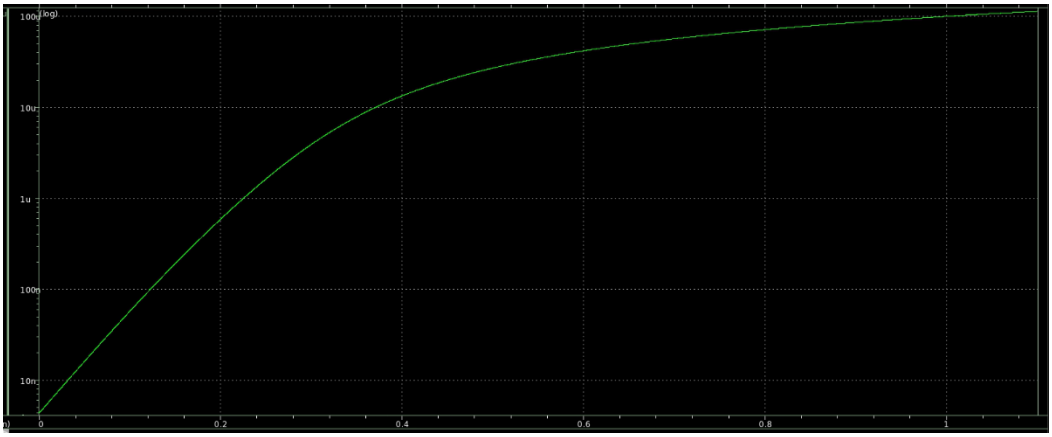


Figure 3 I_{DS}-V_{GS} Curve of 45nm NMOS(with Logarithmic Coordinate)

7nm case: Shown as Figure4.

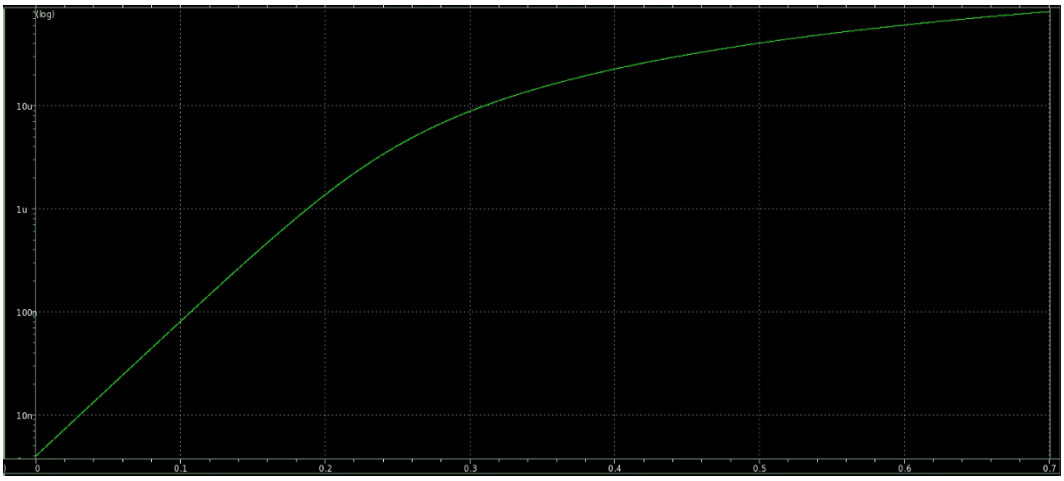


Figure 4 I_{DS}-V_{GS} Curve of 7nm NMOS(with Logarithmic Coordinate)

b) subthreshold slope

I use two H-cursors in Custom WaveView to measure the V_{GS} when I_{DS}=10nA or 100nA.

45nm case: V_{GS}=31.6mV when I_{DS}=10nA, V_{GS}=123mV when I_{DS}=100nA.

$$\boldsymbol{S} = 123\text{-}31.6 = 91.4\text{mV/decade}$$

7nm case: V_{GS}=30.6mV when I_{DS}=10nA, V_{GS}=107mV when I_{DS}=100nA.

$$\boldsymbol{S} = 107\text{-}30.6 = 76.4\text{mV/decade}$$

c) V_{TH}

Since the given V_{DS}=V_{dd}, so the NMOS works in either 'cut-off' mode or 'saturate' mode. Thus, I read the paper in slide 68 and use **Extrapolation method in the region**, which is mentioned in its 3.1 section.

The method contains the following steps:

a)Plot the $I_D^{0.5} - V_g$ curve.

b)Find its maximum slope point.

c)Find its V_g axis intercept($I_D^{0.5} = 0$).

45nm case: The $I_D{}^{0.5} - V_g$ curve and its derivate curve is shown as Figure5.

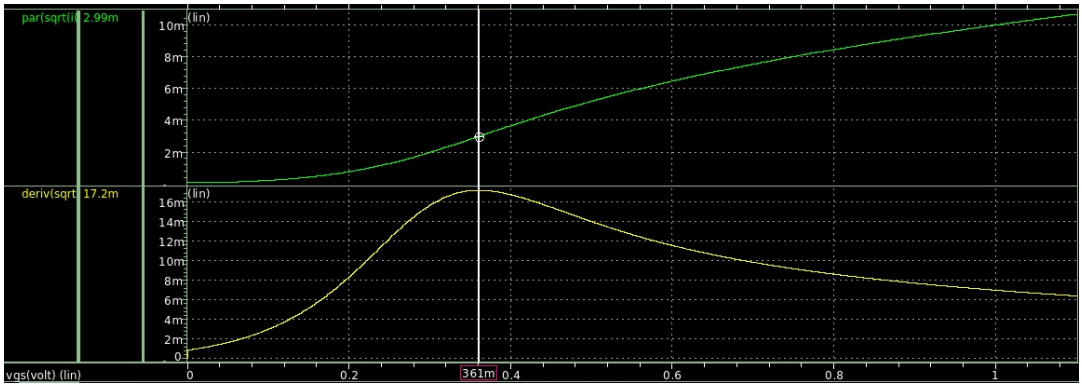


Figure 5 The $I_D{}^{0.5}$-V_g Curve & The 1st Order Derivate Curve of $I_D{}^{0.5}$-V_g in 45nm NMOS

We can see the derivative reaches maximum 17.2m at V_{GS}=0.361V. And then we assume the tangent equation as $y = 17.2mx + b$.Then we use the point $(0.361, 2.99m)$ in the green curve and get the final tangent equation as $y = 17.2mx - 3.2192m$ .Therefore we get the intercept x = 3.2192/17.2 = 0.187V.

Thus, I determine V_{TH}=0.186V for 45nm NMOS.

Figure 1 can verify my conclusion. The bottom curves are plotted with V_{GS}=0.1V(green color) & V_{GS}=0.3V(yellow color). The green curve is in 'cut-off' mode while the yellow curve is not. It indicates that the V_{TH} should be higher than 0.1V and lower than 0.3V, which is consistent with my result.

7nm case: The $I_D{}^{0.5} - V_g$ curve and its derivate curve is shown as Figure6.

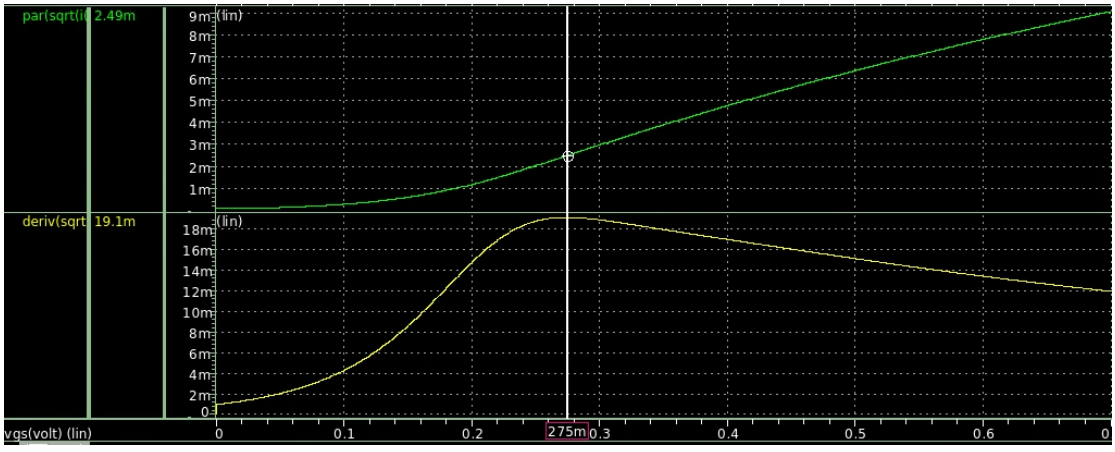


Figure 6 The $I_D{}^{0.5}$-V_g Curve & The 1st Order Derivate Curve of $I_D{}^{0.5}$-V_g in 7nm NMOS

We can see the derivative reaches maximum 19.1m at V_{GS}=0.275V. And then we assume the tangent equation as $y = 19.1mx + b$.Then we use the point $(0.275, 2.49m)$ in the green curve and get the final tangent equation as $y = 19.1mx - 2.7625m$ .Therefore we get the intercept x =

2.7625/19.1 = 0.145V.

Thus, I determine V_{TH}=0.145V for 7nm NMOS.

Figure 1 can verify my conclusion. The curves are plotted with V_{GS}>0.3V. And they all work fine. It indicates that the V_{TH} should be lower than 0.3V, which is consistent with my result.

d) body coefficient

45nm case: Find V_{TH} with the same steps as c).

Since V_{BS} varies from -1.1V to 0V, I use 0.1V as gap and plot 12 points for V_{TH} as shown in Table 3 & the relationship curve in shown as Figure7..

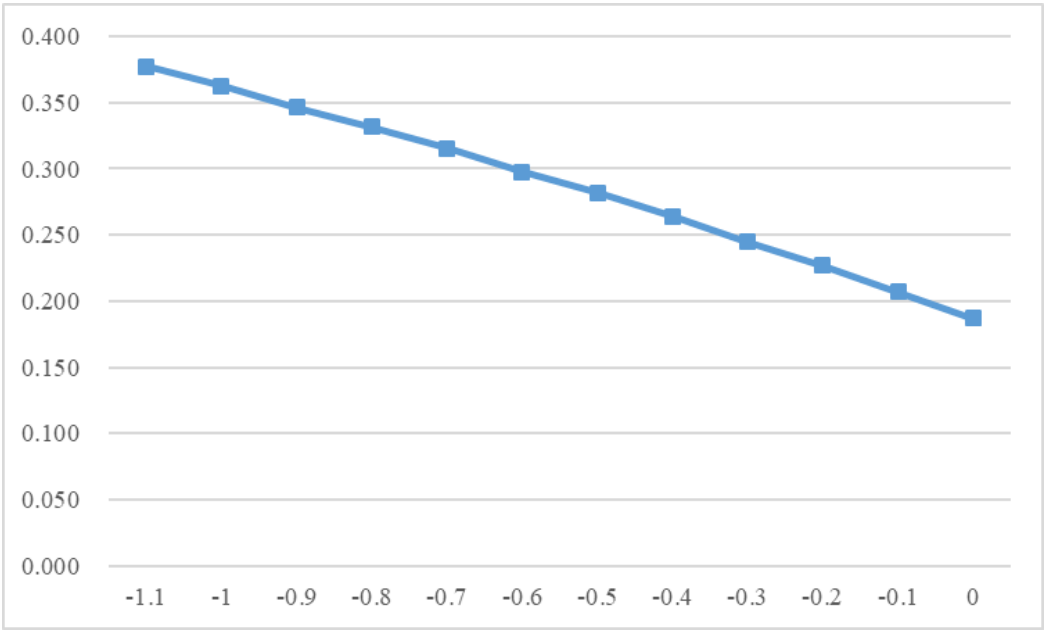


Figure 7 The Relationship Curve between V_{TH} & V_{BS} for 45nm NMOS

Table 3 The Relationship between V_{TH} & V_{BS} for 45nm NMOS

V_{BS} (V)	MAX derivate (mV)	V_{GS} (V)	$I_{DS}^{0.5}$ ($mA^{0.5}$)	V_{TH} (V)
-1.1	15.7	0.553	2.76	0.377
-1.0	15.8	0.537	2.76	0.362
-0.9	15.9	0.522	2.79	0.347
-0.8	16.1	0.506	2.81	0.331
-0.7	16.2	0.49	2.83	0.315
-0.6	16.3	0.473	2.86	0.298
-0.5	16.5	0.455	2.86	0.282
-0.4	16.6	0.438	2.89	0.264
-0.3	16.7	0.419	2.91	0.245
-0.2	16.9	0.401	2.94	0.227
-0.1	17	0.378	2.91	0.207
0	17.2	0.361	2.99	0.187

The threshold voltage equation with body-bias effect is shown as Equation 1.2.

$$V_T = V_{T0} + \gamma(\sqrt{\varphi_s + V_{SB}} - \sqrt{\varphi_s}) \quad (1.2)$$

Given $\varphi_s = 0.93V$ and the data above in the table, the coefficient of body-effect γ can be worked out. $0.377 = V_{T0} + \gamma(\sqrt{0.93+1.1} - \sqrt{0.93})$, $0.207 = V_{T0} + \gamma(\sqrt{0.93+0.1} - \sqrt{0.93})$

$\gamma = 0.415$ for 45nm NMOS.

7nm case:

Since V_{BS} varies from -1.1V to 0V, I use 0.1V as gap and plot 12 points for V_{TH} as shown in Table 4 & the relationship curve in shown as Figure8.

Table 4 The Relationship between V_{TH} & V_{BS} for 7nm NMOS

V_{BS} (V)	MAX derivate (mV)	V_{GS} (V)	$I_{DS}^{0.5}$ ($mA^{0.5}$)	V_{TH} (V)
-1.1	19.1	0.275	2.49	0.145
-1	19.1	0.275	2.49	0.145
-0.9	19.1	0.275	2.49	0.145
-0.8	19.1	0.275	2.49	0.145
-0.7	19.1	0.275	2.49	0.145
-0.6	19.1	0.275	2.49	0.145
-0.5	19.1	0.275	2.49	0.145
-0.4	19.1	0.275	2.49	0.145
-0.3	19.1	0.275	2.49	0.145
-0.2	19.1	0.275	2.49	0.145
-0.1	19.1	0.275	2.49	0.145
0	19.1	0.275	2.49	0.145

The V_{TH} is not affected by V_{BS} at all in 7nm case!!!

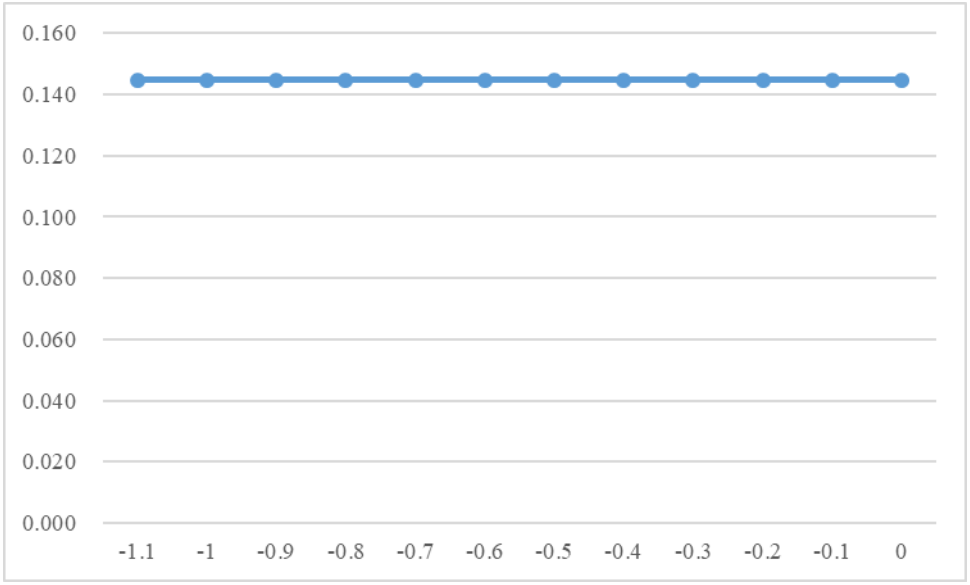


Figure 8 The Relationship Curve between V_{TH} & V_{BS} for 7nm NMOS

e) DIBL

45nm case: Find V_{TH} with the same steps as c).

The derivative reaches maximum 14.1m at V_{GS}=0.398V. And then we assume the tangent equation as $y = 14.1mx + b$.Then we use the point $(0.398, 2.17m)$ in the green curve and get the final tangent equation as $y = 14.1mx - 3.4418m$ .Therefore we get the intercept x = 3.4418/14.1 = 0.244V. Thus, I determine V_{TH} = 0.244V for 45nm NMOS.

Now let's take DIBL into account. When V_{DS} = 0.1V, V_{TH} = 0.244V; when V_{DS} = 1.1V, V_{TH} = 0.187V. The DIBL equation is as the following. (Equation 1.3)

$$V_t^{'} = V_t - \eta V_{ds} \tag{1.3}$$

Thus, $\eta = \dfrac{0.244 - 0.187}{1.1 - 0.1} = 0.057$ for 45nm NMOS.

7nm case: Find V_{TH} with the same steps as c).

The derivative reaches maximum 18.2m at V_{GS}=0.325V. And then we assume the tangent equation as $y = 18.2mx + b$.Then we use the point $(0.325, 2.44m)$ in the green curve and get the final tangent equation as $y = 18.2mx - 3.475m$ .Therefore we get the intercept x = 3.475/18.2 = 0.191V. Thus, I determine V_{TH} = 0.191V for 7nm NMOS.

Now let's take DIBL into account. When V_{DS} = 0.1V, V_{TH} = 0.191V; when V_{DS} = 0.7V, V_{TH} = 0.145V. The DIBL equation is as the following. (Equation 1.2)

$$V_t^{'} = V_t - \eta V_{ds} \tag{1.2}$$

Thus, $\eta = \dfrac{0.191 - 0.145}{0.7 - 0.1} = 0.077$ for 7nm NMOS.

3) Temperature

45nm case:

When V_{GS}=0.1V, the NMOS is OFF, I_{DS} increases with temperature. (Shown as Figure 9)

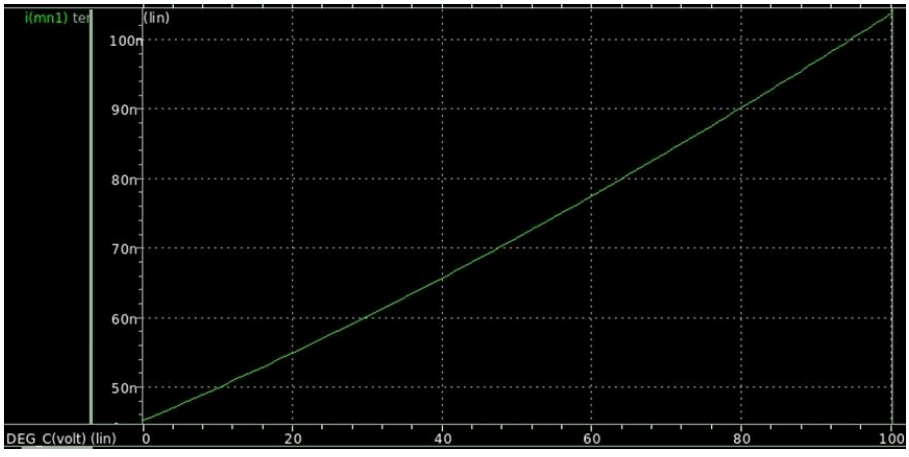


Figure 9 I_{DS}-Temperature Curve of 45nm NMOS(OFF)

When V_{GS}=0.5V, the NMOS is ON, I_{DS} decreases with temperature. (Shown as Figure 10)

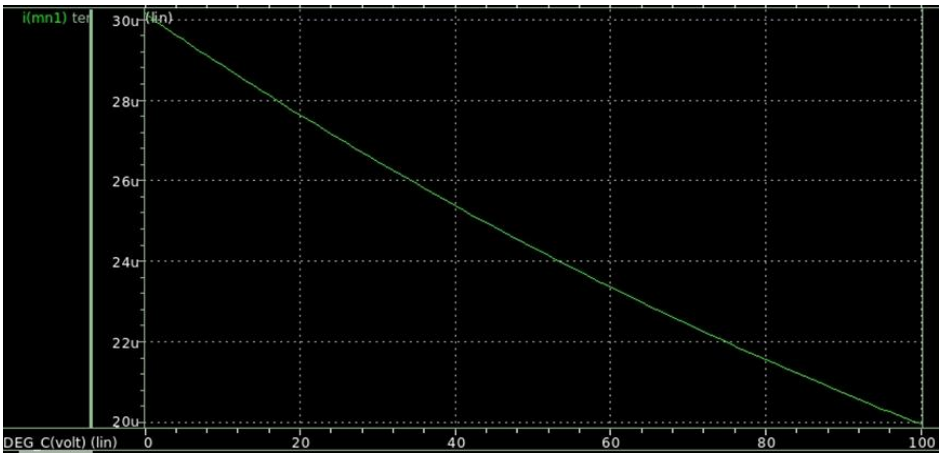


Figure 10 I_{DS}-Temperature Curve of 45nm NMOS(ON)

7nm case:

When V_{GS}=0.1V, the NMOS is OFF, I_{DS} increases with temperature. (Shown as Figure 11)

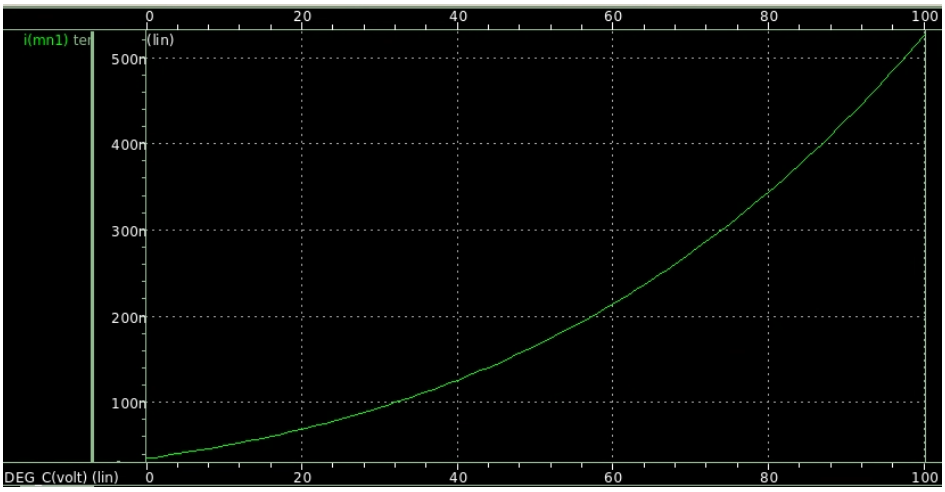


Figure 8 I_{DS}-Temperature Curve of 7nm NMOS(OFF)

When V_{GS}=0.5V, the NMOS is ON, I_{DS} **also** increases with temperature. (Shown as Figure 12)

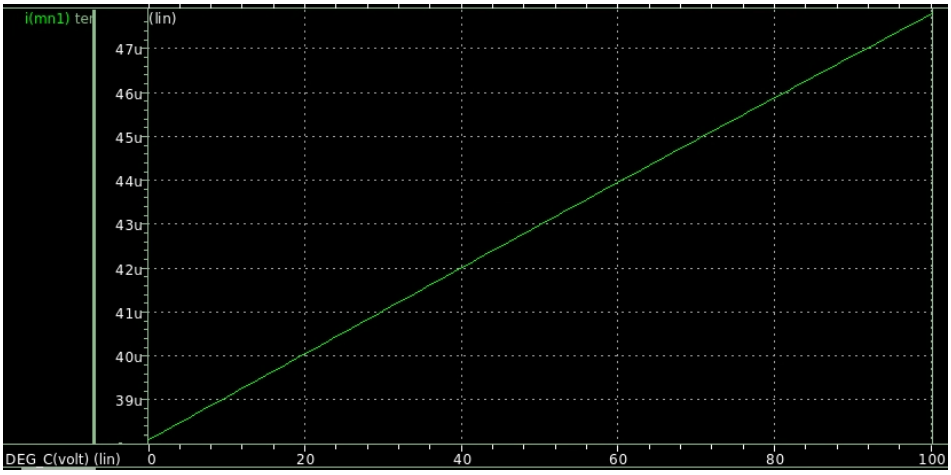


Figure 12 I_{DS}-Temperature Curve of 7nm NMOS(ON)

Assignment #2 R/C-V Characteristics

1) Resistance of a transistor

According to Topic-01 P84,when $V_{GS}=V_{DD}$ and V_{DS} ranges from $V_{DD}/2$ to V_{DD}, I_{DS} can be seen as linear. So R_{on} can be approximated by Equation 2.1.

$$Req = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1+\lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1+\lambda V_{DD}/2)}\right) = \frac{1}{2}(R_0 + R_{mid}) \qquad (2.1)$$

Thus, I calculate the ratio between V_{DS} and I_{DS} to get R when V_{DS} is $V_{DD}/2$ or V_{DD}. Then I take the average value as the resistance of a transistor.

45nm case:

The solution of Req of 45nm NMOS & PMOS in shown as Table 5 and the Req-V_{DD} curve for 45nm NMOS & PMOS is shown as Figure13.

Table 5 R_{eq} Variation with respect to V_{DD} Value for 45nm NMOS & PMOS

	NMOS			PMOS		
V_{DD}(V)	R_{mid}(kΩ)	R_0(kΩ)	R_{eq}(kΩ)	R_{mid}(kΩ)	R_0(kΩ)	R_{eq}(kΩ)
0.4	34.1	54.8	44.45	32.3	49.1	40.70
0.6	9.98	17.3	13.64	9.78	16.2	12.99
0.8	6.81	12	9.41	6.52	11.1	8.81
1	5.74	10.2	7.97	5.33	9.18	7.26
1.2	5.22	9.27	7.25	4.73	8.17	6.45
1.4	4.93	8.75	6.84	4.36	7.53	5.95
1.6	4.75	8.43	6.59	4.13	7.05	5.59
1.8	4.64	8.2	6.42	3.98	6.61	5.30

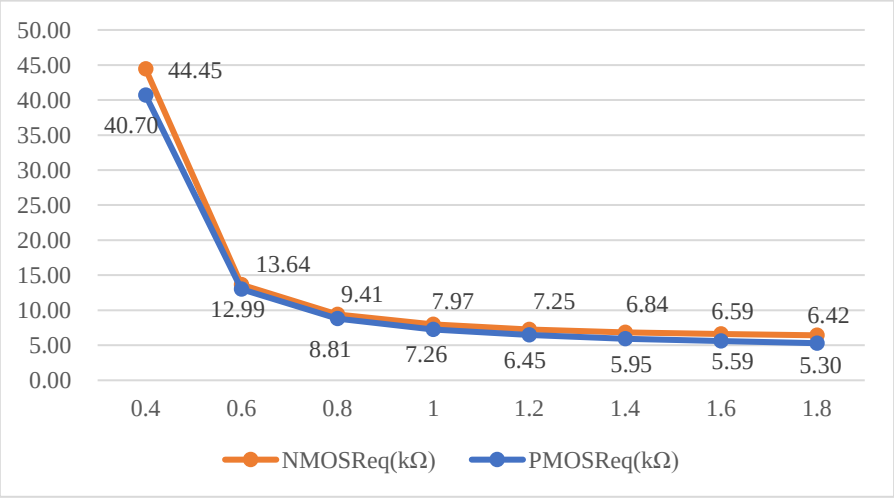


Figure 13 The R_{eq}-V_{DD} Curve for 45nm NMOS & PMOS

7nm case:

The solution of Req of 7nm NMOS & PMOS in shown as Table 6 and the Req-V_{DD} curve for 45nm NMOS & PMOS is shown as Figure14. Since the resistance in 7nm differs a lot, the Req-axis is in **logarithmic coordinate** in Figure14..

Table 6 R_{eq} Variation with respect to V_{DD} Value for 7nm NMOS & PMOS

	NMOS			PMOS		
V_{DD}(V)	R_{mid}(kΩ)	R_0(kΩ)	R_{eq}(kΩ)	R_{mid}(kΩ)	R_0(kΩ)	R_{eq}(kΩ)
0.2	292	445	368.50	419	605	512.00
0.4	12.7	21.4	17.05	15.4	25.1	20.25
0.6	5.86	10.2	8.03	6.84	11.7	9.27
0.8	4.32	7.51	5.92	4.98	8.5	6.74
1	3.7	6.34	5.02	4.25	7.14	5.70
1.2	3.39	5.7	4.55	3.91	6.4	5.16
1.4	3.24	5.29	4.27	3.76	5.93	4.85

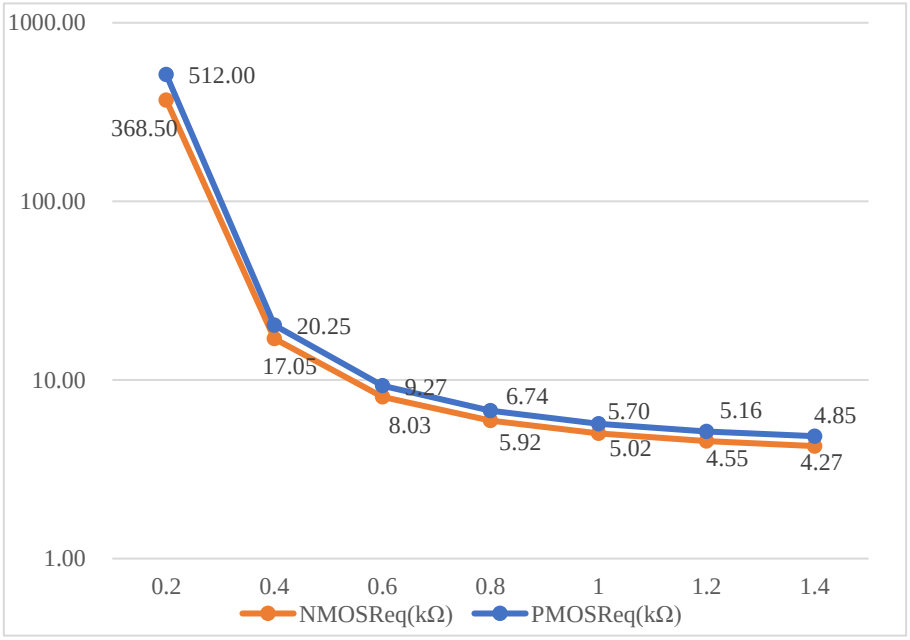


Figure 14 The R_{eq}-V_{DD} Curve for 7nm NMOS & PMOS

2) Gate capacitance versus gate voltage

I mainly utilize the *lx18* function in Hspice to get the gate voltage. Since gate voltage is a variable , the drain voltage is set to be zero. The diagram is from Topic01 P99 as Figure 15.

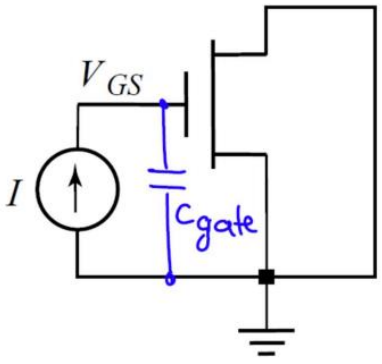


Figure 15 The Diagram for Measuring the Gate Capacitance

When using *lx18*, it is easy to get C_g with just sweeping V_{GS} from -2V to 2V.

45nm case: Shown as Figure16.

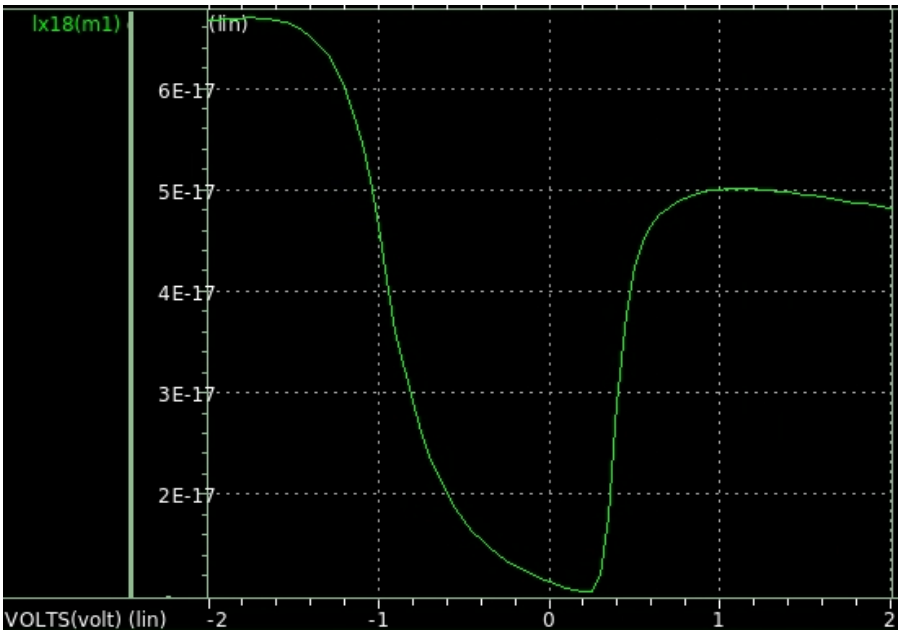
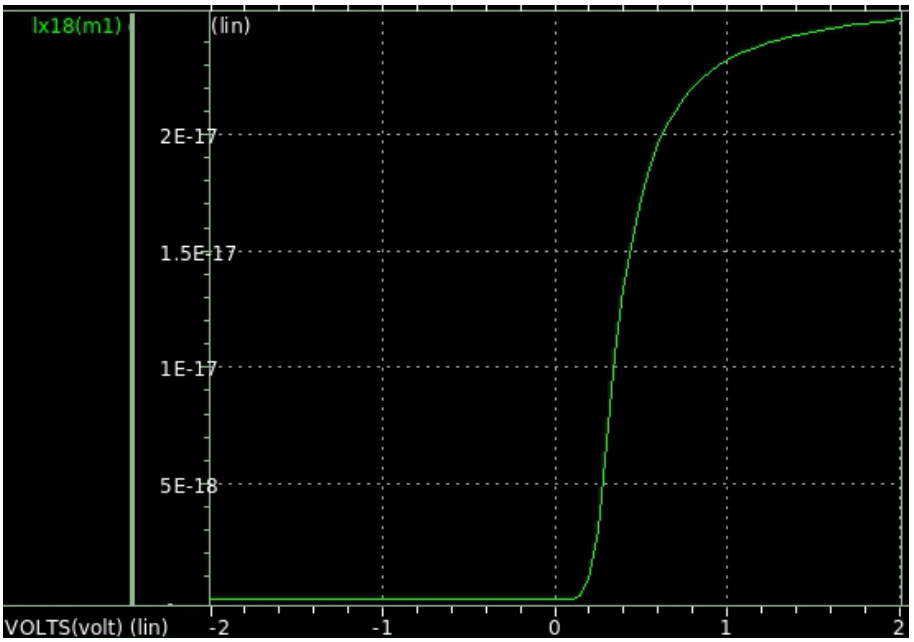


Figure 16 The C_G-V_{GS} Curve for 45nm NMOS

7nm case: Shown as Figure17.



Note: Another method is to use a small AC voltage source to connect the gate of NMOS, and the drain & source of the NMOS is still connected to GND. Then use AC analysis at the fixed frequent(e.g. $f = \frac{1}{2\pi}$) . When VGS varies from -2V to 2V, measure the I_{GS} at that frequent. The current equals to the gate capacitance value.

This method mainly depends on the formula of the definition of capacitance, but I don't work it out in hspice! ☹

Assignment #3 45nm Planer MOSFET vs. 7nm FinFET

Differences between two process nodes.

1) Of course, 7nm FinFET demands **lower V_{DD}** than 45nm MOSFET.
2) The channel length modulation λ of 7nm FinFET seems to be larger than 45nm MOSFET, which means **stronger channel modulation effect**, and the I_{DS}-V_{DS} curve tends to a straight line with a slope.
3) The **subthreshold slope** of 7nm FinFET is smaller than 45nm MOSFET.
4) The **threshold voltage** of 7nm FinFET is smaller than 45nm MOSFET.
5) The 45nm MOSFET suffers from body-effect, while the 7nm FinFET seems to be **not affected by the body-effect**, its threshold voltage is independent of body voltage bias.
6) The 7nm FinFET suffers from **stronger DIBL effect**, its threshold voltage drops faster when V_{DS} increases compared to the 45 nm MOSFET.
7) Commonly, like 45nm MOSFET, I_{ON} decreases with temperature and I_{OFF} increases with temperature. But in 7nm FinFET case, **I_{ON} & I_{OFF} both increases with temperature**.
8) The **resistance** of 7nm FinFET is much larger than 45nm MOSFET when **V_{DD} is low**.
9) The C-V curve of 45nm NMOS is about to be symmetric, while the C-V curve of 7nm FinFET is **flat** on the left half axis(negative V_{GS}).