RULES:

- **Closed-book, closed-notes. Calculators ok, but laptops and smartphones are not allowed.**
- **Cheat sheet of one A4 paper is allowed.**
- **Please answer the questions in English only. No Chinese answers will be accepted.**
- **Please show all intermediate steps: a correct solution without an explanation will get zero credit.**

1. Short Channel MOS (10 pts)

For the short-channel device shown in Fig. 1, given that $V_{dd} = 2.5V, V_{t0} = 0.4V, \gamma = 0.1\ V^{0.5}$, velocity saturation voltage $V'_{dsat} = 1V$, $2\emptyset_F = 0.6V$.

(a) Determine the different operation modes of the device while V_o is changed from 0 to V_{dd}.

(b) Derive the condition for V_o at the boundary of each operation mode. You do **NOT** need to calculate the actual value of V_o.

Hint: Threshold voltage $V_t = V_{t0} + \gamma\left(\sqrt{2\emptyset_F + V_{SB}} - \sqrt{2\emptyset_F}\right)$.

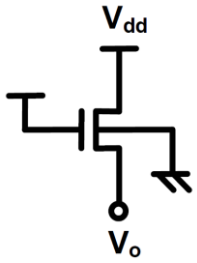


Fig. 1

Operation mode;

velocity saturation

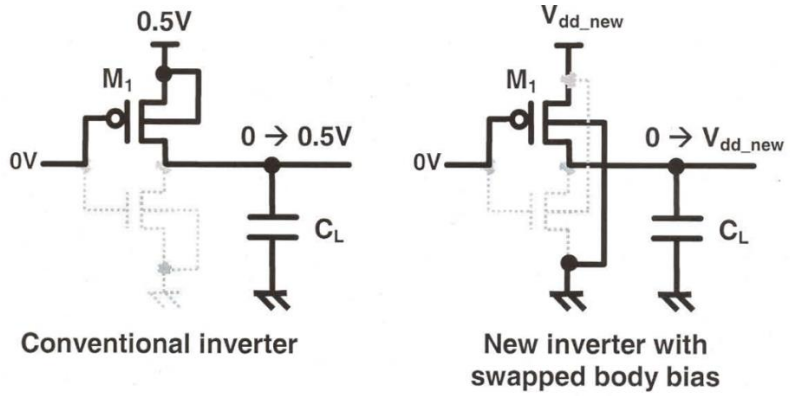
↓ B.C.; $V_{dsat} = V_{dd} - V_o - (V_{t\emptyset} + \gamma(\sqrt{2\emptyset_B + V_o} - \sqrt{2\emptyset_B}))$

saturation

↓ B.C.; $0 = V_{dd} - V_o - (V_{t\emptyset} + \gamma(\sqrt{2\emptyset_B + V_o} - \sqrt{2\emptyset_B}))$

cut-off

2. MOSFET Delay (12 pts)



Consider a new inverter in the upper right figure where the PMOS and NMOS body biases are swapped.

(a) Calculate V_{dd_new}, the supply voltage of the new inverter, which will make the delay of the new inverter equal to that of a conventional inverter operating at 0.5V.

(b) Give a qualitative explanation of the results (i.e. how the swapped body bias scheme affects the operating voltage).

Assume the following:

(i) The input to the inverter is a step function. In other words, the input switches instantly.

(ii) Propagation delay is defined as the 50% input change to 50% output change.

(iii) Approximate the average drive current, I_{av}, as the I_{ds} when $|V_{gs}|=|V_{ds}|$=supply voltage.

(iv) Sizing and total output capacitances are identical for both inverters.

(v) Ignore channel length modulation, leakage, slope dependency, short circuit current, etc.

V_{t0} = -0.2[V], V_{dsat} = -1[V], kp' = -30 x 10^{-6} [A/V^2], W/L = 1um/0.25um, λ=0 , $\gamma=\frac{\Delta V_t}{\Delta V_{sb}}=100[mV/V]$.

Hints:

1. V_t can be calculated by $V_t = V_{t0} + \Delta V_t = V_{t0} + \gamma \Delta V_{sb}$.
2. Saturation current of I_{ds} can be calculated as I_{dsat} = -1/2 kp'W/L$(V_{gs}-V_t)^2$.

Your answer to Problem 1:

$$\text{Delay} = \frac{C_L V_{dd}}{I_{av}}$$

$$\text{Delay of conventional inv} = \frac{C_L \cdot 0.5}{-k_p' \frac{W}{L} (-0.5-(-0.2))^2}$$

$$= \frac{C_L}{-k_p' \cdot \frac{W}{L}} \times \frac{0.5}{0.3^2} \quad \text{——} \ ①$$

$$\text{Delay of new inv} = \frac{C_L V_{dd}}{-k_p' \frac{W}{L} (-V_{dd} - (-0.2 + 0.1 V_{dd}))}$$

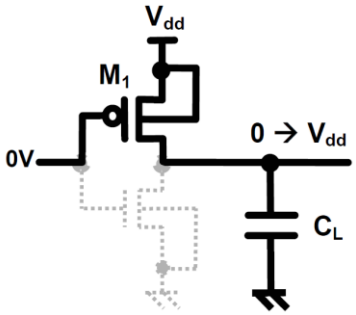
$$= \frac{C_L}{-k_p' \frac{W}{L}} \times \frac{V_{dd}}{(1.1 V_{dd} - 0.2)^2} \quad \text{——} \ ②$$

$① = ②$; $\frac{0.5}{0.3^2} = \frac{V_{dd}}{(1.1 V_{dd} - 0.2)^2} \Rightarrow V_{dd} \approx 0.437 \text{ V}$.

Forward body bias allows the supply to be lowered for the same operating frequency.

3. Energy Dissipation [16 pts]

(a) [5 pts] In Fig. 2, calculate the energy dissipated as heat in M_1 during the low to high transition in the output. Ignore the parasitic capacitances.



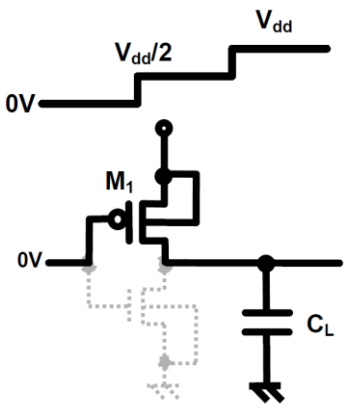
$$C_L V_{dd}^2 - \frac{1}{2} C_L V_{dd}^2 = \boxed{\frac{1}{2} C_L V_{dd}^2}$$

Fig. 2

(b) [3 pts] What happens to the energy dissipation in (a) if the transistor length of M_1 is doubled?

Does not change

(c) [8 pts] In Fig. 3, calculate the energy dissipated as heat in M_1 if the supply voltage is increased from 0V to V_{dd} with as step of $V_{dd}/2$. The output is initially at 0V. Ignore the parasitic capacitances and assume $|V_{tp}| < V_{dd}/2$.



Energy drawn from supply

$$= \frac{V_{dd}}{2} \cdot \frac{V_{dd}}{2} \cdot C_L + V_{dd} \cdot \frac{V_{dd}}{2} \cdot C_L$$

$$= \frac{3}{4} C_L V_{dd}^2$$

Energy stored in capacitor

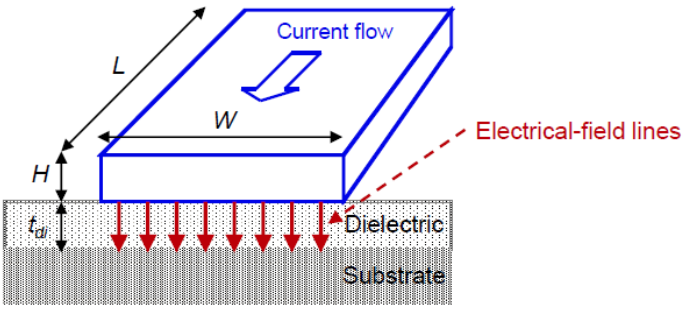
$$= \frac{1}{2} C_L V_{dd}^2$$

Fig. 3

$$\therefore \quad \frac{3}{4} C_L V_{dd}^2 - \frac{1}{2} C_L V_{dd}^2 = \boxed{\frac{1}{4} C_L V_{dd}^2}$$

4. Wire Delay [12 pts]

Consider an isolated 2mm long and 1μm wide metal 1 wire over a silicon substrate driven by an inverter that has zero resistance and zero parasitic output capacitance. How will the delay change for the following cases? Briefly explain your reasoning in each case. *Only consider the parallel-plate capacitance.*



Delay ∝ RC

Fig. 4

(a) [3 pts] If the wire width is doubled.

R is halved, C is doubled
∴ Delay remains constant

(b) [3 pts] If the wire length is halved.

R is halved, C is halved
∴ Delay becomes $\frac{1}{4}$

(c) [3 pts] If the wire thickness is doubled.

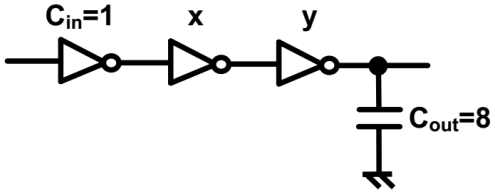
R is halved, C is constant
∴ Delay becomes $\frac{1}{2}$

(d) [3 pts] If the thickness of the dielectric between the wire and the substrate is doubled.

R is constant, C is halved
∴ Delay becomes $\frac{1}{2}$

5. Inverter Chain [16 pts]

Assume $\gamma = 1$ ($C_{int} = C_{gate}$). For a static inverter, $W_P : W_N = 2:1$ gives equivalent pull-up and pull-down resistances. The delay of a reference inverter is t_{p0}.



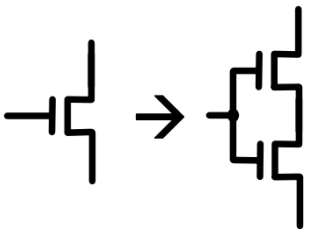
(a) [4pts] What is the minimum delay of this inverter chain, in terms of t_{p0}?

g =	1	1	1
f =	x	$\frac{y}{x}$	$\frac{8}{y}$
p =	1	1	1

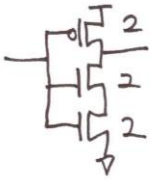
$\Rightarrow h^* = \sqrt[3]{8} = 2$

$\therefore D_{min} = 1 \times 3 + 3 \times 2 = 9$

(b) [6 pts] Now suppose that you are to use a two stack for all NMOS devices (not for PMOS's) in the inverter chain design (for example, stacks can be used to reduce the leakage power). What is the minimum delay of the new inverter chain?



new inverter



$p = \frac{4}{3}$

$g = 2$

g =	2	2	2
f =	x	$\frac{y}{x}$	$\frac{8}{y}$
p =	$\frac{4}{3}$	$\frac{4}{3}$	$\frac{4}{3}$

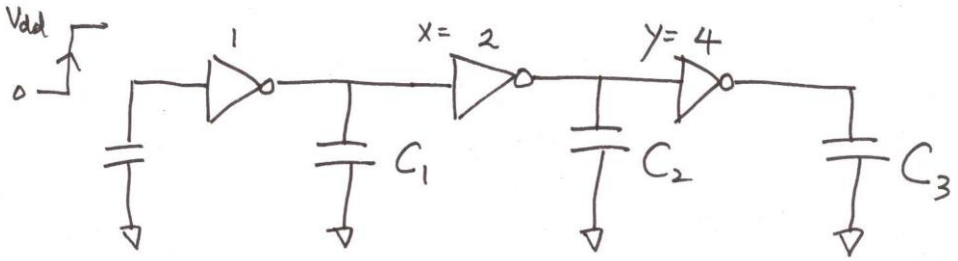
$h^* = \sqrt[3]{8 \times 8} = 4$

$\therefore D_{min} = \frac{4}{3} \times 3 + 3 \times 4$

$= 16$

(c) [6 pts] For the new inverter chain, when the primary input switches from 0V to V_{dd}, what is
   i. the total energy drawn from V_{dd}, and
   ii. the total energy dissipated by heat?

Ignore the intermediate node capacitances in the stacks and do NOT include the switching energy of the primary input.



$$C_{node} = C_{parasitic} + C_{gate}$$

$$C_1 = \frac{2}{3} + 2 = \frac{8}{3}$$

$$C_2 = \frac{4}{3} + 4 = \frac{16}{3}$$

$$C_3 = \frac{8}{3} + 8 = \frac{32}{3}$$

(i) $E_{drawn} = C_2 \times CV_{dd}^2 = \frac{16}{3} CV_{dd}^2$

(ii) $E_{diss} = \frac{1}{2}(C_1 + C_2 + C_3) \times CV_{dd}^2$

$$= \frac{1}{2}\left(\frac{8}{3} + \frac{16}{3} + \frac{32}{3}\right) \times CV_{dd}^2$$

$$= \frac{28}{3} CV_{dd}^2$$

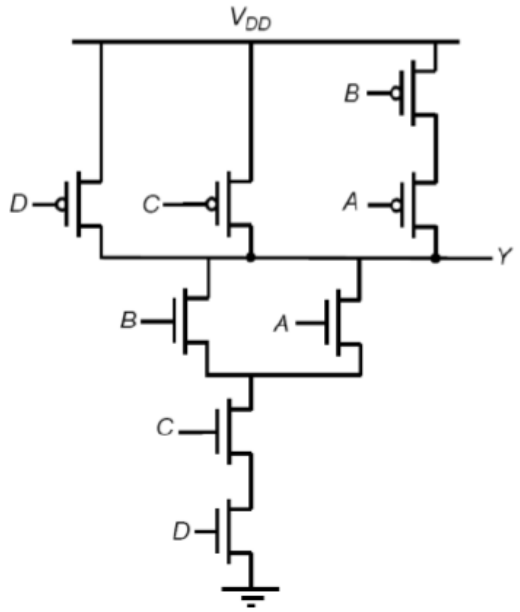
6. Combinational Logic [14 pts]

For the function $Y = \overline{(A+B)CD}$,

(a) [5 pts] Implement it using complementary CMOS.

(b) [5 pts] Size the devices in 1) so that that output resistance is the same as that of an inverter with an NMOS $W_N = W$ and PMOS $W_P = 2W$. Assume that for a static inverter, $W_P : W_N = 2:1$ gives equivalent pull-up and pull-down resistance.

(c) [4 pts] Calculate the logical effort of the gate you implemented in 1).



(b) NMOS: $W_A = W_B = W_C = W_D = 3W$
PMOS: $W_A = W_B = 4W, W_C = W_D = 2W$

(c) $LE_A = LE_B = \frac{7}{3}, LE_C = LE_D = \frac{5}{3}$

Or

(b) NMOS: $W_A = W_B = 2W,\ W_C = W_D = 4W$
PMOS: $W_A = W_B = 4W, W_C = W_D = 2W$

(c) $LE_A = LE_B = LE_C = LE_D = 2$

7. Complementary CMOS [20 pts]

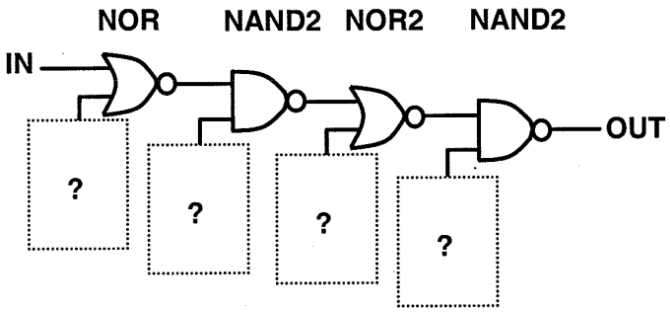
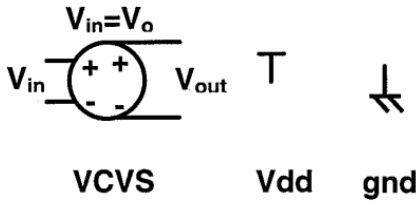


Fig. 6

(a) [10 pts] Your supervisor has asked you to simulate the worst and best case IN-to-OUT delay of a chain of NAND2 and NOR2 gates (see Fig. 6) in HSPICE when IN switches from V_{dd} to 0. Complete the above schematic by filling the empty boxes with appropriate instances for the worst and best case delay simulation.

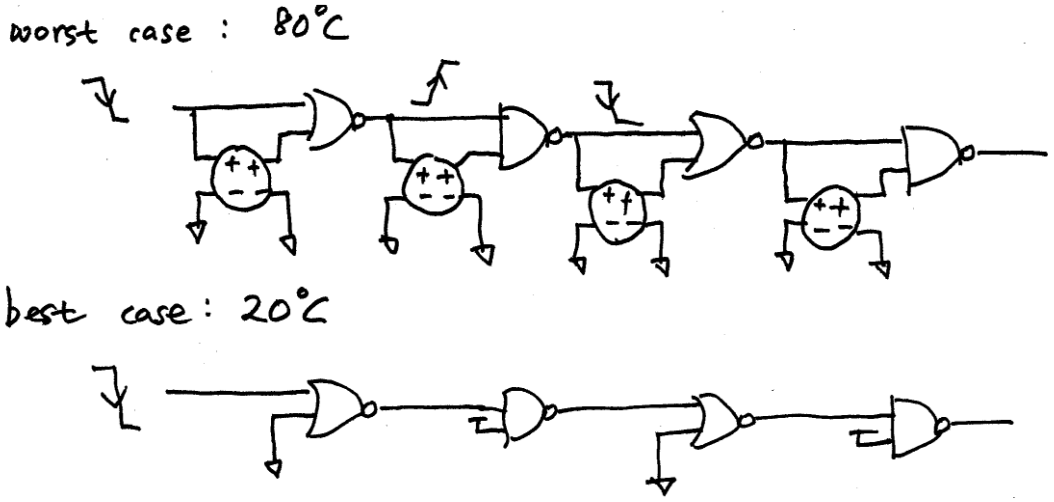
You are only allowed to use the following 3 instances. (VCVS: voltage controlled voltage source)



Given that the die temperature for this circuit's application can range from 20˚C to 80 ˚C, what temperature should you choose for each delay simulation?

Explain your answer.

Hint: We do not consider the situations when the input signal of a gate is blocked by another input (for instance, a '0' input can block the other input in a NAND2 gate).



(b) [10 pts] Repeat (a) for the case when IN switches from 0 to V_{dd}.