Design of a Single-Bit Half Adder and a Full Adder

Guideline:

1) Please prepare your **submission in English**. No Chinese submissions will be accepted.
2) Please put all your **simulation results** (including figures and values of coefficients) as well as some **descriptions** in a report (.PDF) and submit it to Blackboard. Also, please pack **all the source files** of each assignment to a zip with name 'EE213 Lab3 + your ID + your Name', and submit the source file package to this link: (http://pan.shanghaitech.edu.cn/cloudservice/outerLink/decode?c3Vnb24xNjY3NjM1Mzc4ODM1c3Vnb24=)
3) Please submit on time. Late submission less than 24h will only get 60% scores. Late submission more than 24h will NOT be accepted.
4) Please **work on your own**. Discussion is permissible, but identical submissions are unacceptable! Here is the Academic Integrity policy of SIST. (https://sist.shanghaitech.edu.cn/2019/1107/c2842a46321/page.htm)

Design Goal:

The goal of this lab is to design **a single-bit half adder and full adder** of **45nm process** using Cadence Virtuoso and simulate them in HSPICE simulators. For each adder, you need to go through two phases:

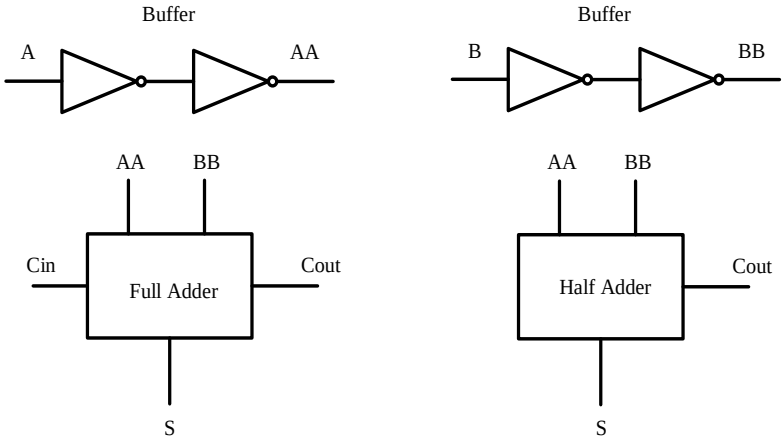
1) **Schematic and Pre-simulation**: Do a literature survey on the half/full adder and design a schematic of one structure. You can test the functionality of your structure by SPICE.
2) **Layout and Post-simulation**: Draw the layout of your adder structure and extract the netlist to simulate in HSPICE simulators.

Design requirements:

1) Use **complementary static CMOS logic** in your design. No pass transistor or dynamic circuit.
2) Include the **parasitic capacitances** when extracting the layout.
3) Follow the naming conventions and input/output conditions given below.

	Half-adder	Full adder	Description
Input pin	A, B	A, B, Cin	Add buffers to input port A and B
Output pin	Cout, S	Cout, S	Add a load of 0.1pF at ouput port
Supply voltage	VDD! GND!		VDD!=0.7V

4) Your half adder and full adder should be like the following figure. You can use your inverter designed in Lab 1 as a buffer.



Simulation guidance:

1) Download the following files from Blackboard:
   "halfadder_delay.sp", "fulladder_delay.sp", "halfadder_power.sp", "fulladder_power.sp".
   You should include your netlist (named as halfadder.sp or fulladder.sp), the model files (PMOS_VTL.inc and NMOS_VTL.inc), the input signals and load capacitance in each of these files in your pre/post simulation.

2) Delay measurement: Run "halfadder_delay.sp" and "fulladder_delay.sp" to test the functionality of your adders using the following input patterns. Also, measure the worst case delay by providing the adders with proper input patterns.
   ****
   Input pattern for half adder test cases:
   A: 0 0 1 1 Vin1 A gnd PULSE (0v 0.7v 9.9n 0.1n 0.1n 9.9n 20n)
   B: 0 1 0 1 Vin2 B gnd PULSE (0v 0.7v 4.9n 0.1n 0.1n 4.9n 10n)
   Input pattern for full adder test cases:
   A: 0 0 0 0 1 1 1 1 Vin1 A gnd PULSE (0v 0.7v 19.9n 0.1n 0.1n 19.9n 40n)
   B: 0 0 1 1 0 0 1 1 Vin2 B gnd PULSE (0v 0.7v 9.9n 0.1n 0.1n 9.9n 20n)
   Cin: 0 1 0 1 0 1 0 1 Vin3 Cin gnd PULSE (0v 0.7v 4.9n 0.1n 0.1n 4.9n 10n)
   ****

3) After you find your maximum delay, replace "10NS" in command line ".PARAM DELAY_MAX =10NS" in "halfadder_power.sp" and "fulladder_power.sp" with **your measured maximum delay** and run simulation to measure power dissipation at maximum operating frequency.
   Note: the input pattern for simulating power should not be changed.
   ****
   Input patterns half adder:
   A: 0 1 0 1 Vin1 A gnd PULSE (0v 0.7v 4.9n 0.1n 0.1n 4.9n 10n)
   B: 0 0 1 1 Vin2 B gnd PULSE (0v 0.7v 9.9n 0.1n 0.1n 9.9n 20n)
   Input patterns full adder:
   A: 0 1 0 1 0 1 0 1 Vin1 A gnd PULSE (0v 0.7v 4.9n 0.1n 0.1n 4.9n 10n)
   B: 0 0 1 1 0 0 1 1 Vin2 B gnd PULSE (0v 0.7v 9.9n 0.1n 0.1n 9.9n 20n)
   Cin: 0 0 0 0 1 1 1 1 Vin3 Cin gnd PULSE (0v 0.7v 19.9n 0.1n 0.1n 19.9n 40n)

Submissions:

A report that contains:

1) **Schematic and Pre-simulation:**
   - Explain your design of half adder and full adder briefly.
   - Schematic of your half adder and full adder.
   - Give some bullet points explaining how you optimized your design.
   - Show the input and output waveforms of the input test cases.
   - Show the worst case delay and its corresponding input/output waveforms for VDD! = 0.7V
   - Give the power consumption at the maximum operating frequency for VDD! = 0.7V.
2) **Layout and Post-simulation:**
   - Layout (with the area information) of your half adder and full adder.
   - LVS, DRC and PEX screenshots showing no violations.
   - Show the input and output waveforms of input test cases.
   - Show the worst case delay and its corresponding input/output waveforms for VDD! = 0.7V.
   - Give the power consumption at the maximum operating frequency for VDD! = 0.7V.

Attachments:

1. Pack the lab files of test cases, worst case delay and power consumption measurements in pre-simulation with title “test_case”, “worst_delay”, and “power”. Put these three files into a folder named as “half_adder_pre” or “full_adder_pre”.
2. Similarly, pack the lab files of test cases, worst case delay and power consumption measurements in post-simulation with title “test_case”, “worst_delay”, and “power”. Put these three files into a folder named as “half_adder_post” or “full_adder_post”.
3. Pack these four files into a compressed file and name it with the title: ‘EE213 Lab3 + your ID + your Name’, and submit the source file package to this link: (http://pan.shanghaitech.edu.cn/cloudservice/outerLink/decode?c3Vnb24xNjY3NjM1Mzc4ODM1c3Vnb24=)