EE216 Re-configurable Computing Homework2 Report

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1 Screenshots

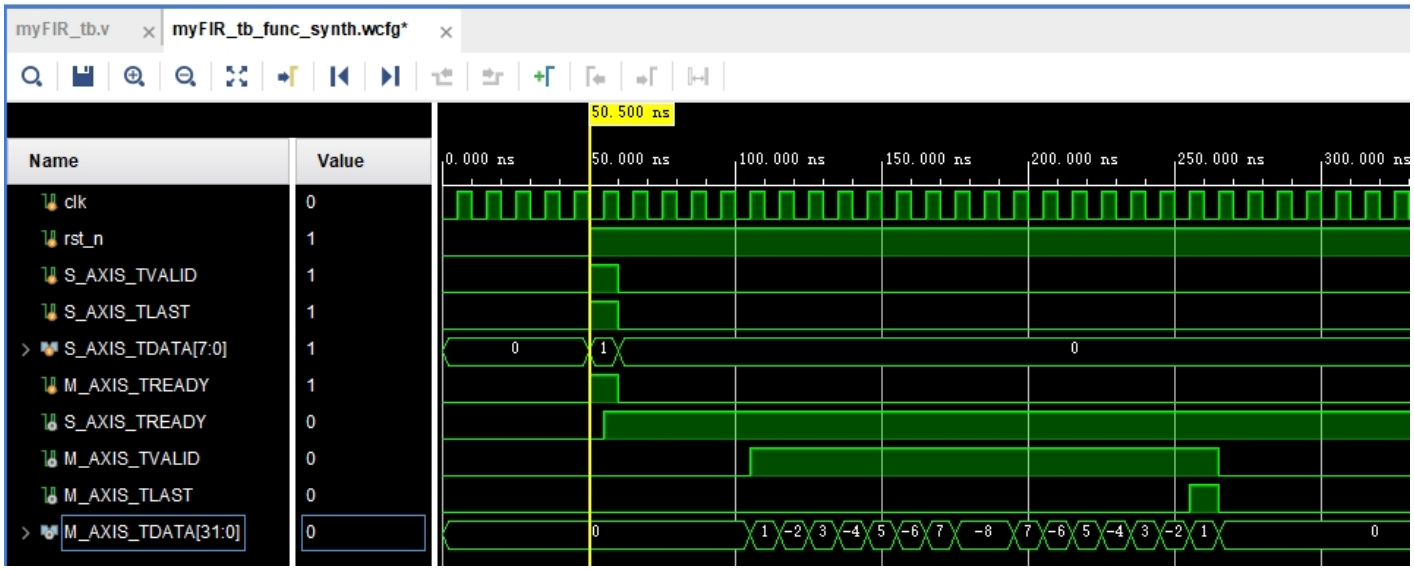

Figure 1: Simulation Result

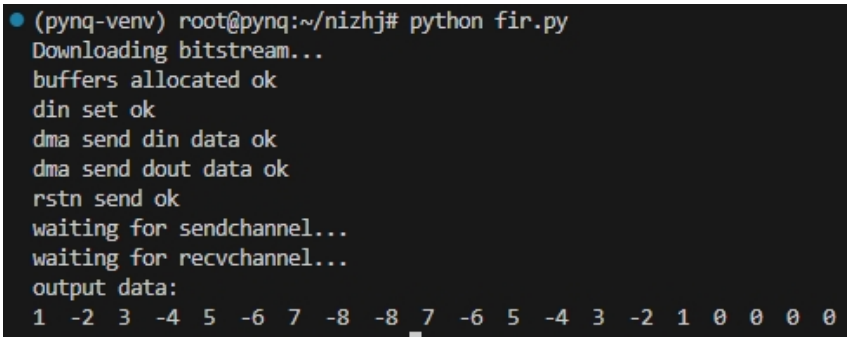

Figure 2: Board Test Result

2 Questions

Answer1: The 1^{st} cycle is used to load data from the shifting register and complete the multiplication and addition. For example, h0*(data[0] + data[15]). After that we should get 8 addition results. Then three cycles are used to complement the adder in pipe-line. The 2^{nd} cycle accumulates eight numbers into four. The 3^{rd} cycle accumulates four numbers into two. The 4^{th} cycle adds two numbers into one. The 5^{th} cycle send the adder output to the M_AXIS_TDATA.

Answer2: The minimum data width should consider data overflow in each stages. The data input is 8 bits. Firstly in the MAC operation, two 8-bit numbers may generate a 9-bit number. Then a 9-bit number multiply a 5-bit signed number and get a 14-bit number. In the first stage of pipe-lined adder, two 14-bit numbers are added into a 15-bit number. In the second stage of pipe-lined adder, two 15-bit numbers are added into a 16-bit number. In the last stage of pipe-lined adder, two 16-bit numbers are added into a 17-bit number. So the minimum data width of the output is 17.