EE216 Re-configurable Computing Homework4 Report

Zhaojun Ni, 2022231102

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1 Optimizing Method

The entire algorithm can be divided into two stages. The first is the shift register, and the second is the multiplication and accumulation module. I first separated them and represented them with **SHIFT** and **MAC**, respectively. Due to the fact that the loop where the **MAC** part is located needs to be executed 16 times, I used unroll factor=16 to make these loops execute in parallel. At the same time, the entire loop was executed using a pipeline with an interval set to 1, which optimized the number of latency cycles and interval cycles to 1. The FF and LUT resources used were 577 and 666, respectively, reducing 35.8% and 15.4% compared to the optimization examples in the tutorial.

2 C-Simulation Result

```
INFO: [SIM 211-2] *************** CSIM start ***************
INFO: [SIM 211-4] CSIM will launch GCC as the compiler.
   Compiling ../../../../FIR.cpp in debug mode
   Generating csim.exe
{1 -2 3 -4 5 -6 7 -8 -8 7 -6 5 -4 3 -2 1 }
Test passed.
INFO: [SIM 211-1] CSim done with 0 errors.
INFO: [SIM 211-3] *************** CSIM finish ***************
INFO: [HLS 200-111] Finished Command csim_design CPU user time: 0 seconds.
Finished C simulation.
```

Figure 1: C-Simulation Result with 0 errors.

3 Synthesis Reports

Synthesis Summary Report of 'fir'

General Information

Date:	Fri Nov 17 20:36:22 2023	Solution:	solution1 (Vivado IP Flow Target)
Version:	2020.2 (Build 3064766 on Wed Nov 18 09:12:45 MST 2020)	Product family:	zynquplus
Project:	FIR	Target device:	xczu7ev-ffvc1156-2-e

Timing Estimate

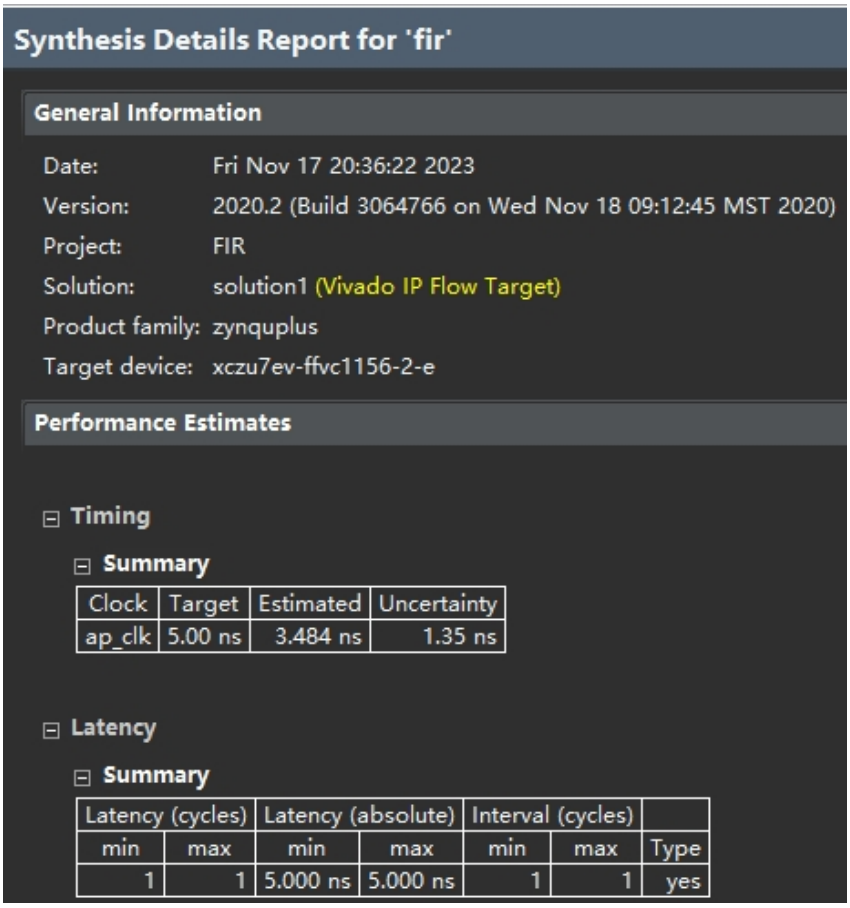
Target	Estimated	Uncertainty
5.00 ns	3.484 ns	1.35 ns

Performance & Resource Estimates

Modules Loops

Modules && Loops	Issue Type	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interval	Trip Count	Pipelined	BRAM	DSP	FF	LUT	URAM
fir		-	1	5.000	-	1	-	yes	0	0	577	666	0

Figure 2: Synthesis Summary Report: 577 FFs and 666 LUTs.



Synthesis Details Report for 'fir'

General Information

Date: Fri Nov 17 20:36:22 2023
Version: 2020.2 (Build 3064766 on Wed Nov 18 09:12:45 MST 2020)
Project: FIR
Solution: solution1 (Vivado IP Flow Target)
Product family: zynquplus
Target device: xczu7ev-ffvc1156-2-e

Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	5.00 ns	3.484 ns	1.35 ns

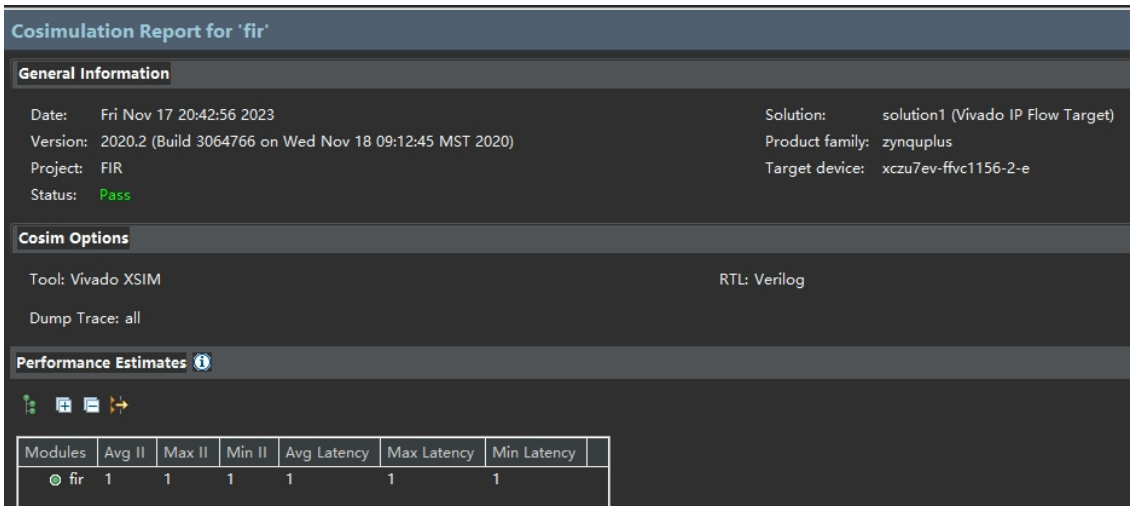
Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
1	1	5.000 ns	5.000 ns	1	1	yes

Figure 3: Synthesis Details Report: 1 Latency cycle and 1 Interval cycle.

4 Co-Simulation Result



Cosimulation Report for 'fir'

General Information

Date: Fri Nov 17 20:42:56 2023
Version: 2020.2 (Build 3064766 on Wed Nov 18 09:12:45 MST 2020)
Project: FIR
Status: Pass
Solution: solution1 (Vivado IP Flow Target)
Product family: zynquplus
Target device: xczu7ev-ffvc1156-2-e

Cosim Options

Tool: Vivado XSIM
RTL: Verilog
Dump Trace: all

Performance Estimates

Modules	Avg II	Max II	Min II	Avg Latency	Max Latency	Min Latency
fir	1	1	1	1	1	1

Figure 4: Co-Simulation Report: PASS.

5 Waveform Screenshot

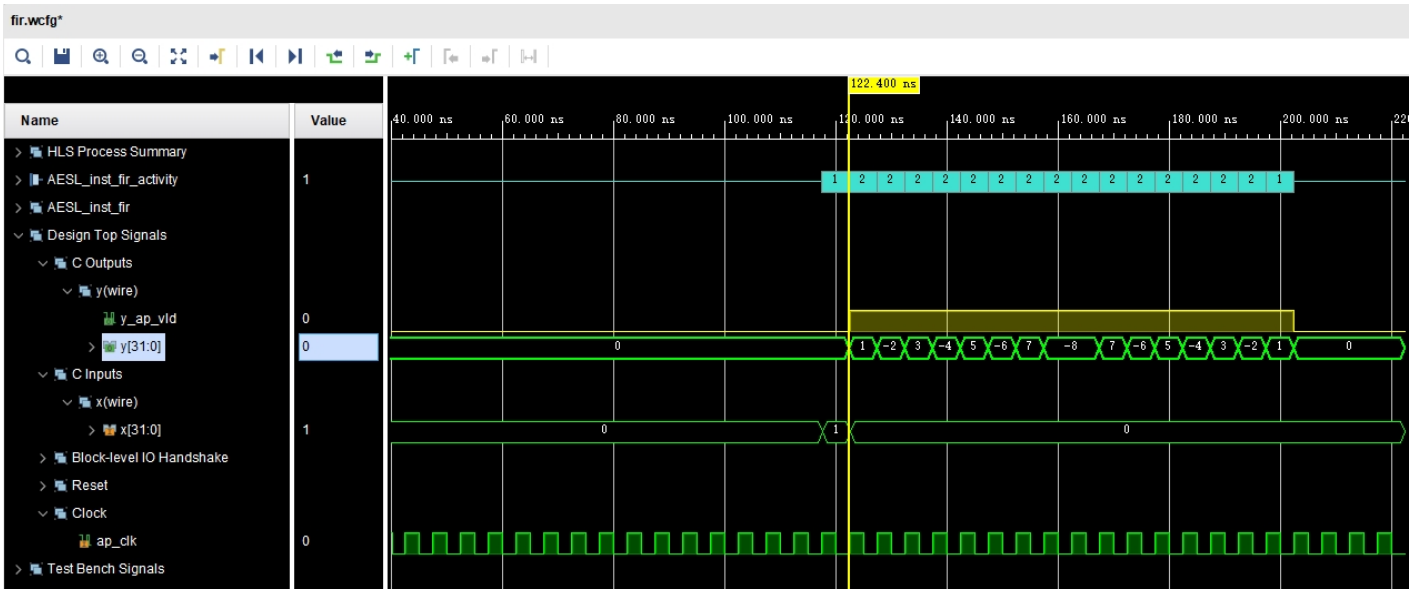


Figure 5: The output is generated 1 cycle behind the input signal.