

## Pre Lab

Pre Lab:

- 1.) - use equation for phase error to find instantaneous frequency error  
 $\dot{\theta}_c(t)$ :

- call instantaneous frequency error:  $w_e(t) = \frac{d\theta_c(t)}{dt}$

- given phase error equation:  $\dot{\theta}_c(t) = \frac{w_0 - w_c}{AK} (1 - e^{-AKt}) + \phi_0 e^{-AKt}$

$$\begin{aligned} \dot{w}_e(t) &= \frac{d}{dt} \left[ \frac{w_0 - w_c}{AK} \right] - \frac{d}{dt} \left[ \left( \frac{w_0 - w_c}{AK} \right) e^{-AKt} \right] + \frac{d}{dt} \phi_0 e^{-AKt} \\ &= \left( \frac{w_0 - w_c}{AK} \right) \cdot (-AK) \cdot e^{-AKt} + \phi_0 (-AK) e^{-AKt} \\ &= (w_0 - w_c) e^{-AKt} - AK \phi_0 e^{-AKt} \end{aligned}$$

$$w_e(t) = [(w_0 - w_c) - AK \phi_0] e^{-AKt}$$

- 2.) - Show effect of  $\phi_0$  is negligible:

- given:  $w_0 = 10 \text{ K rad/s}$  from  $C_r = \sin(10000t)$   
 $\phi_0 = 0$  (since  $A \sin(w_0 t + \phi_0)$ )

- $w_e(t) = [(w_0 - w_c) - AK \cdot (0)] e^{-AKt}$

$$w_e(t) = (w_0 - w_c) e^{-AKt}$$

- 3.) - solve for time to achieve specified frequency errors:

- given  $w_0 = 10 \text{ K rad/s}$   
 $w_c = 5 \text{ K rad/s}$

$$K = A = 1$$

- $w_e(t) = (10K - 5K) \cdot e^{-(10K)t}$

$$w_e(t) = 5K e^{-t}$$

solve for  $t$

$$\rightarrow e^{-t} = \frac{w_e(t)}{5K} \Rightarrow t = \ln\left(\frac{5000}{w_e(t)}\right)$$

- for 10 rad/s:  $t = \ln\left(\frac{5000}{10}\right)$ ,  $t \approx 6.215 \text{ s}$

- for 1 rad/s:  $t = \ln\left(\frac{5000}{1}\right)$ ,  $t \approx 8.517 \text{ s}$

- for 0.1 rad/s:  $t = \ln\left(\frac{5000}{0.1}\right)$ ,  $t \approx 10.820 \text{ s}$

## Lab

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The focus of this lab is to show the relationship between the carrier frequency and the minimum loop bandwidth required to achieve a lock. At a 250 Hz carrier frequency, the PLL successfully locked with a loop bandwidth of 0.08 (Figure 3), while a lower bandwidth failed to synchronize (Figure 4). When the carrier frequency was increased to 500 Hz, the 0.08 bandwidth was no longer sufficient, as shown by the out-of-sync signals in Figure 5. A wider bandwidth of 0.150 was required to establish a stable lock (Figure 6). The trend continued with the 1000 Hz carrier, which was unlocked at a 0.100 bandwidth (Figure 8) and required a wider bandwidth of about 0.291 to finally acquire the signal (Figure 9).

This also highlights the trade-off of the PLL's loop bandwidth. While a wider bandwidth is necessary to acquire higher frequency signals, it is also more susceptible to noise. This is evident by comparing the relatively clean output in Figure 6 (0.150 BW) with the much jitterier output in Figure 9 (0.291 BW), which allowed more noise to pass through. Overall, increasing the noise amplitude directly degrades the PLL's performance. As shown in Figure 7, when the noise was amplified, the PLL's output became visibly less stable as it struggled to maintain its lock on the noisy input signal.

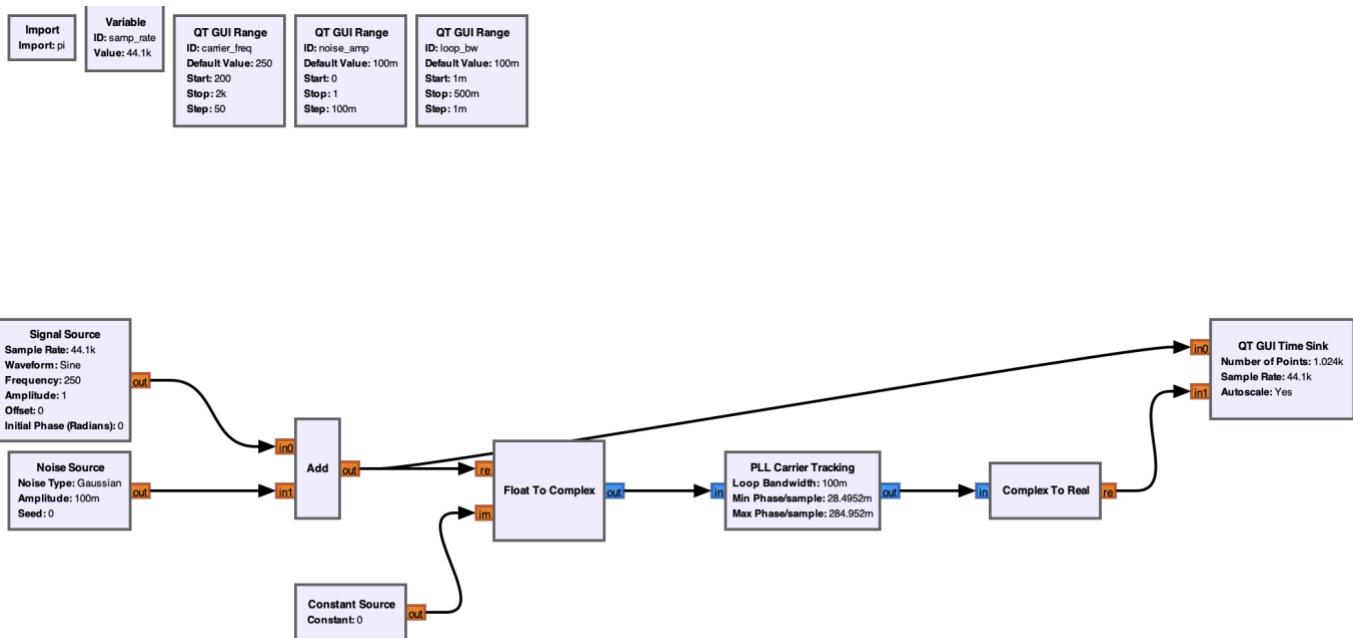


Figure 1: Block Diagram for PLL

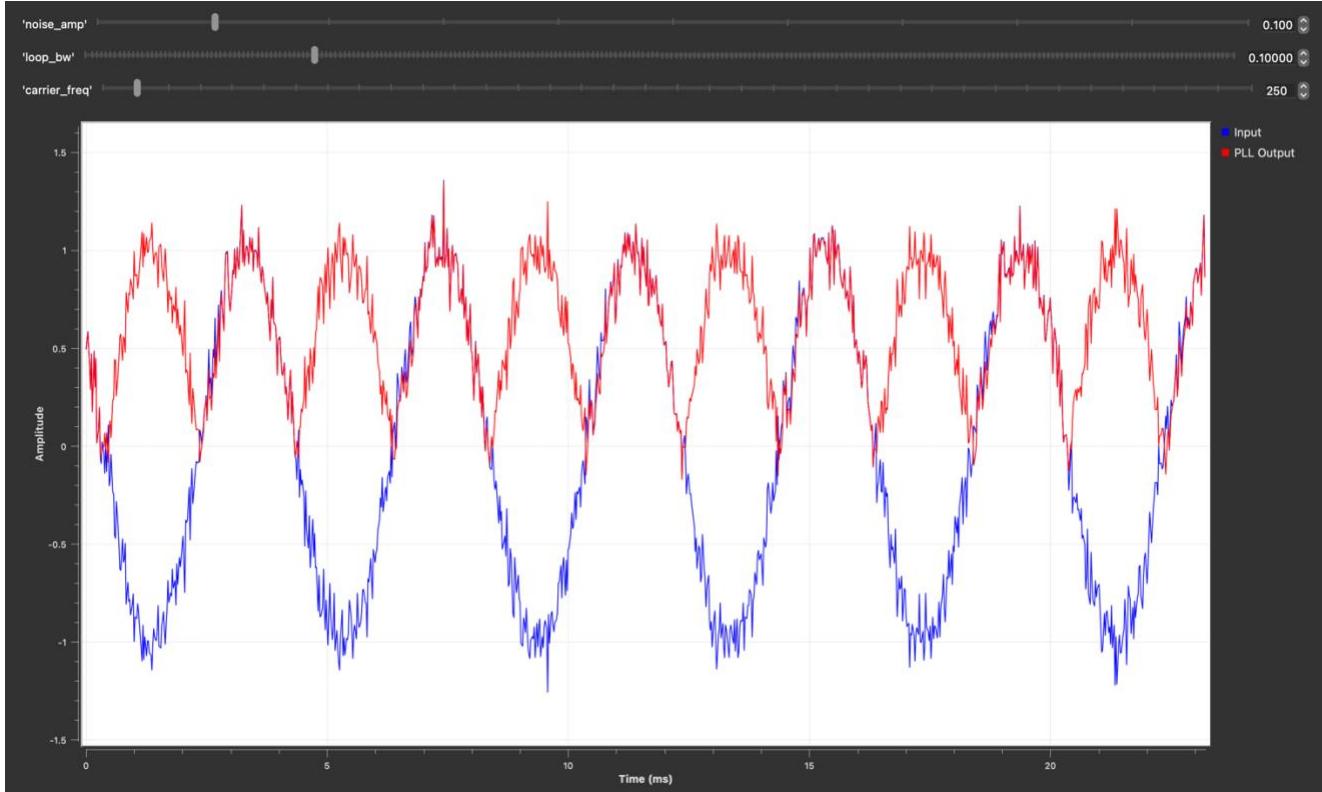


Figure 2: Carrier Frequency at 250Hz

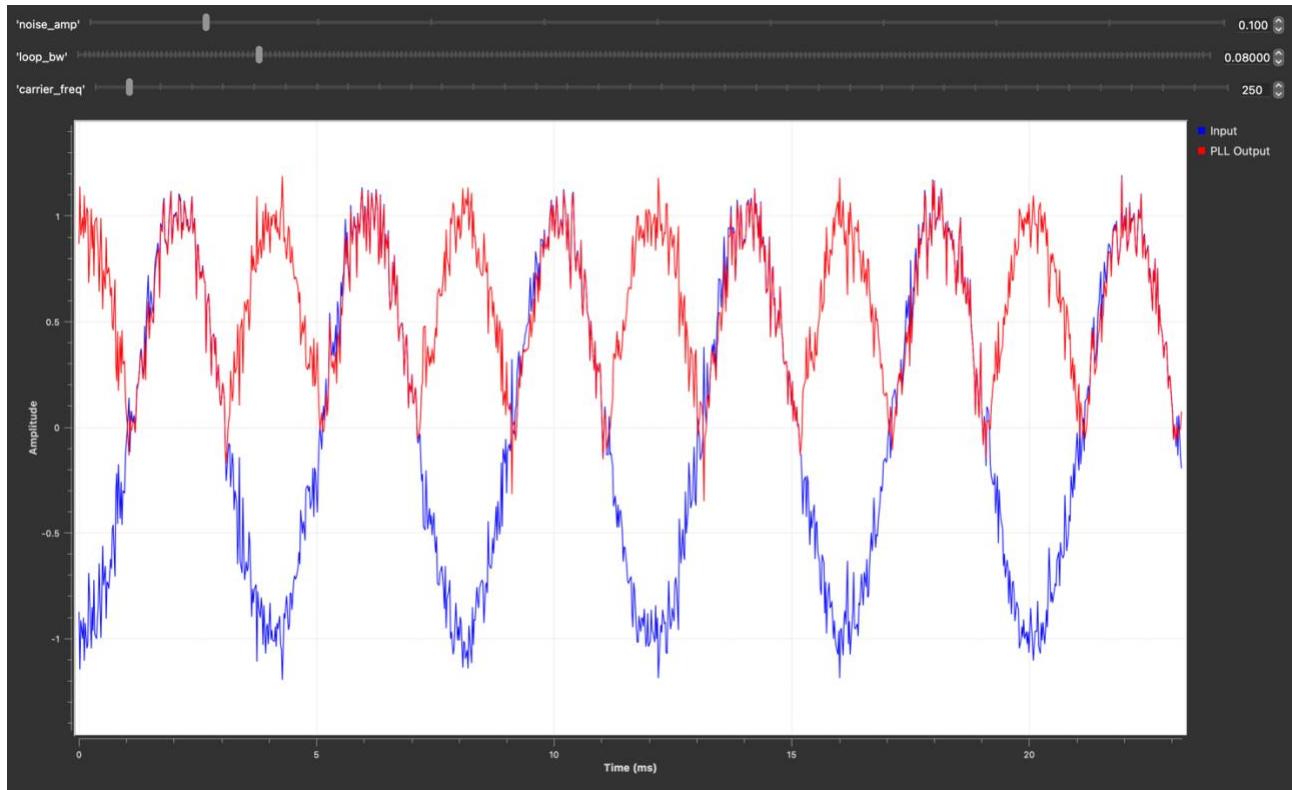


Figure 3: PLL locked on at loop bandwidth of 0.08 at 250Hz frequency

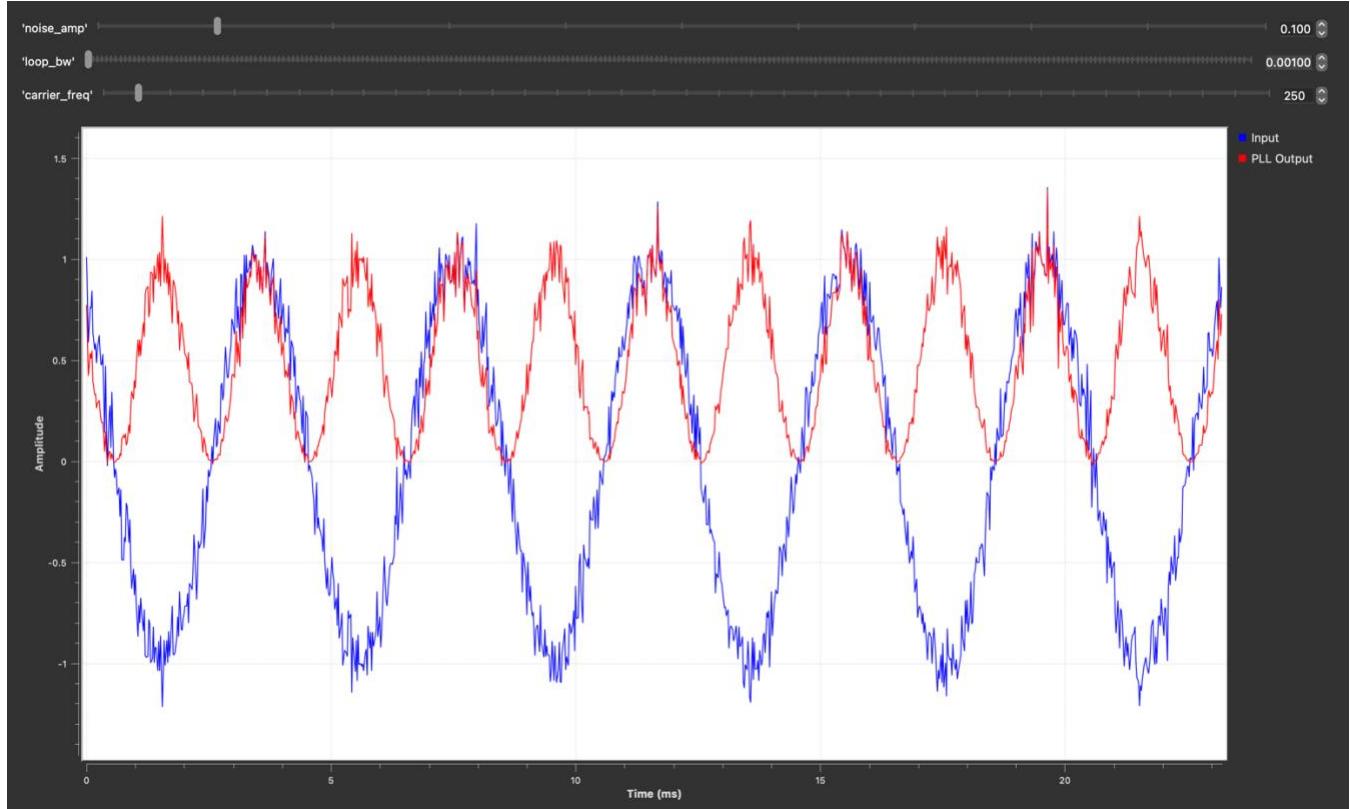


Figure 3: PLL unlocked so the input is out of sync with the output

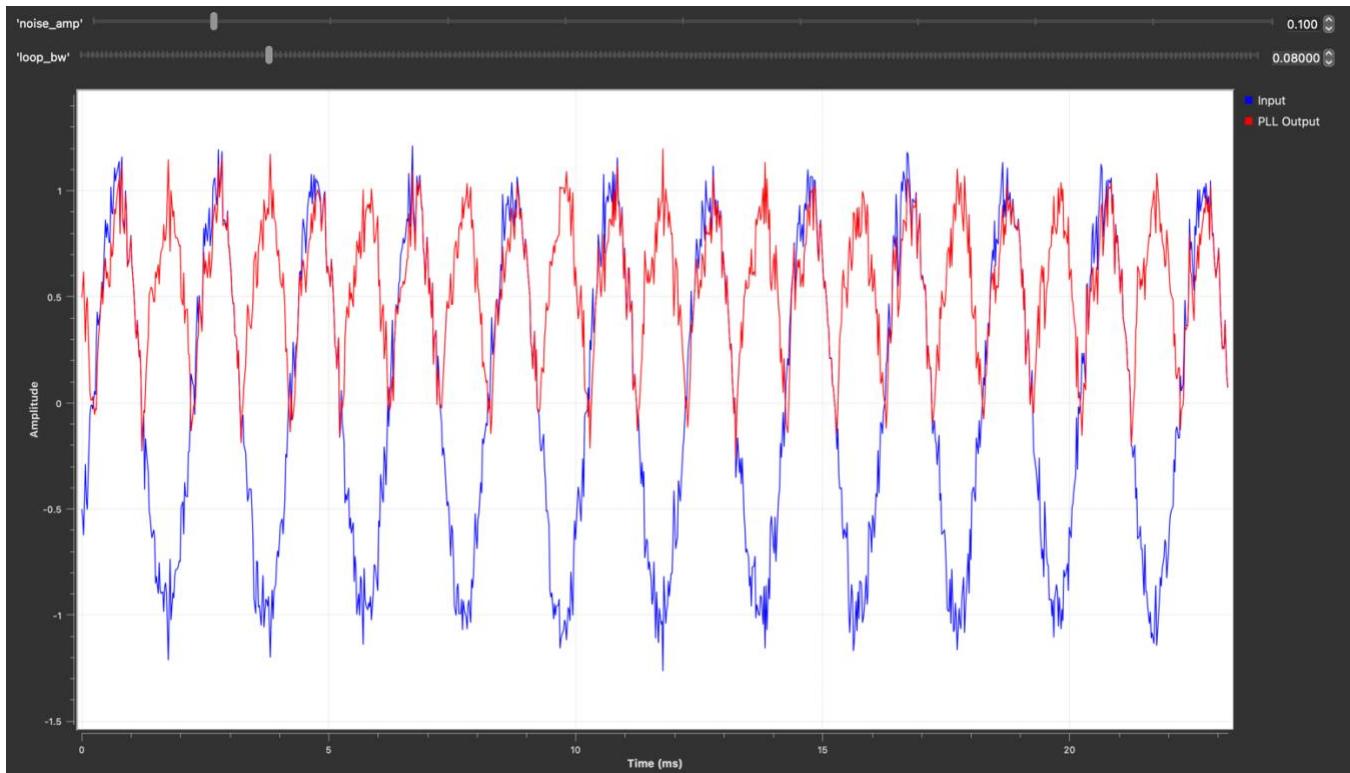


Figure 4: PLL out of sync with loop bandwidth at 0.08 when frequency is 500Hz

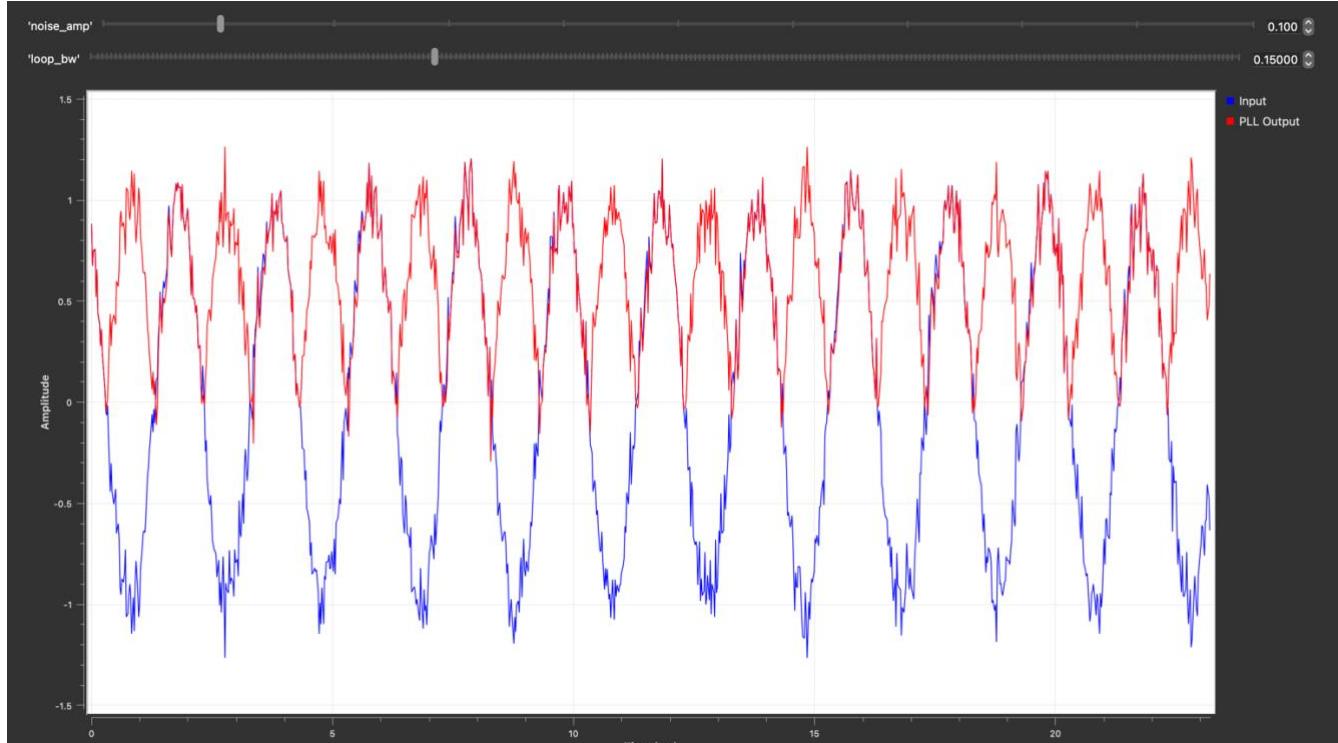


Figure 5: PLL locked at loop bandwidth of 0.150 for 500Hz frequency

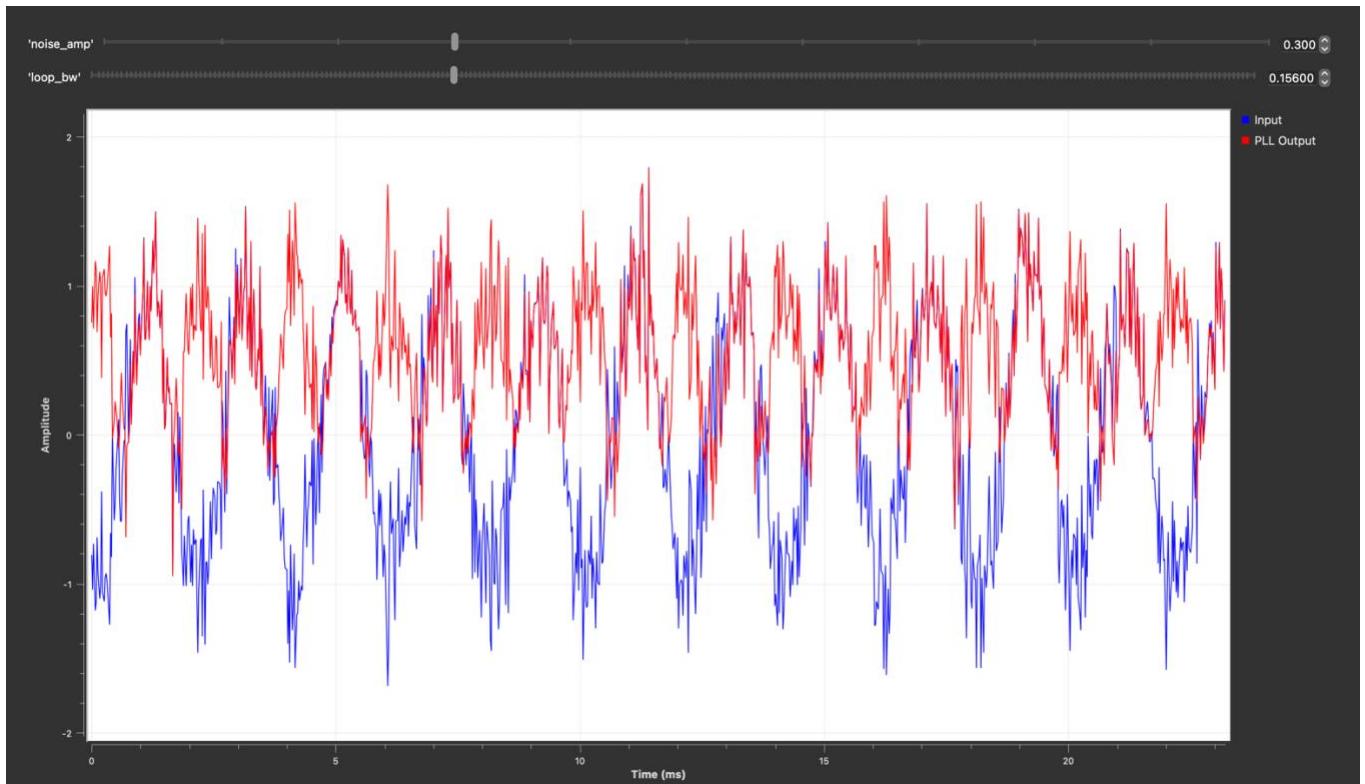


Figure 6: PLL struggling to stay locked with noise amplified

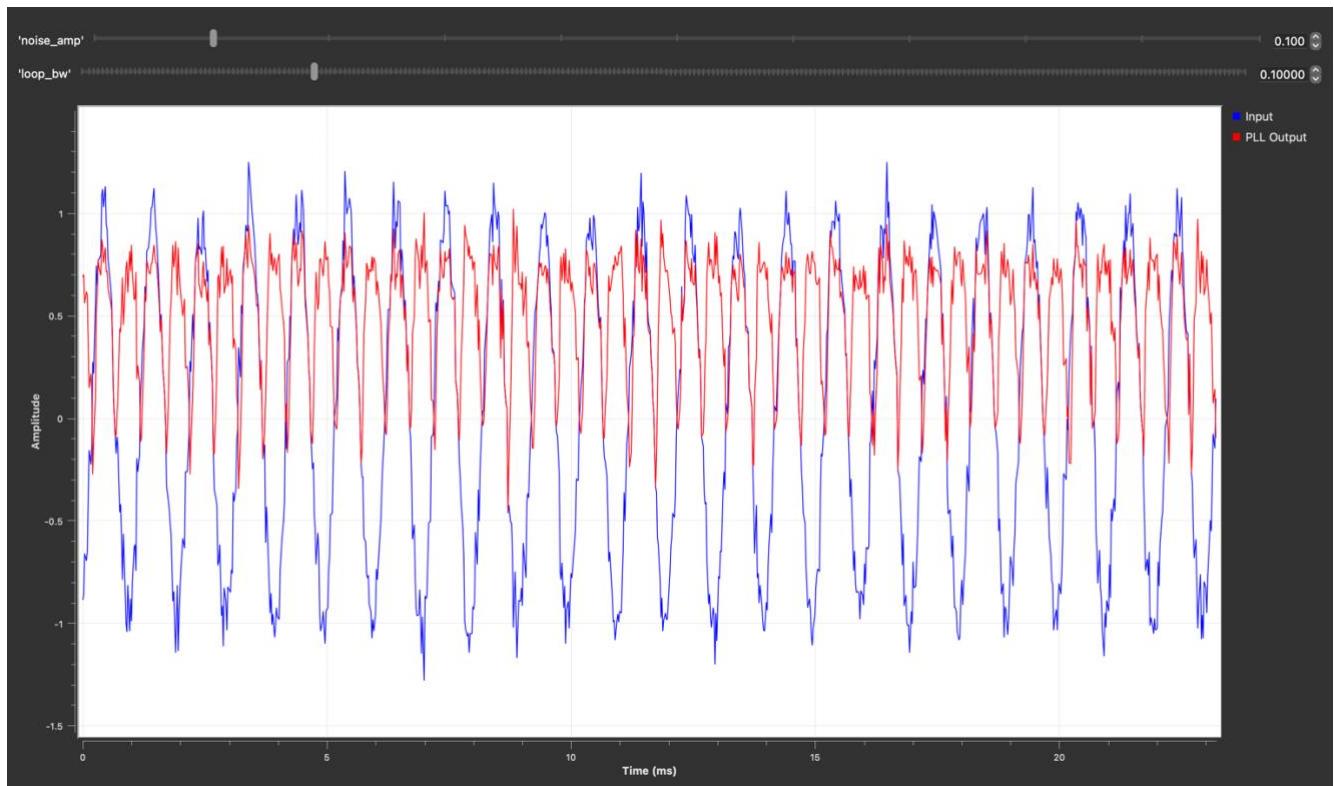


Figure 7: PLL unlocked with 1000Hz carrier

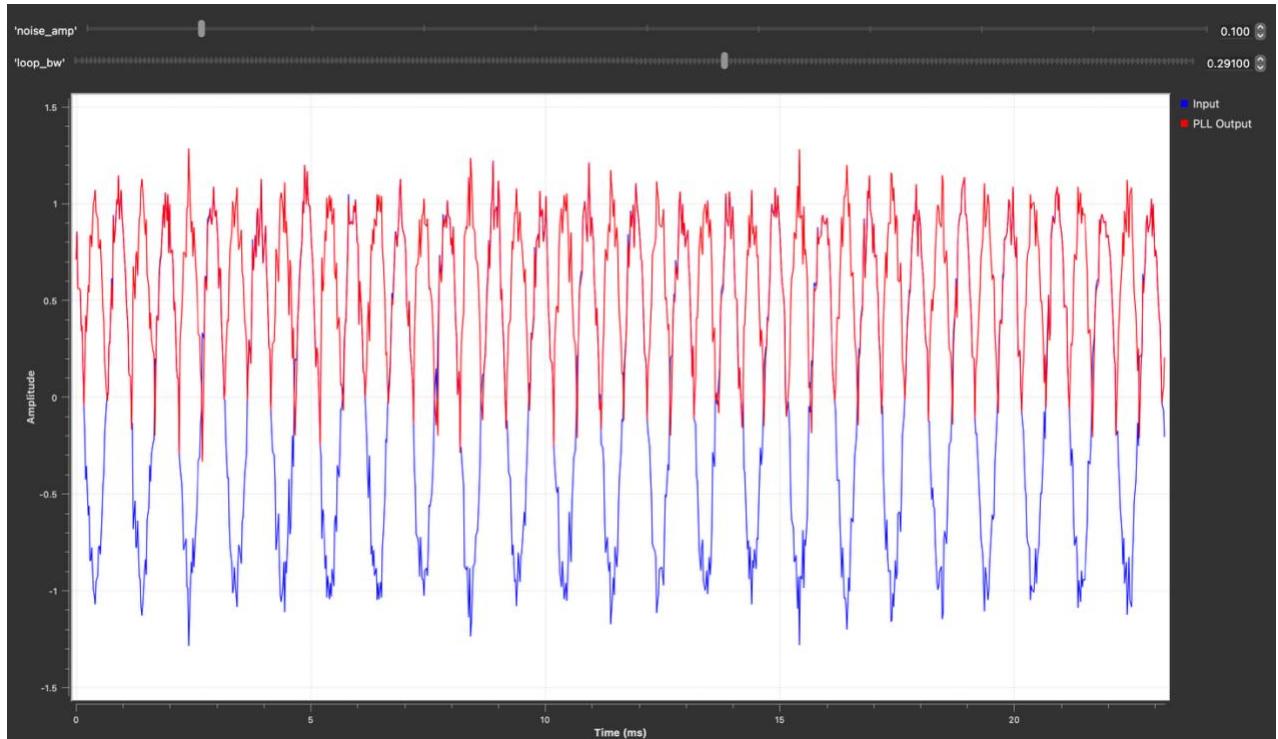


Figure 8: PLL locked with higher loop bandwidth (0.291)

For the next part of the lab (Question 8), the carrier is modulated by a 10 Hz sine wave using a multiplier block, as shown in the flowgraph in Figure 9. This created a Double Sideband Suppressed Carrier (DSB-SC) signal, which was then fed into the PLL. This type of modulation suppresses the original carrier, leaving power only in the sidebands. The effect on the PLL is pretty clear - it was completely unable to acquire a stable lock. Figures 10 and 11 demonstrate this at 250 Hz; with either a narrow or wide bandwidth, the PLL's output is unlocked and out of sync with the input signal's frequency.

This behavior persisted across all carrier frequencies. At 500 Hz (Figure 12) and 1 kHz (Figure 14), the PLL was similarly unable to lock. A further test was conducted by dramatically increasing the loop bandwidth to see if the PLL could be forced to track the signal. As seen in Figure 13 and Figure 15, this wide bandwidth causes the PLL to attempt to lock, but the result is an unstable, intermittent track. The PLL output is "pulled" by the energy in the signal's sidebands but loses this track whenever the 10 Hz message envelope passes through zero. This shows that a standard PLL cannot be used to recover a carrier from a DSB-SC signal, as the output is just as noisy and modulated as the input.

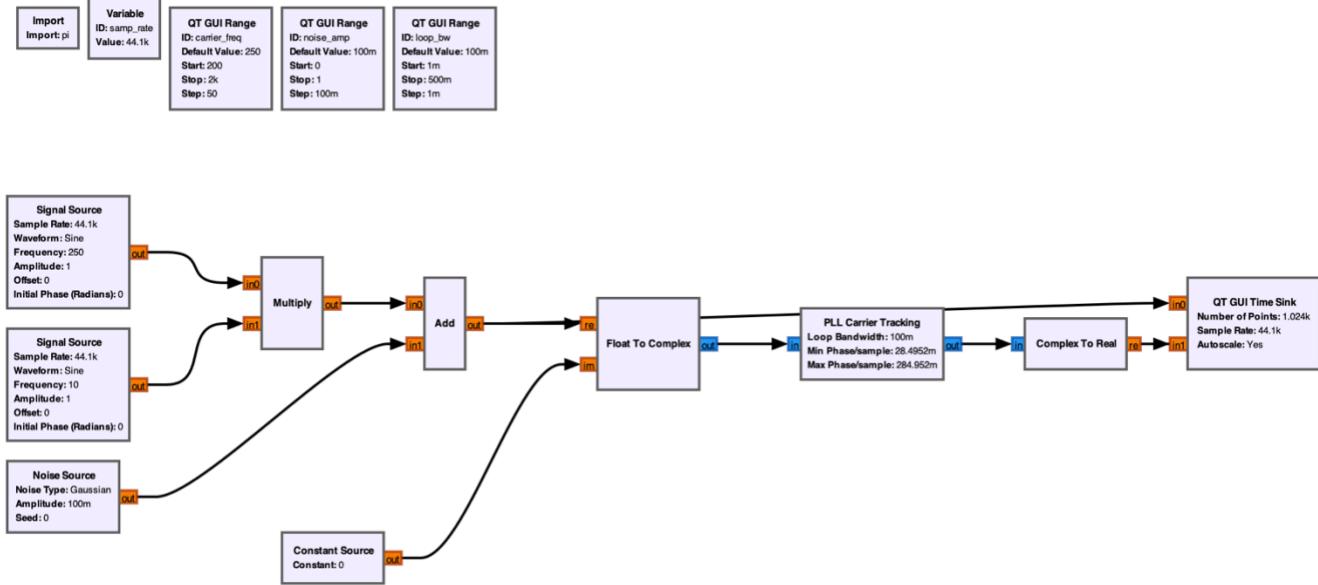


Figure 9: Block diagram with modulated carrier

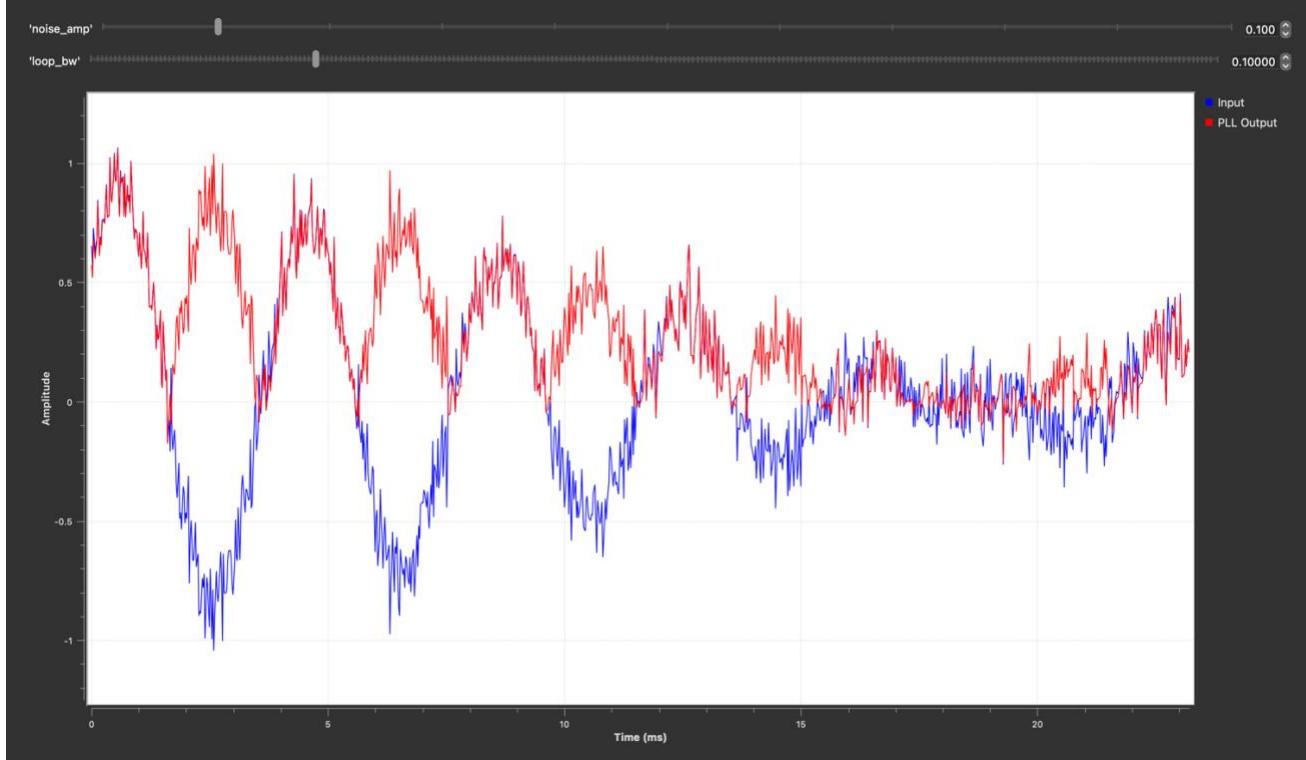


Figure 10: Modulated signal with 250Hz carrier signal modulated with 10Hz sine wave and loop bandwidth set to 0.100

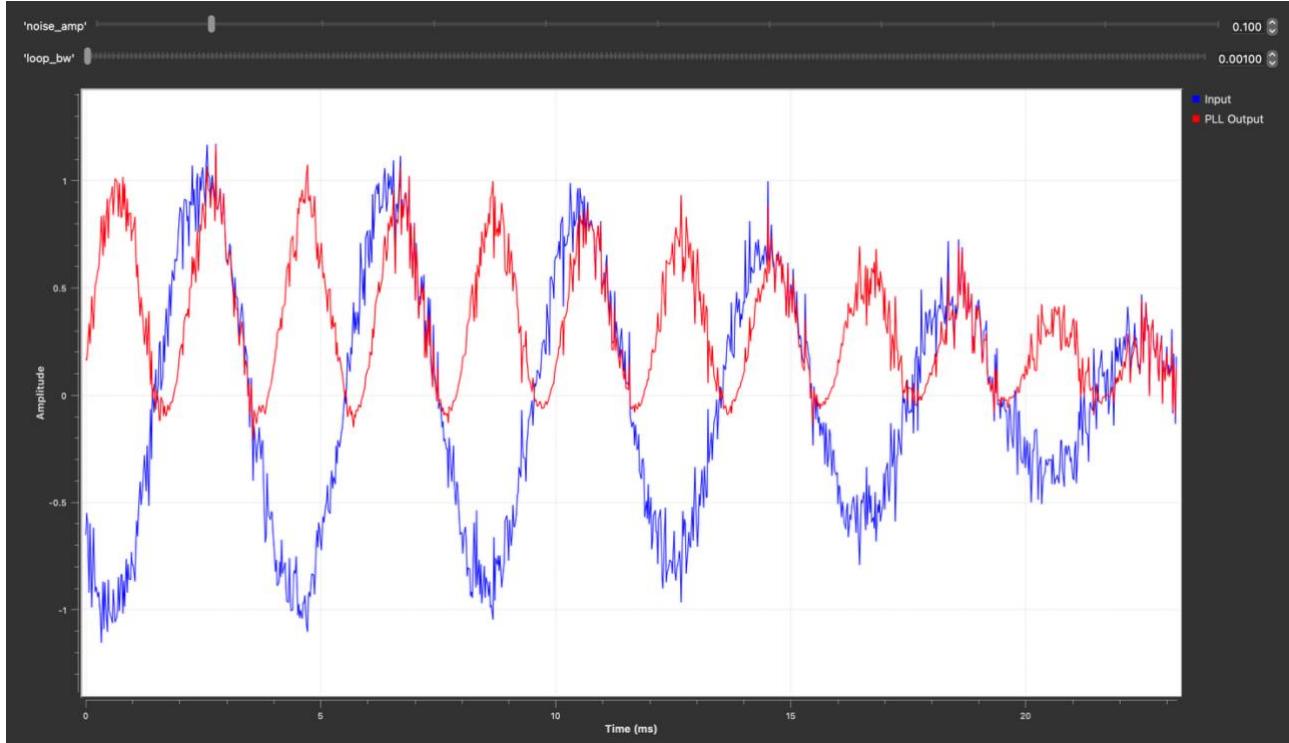


Figure 11: PLL unlocked when loop bandwidth is turned down

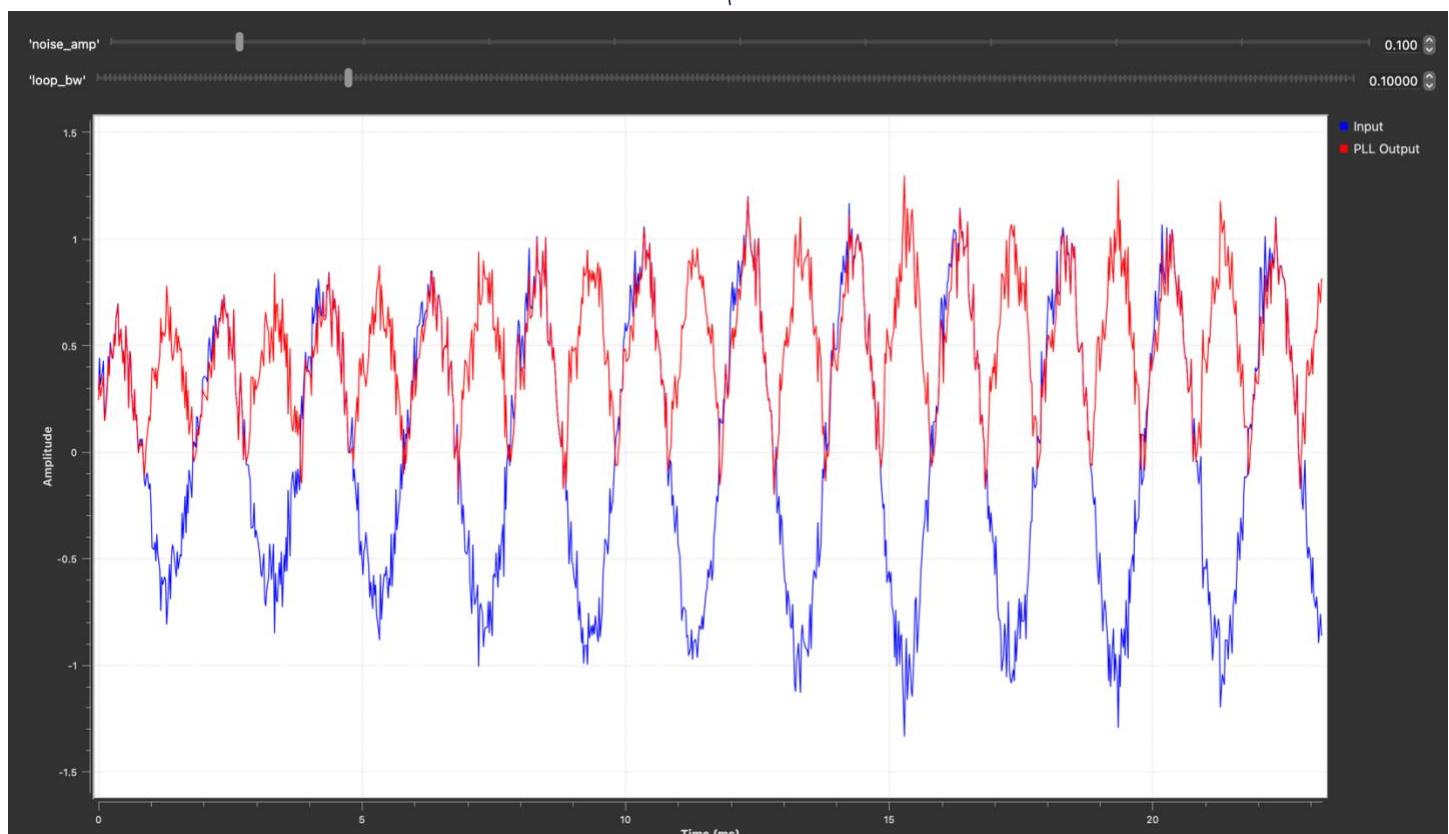


Figure 12: Carrier frequency at 500Hz, the PLL is struggling to lock and is attenuating from the modulation

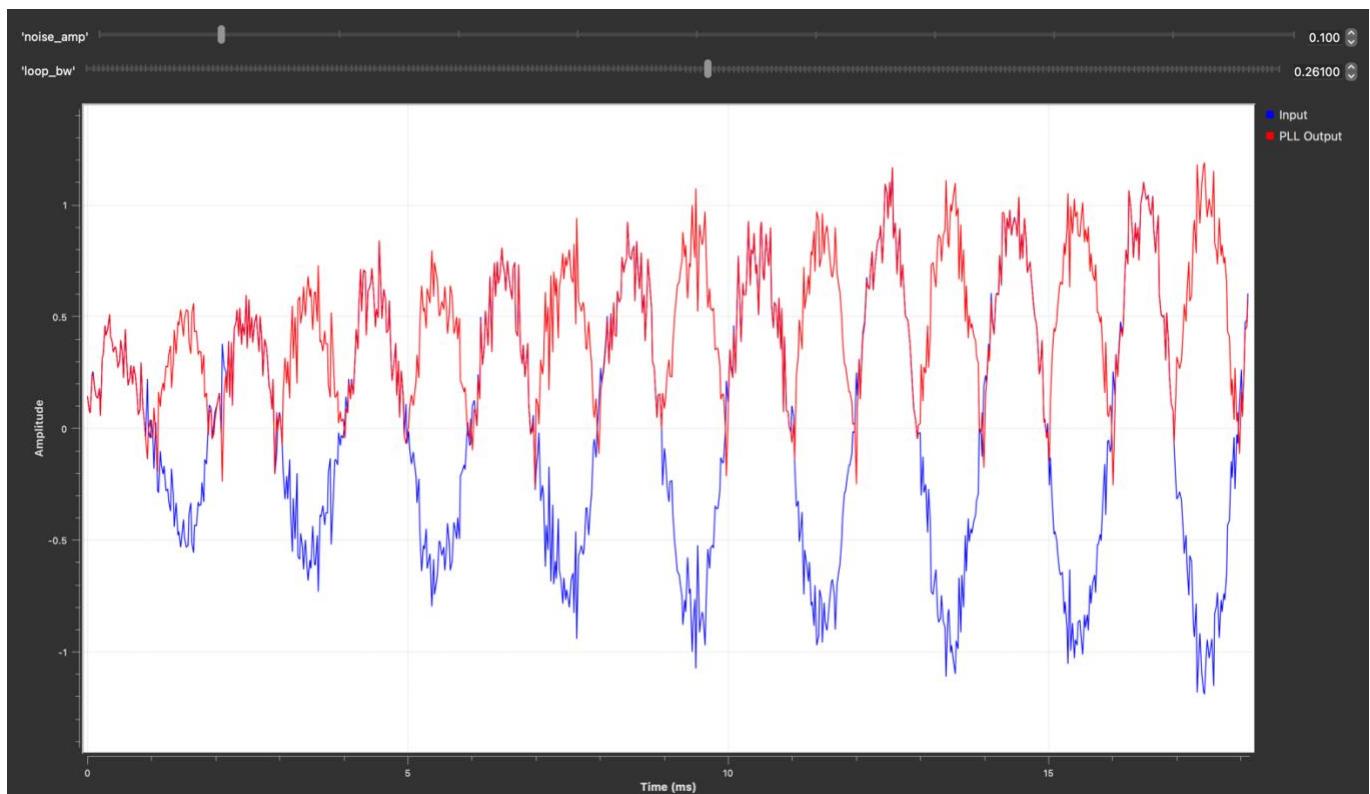


Figure 13: The PLL locks with a higher loop bandwidth but still suffers to lock at points due to the modulated signal

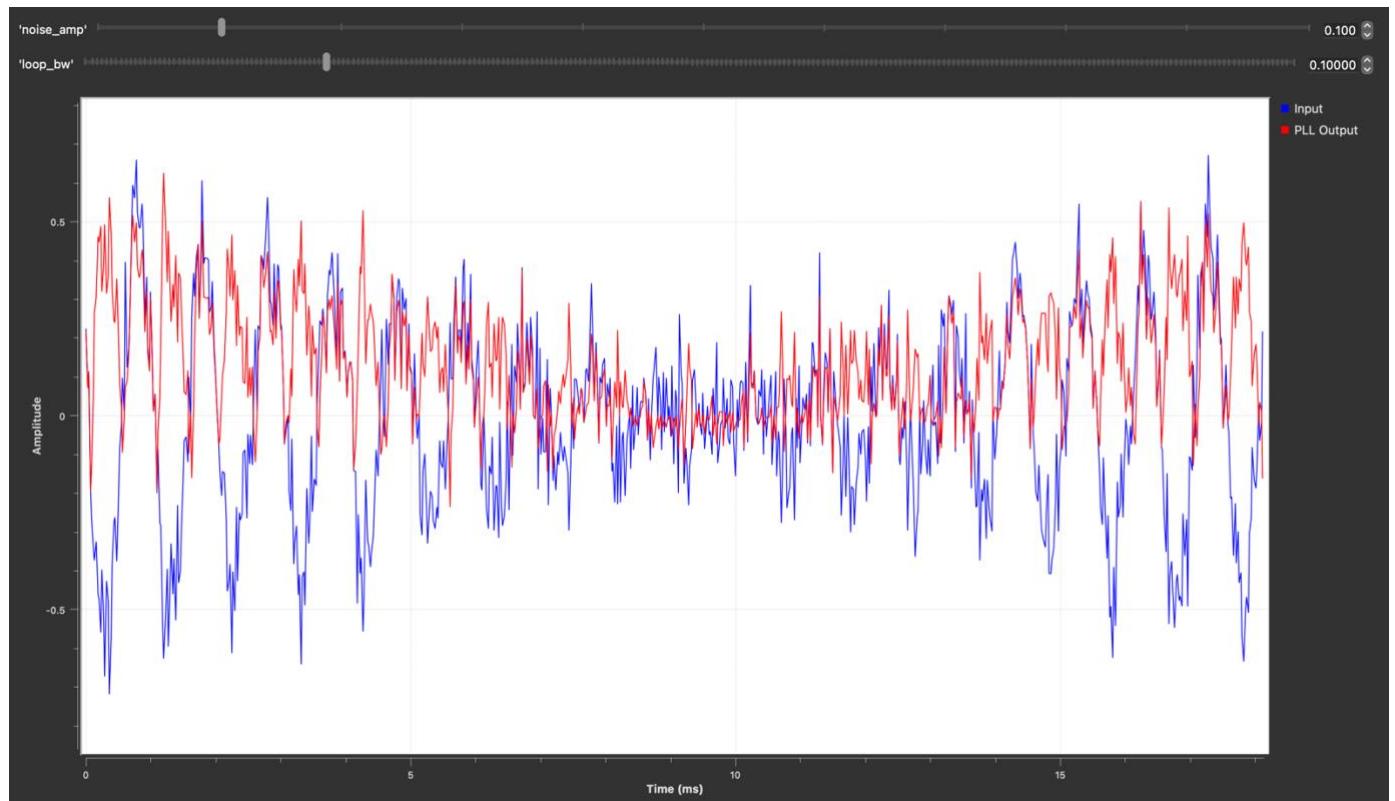


Figure 14: As expected, the PLL struggles to lock when the carrier frequency is increased to 1KHz

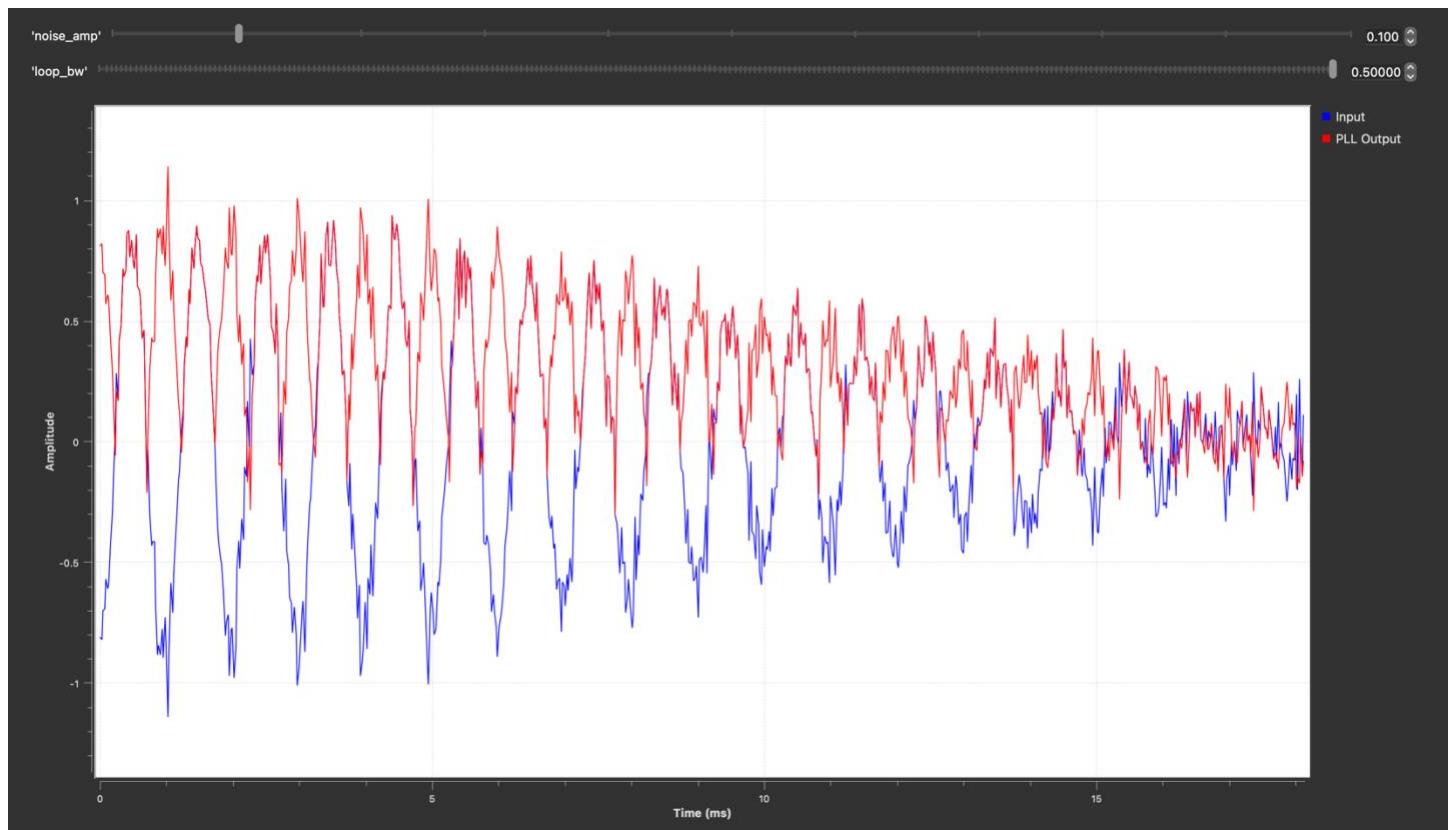


Figure 15: Carrier frequency at 1Khz with a high loop bandwidth