



ELECTRICAL MODEL DOCUMENTATION

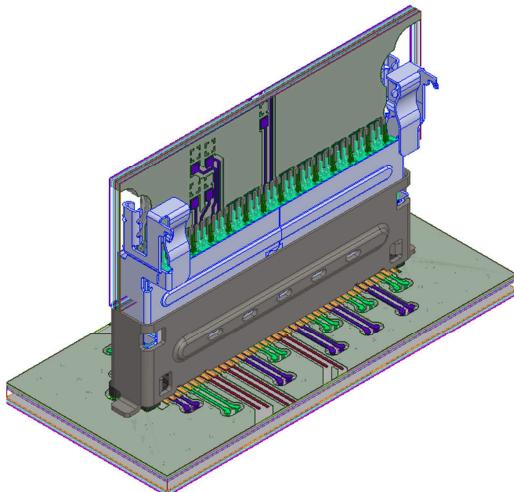
MODEL SUMMARY

This is an electrical model documentation of the Nano-Pitch IO Vertical Connector. This connector supports 25 Gb/s external applications. Eight differential TX and eight differential RX pairs (as defined on page 4) represent high speed signals.

This model can be used as a standalone model for analysis of connector performance or with other models to complete a channel.

Further information regarding this connector product line and other related Molex Nano-Pitch IO products can be found at <http://www.molex.com/>

Nano-Pitch IO Vertical Connector



MODEL TYPE: S-Parameter	MODEL FORMAT: Touchstone (*.sNp)
MODEL FILENAME: SP-173162-0010-RevA.s80p	DATA FORMAT: Magnitude/Angle
MODEL BASIS: Analytical 3-D field solution	MODEL SOURCE: ANSYS HFSS 2015.1.0
BANDWIDTH: 50 MHz – 40 GHz	RESOLUTION: 50 MHz steps
REFERENCE: 42.5 ohms	NUMBER OF POINTS: 800
NUMBER OF CHANNELS: 20 differential (16 high speed and 4 low speed)	NUMBER OF PORTS: 80 single-ended
CHANNEL TYPE: Coupled pairs + 85ohm uStrip	VALIDATION: Pending
MODEL APPLICATIONS: Pending	DATA RATE: 25 Gb/s

APPLICABLE PART NUMBER(S):

173162-03xx (Fixed)
173217-xxxx (Free)

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REVISION: A	ECN INFORMATION: EC No: UCP2016-3784 DATE: 3/23/2016	TITLE: Nano-Pitch IO Vertical to Straddle 85Ohm 80ckt Connector Electrical Model Documentation	SHEET No. 1 of 11
DOCUMENT NUMBER: EE-173162-0010	CREATED BY: K. Chen	REVIEWED BY: P. Phuyal	APPROVED BY: J. Dambach



ELECTRICAL MODEL DOCUMENTATION

MODEL DESCRIPTION

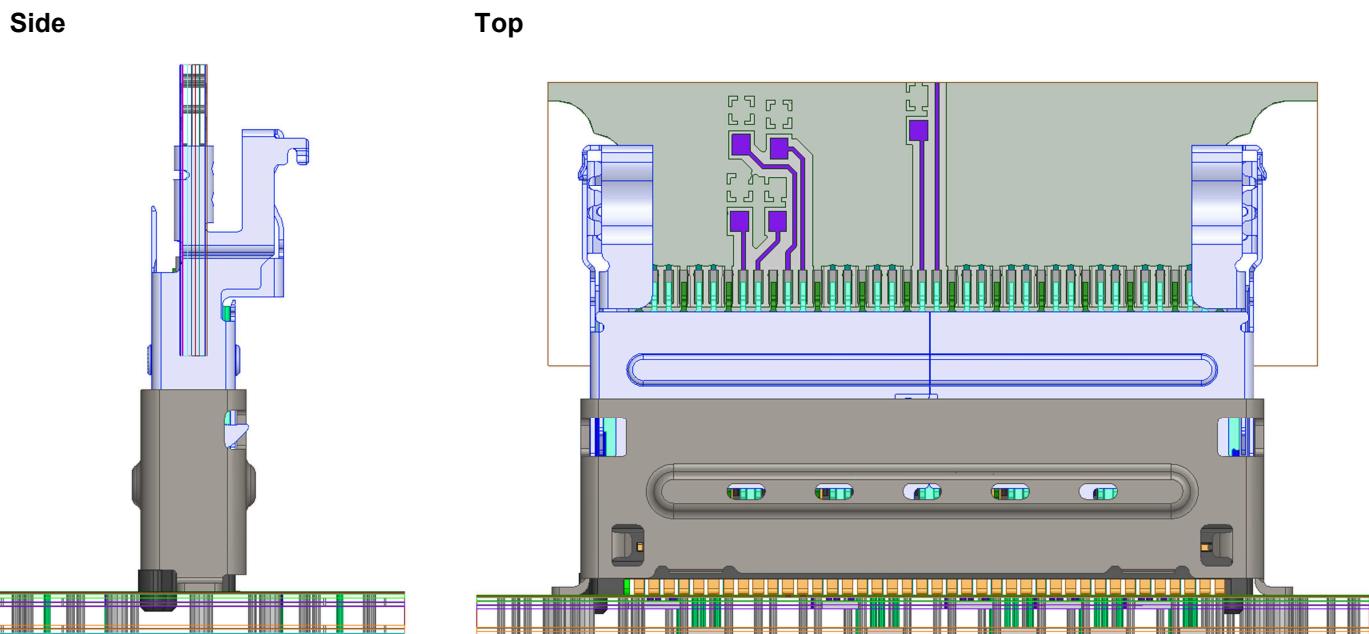
This model contains 20 differential pairs (and their associated grounds) and circuit board interfaces. It is represented by an 80-port, single-ended S-parameter matrix. The signal path simulated by the model consists of a surface mounted host circuit board interface, the Nano-Pitch IO Vertical connector, and an edge card.

The host board thickness is ~1.5 mm (0.059"). A multi-layered dielectric constant of 4.1~4.63 was used for the modeled material properties. It represents an application with at least 8 layers, 4 power/ground layers and 2 high-speed signal layers. The edge board thickness is ~0.86 mm. A multi-layered dielectric constant of 3.87~3.94 was used for the modeled material properties.

The assumptions for the data shown in this report were chosen to demonstrate the performance of the connector with a high degree of resolution. In an actual application, results will demonstrate less or different detail due to channel losses/dispersion (i.e. package and board). These assumptions include short PCB channels attached to connector, 20ps in progress rise-time, frequency independent 850hm differential ports.

PART ILLUSTRATIONS

Connector



REVISION: A	ECN INFORMATION: EC No: UCP2016-3784 DATE: 3/23/2016	TITLE: Nano-Pitch IO Vertical to Straddle 850Ohm 80ckt Connector Electrical Model Documentation	SHEET No. 2 of 11
DOCUMENT NUMBER: EE-173162-0010	CREATED BY: K. Chen	REVIEWED BY: P. Phuyal	APPROVED BY: J. Dambach

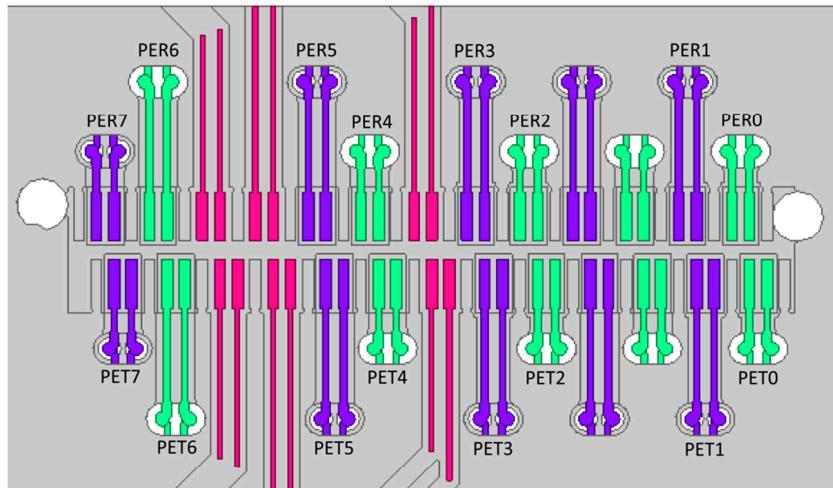


ELECTRICAL MODEL DOCUMENTATION

Host board Detail (Fixed side)

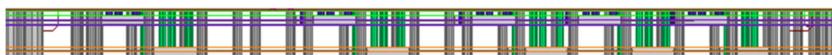
Board construction

Thickness: 59.2mil
Layers: 8 layers
Board Material: Dk = 4.1~4.63
Df = 0.0205~0.021
Copper: 1.5 oz.



Pad Dimensions

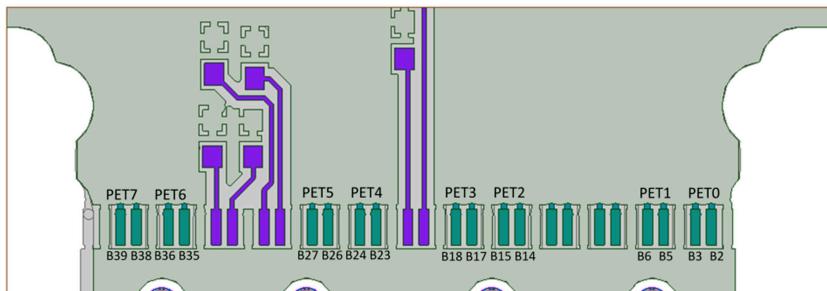
Signal: 1.4mm x 0.31mm
Ground: 1.4mm x 0.31mm



Edge card Detail (Free side)

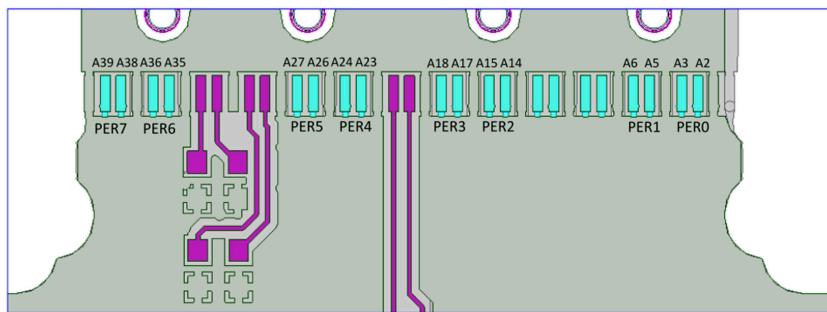
Board construction

Thickness: 0.8636mm
Layers: 6 layers
Board Material: Dk = 3.87~3.94
Df = 0.0107~0.0111
Copper: 1.5 oz.



Pad Dimensions

Signal: 1.15mm x 0.31mm
Ground: 1.15mm x 0.31mm



**Nano-Pitch IO Vertical to Straddle
85Ohm 80ckt Connector
Electrical Model Documentation**

REVISION:	ECN INFORMATION:	TITLE:	SHEET No.	
A	EC No: UCP2016-3784 DATE: 3/23/2016		3 of 11	
DOCUMENT NUMBER:		CREATED BY:	REVIEWED BY:	APPROVED BY:
EE-173162-0010		K. Chen	P. Phuyal	J. Dambach



ELECTRICAL MODEL DOCUMENTATION

STANDARD PIN OUT (SFF-9401)

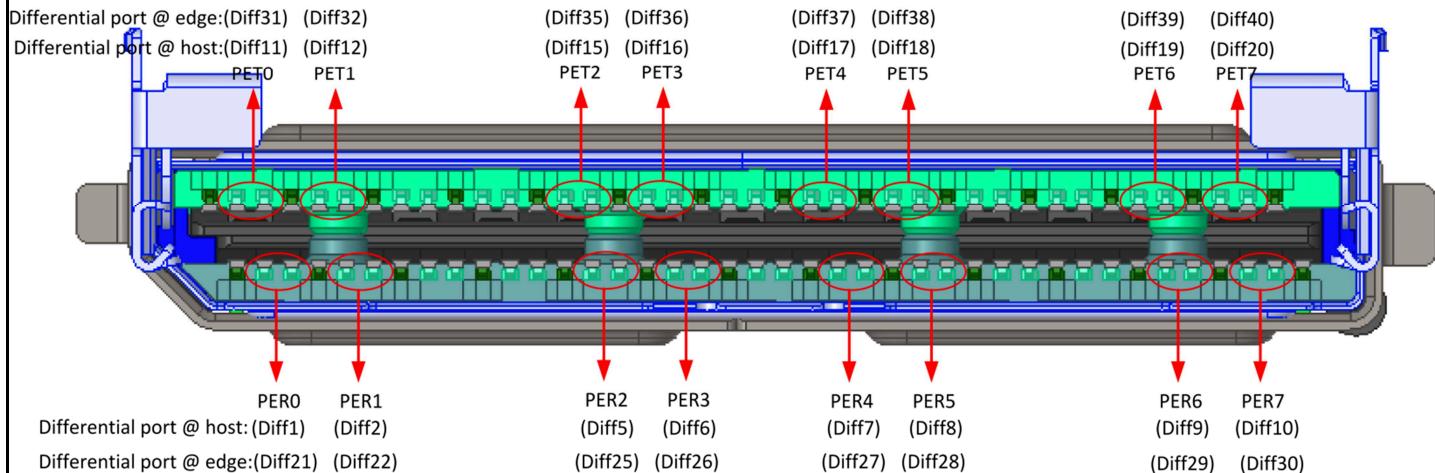
OCuLink	9400(V2)	CABLE	9400(V2)	OCuLink
PCIE	UNIVERSIAL		UNIVERSAL	PCIE
PIN	ROOT	DIR	END Point	PIN
A1	GROUND	☒	GROUND	B1
A2	PER(RX)p0	←	PET(TX)p0	B2
A3	PER(RX)n0	←	PET(TX)n0	B3
A4	GROUND	☒	GROUND	B4
A5	PER(RX)p1	←	PET(TX)p1	B5
A6	PER(RX)n1	←	PET(TX)n1	B6
A7	GROUND	☒	GROUND	B7
A8(BP_TYPE)	VSP7/SB7	←	VSP7/SB7	B8(BP_TYPE)
A9(CWAKE#)	VSP3/SB3	←	VSP3/SB3	B9(CWAKE#)
A10(GND)	VSP9/SB9	☒	VSP9/SB9	B10(GND)
A11(VSP)	VSP4/SB4	→	VSP4/SB4	B11(VSP)
A12(VSP)	VSP5/SB5	→	VSP5/SB5	B12(VSP)
A13	GROUND	☒	GROUND	B13
A14	PER(RX)p2	←	PETp2	B14
A15	PER(RX)n2	←	PETn2	B15
A16	GROUND	☒	GROUND	B16
A17	PER(RX)p3	←	PET(TX)p3	B17
A18	PER(RX)n3	←	PET(TX)n3	B18
A19	GROUND	☒	GROUND	B19
A20	RESERVED	NC	RESERVED	B20
A21	RESERVED	NC	RESERVED	B21
A22	GROUND	☒	GROUND	B22
A23	PER(RX)p4	←	PET(TX)p4	B23
A24	PER(RX)n4	←	PET(TX)n4	B24
A25	GROUND	☒	GROUND	B25
A26	PER(RX)p5	←	PET(TX)p5	B26
A27	PER(RX)n5	←	PET(TX)n5	B27
A28	GROUND	☒	GROUND	B28
A29(BP_TYPE)	VSP7/SB7	←	VSP7/SB7	B29(BP_TYPE)
A30(CWAKE#)	VSP3/SB3	←	VSP3/SB3	B30(CWAKE#)
A31(GND)	VSP9/SB9	☒	VSP9/SB9	B31(GND)
A32(VSP)	VSP4/SB4	→	VSP4/SB4	B32(VSP)
A33(VSP)	VSP5/SB5	→	VSP5/SB5	B33(VSP)
A34	GROUND	☒	GROUND	B34
A35	PER(RX)p6	←	PETp6	B35
A36	PER(RX)n6	←	PETn6	B36
A37	GROUND	☒	GROUND	B37
A38	PER(RX)p7	←	PET(TX)p7	B38
A39	PER(RX)n7	←	PET(TX)n7	B39
A40	GROUND	☒	GROUND	B40

REVISION: A	ECN INFORMATION: EC No: UCP2016-3784 DATE: 3/23/2016	TITLE: Nano-Pitch IO Vertical to Straddle 85Ohm 80ckt Connector Electrical Model Documentation	SHEET No. 4 of 11
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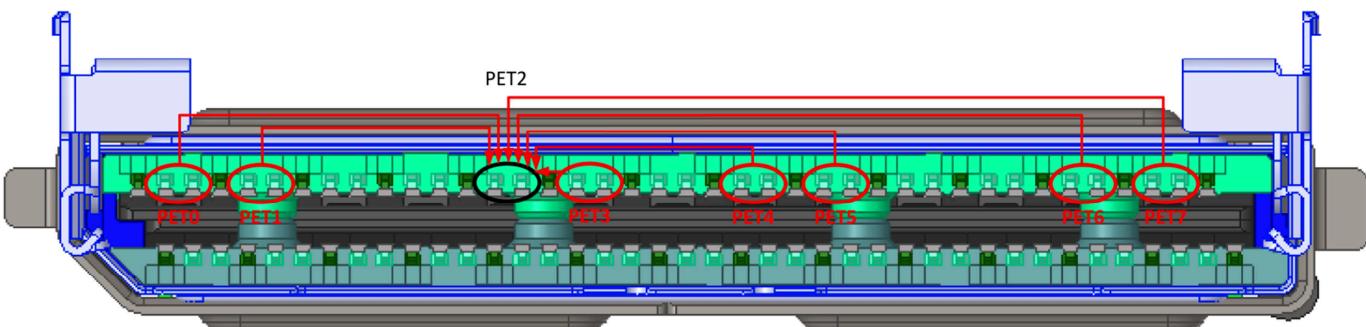
ELECTRICAL MODEL DOCUMENTATION

TERMINAL TO MODEL PORT MAPPING

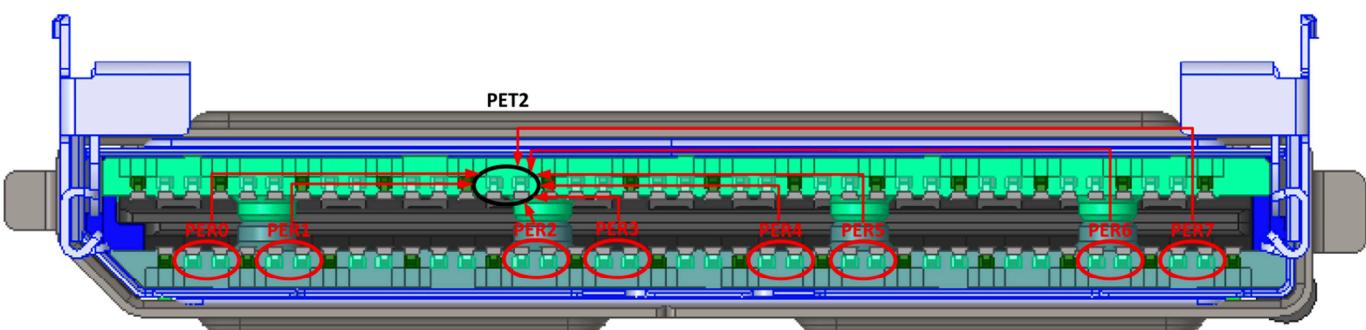


CROSSTALK MAP 1

Victim: PET2 (high speed pairs)
Far-end Differential Crosstalk (FEXT)



Near-end Differential Crosstalk (NEXT)



REVISION:	ECN INFORMATION:	TITLE:	SHEET No.	
A	EC No: UCP2016-3784 DATE: 3/23/2016	Nano-Pitch IO Vertical to Straddle 85Ohm 80ckt Connector Electrical Model Documentation	5 of 11	
DOCUMENT NUMBER:		CREATED BY:	REVIEWED BY:	APPROVED BY:
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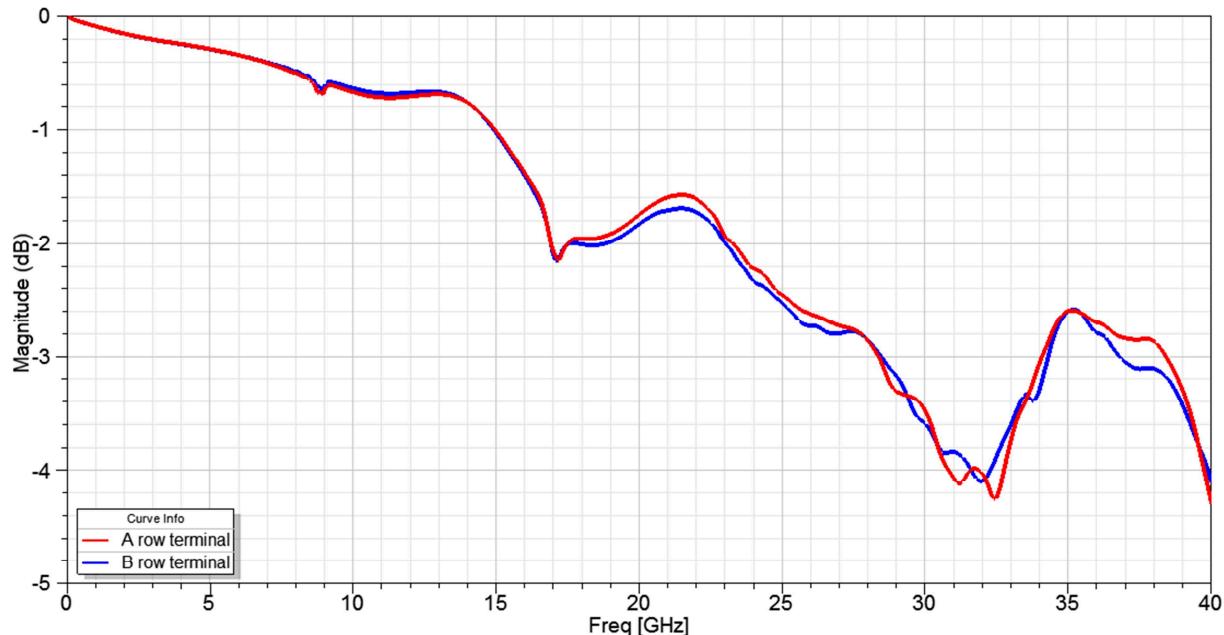


ELECTRICAL MODEL DOCUMENTATION

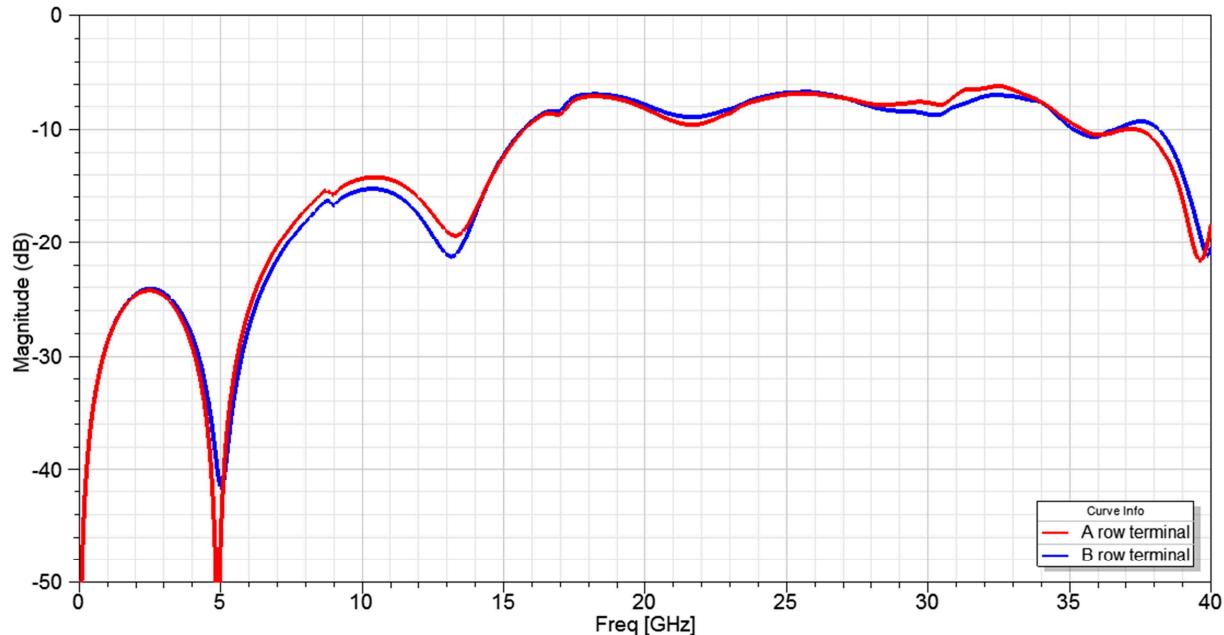
REFERENCE RESULTS

Frequency Domain

Differential Insertion Loss



Differential Return Loss



REVISION: A	ECN INFORMATION: EC No: UCP2016-3784 DATE: 3/23/2016	TITLE: Nano-Pitch IO Vertical to Straddle 85Ohm 80ckt Connector Electrical Model Documentation	SHEET No. 6 of 11
DOCUMENT NUMBER: EE-173162-0010	CREATED BY: K. Chen	REVIEWED BY: P. Phuyal	APPROVED BY: J. Dambach

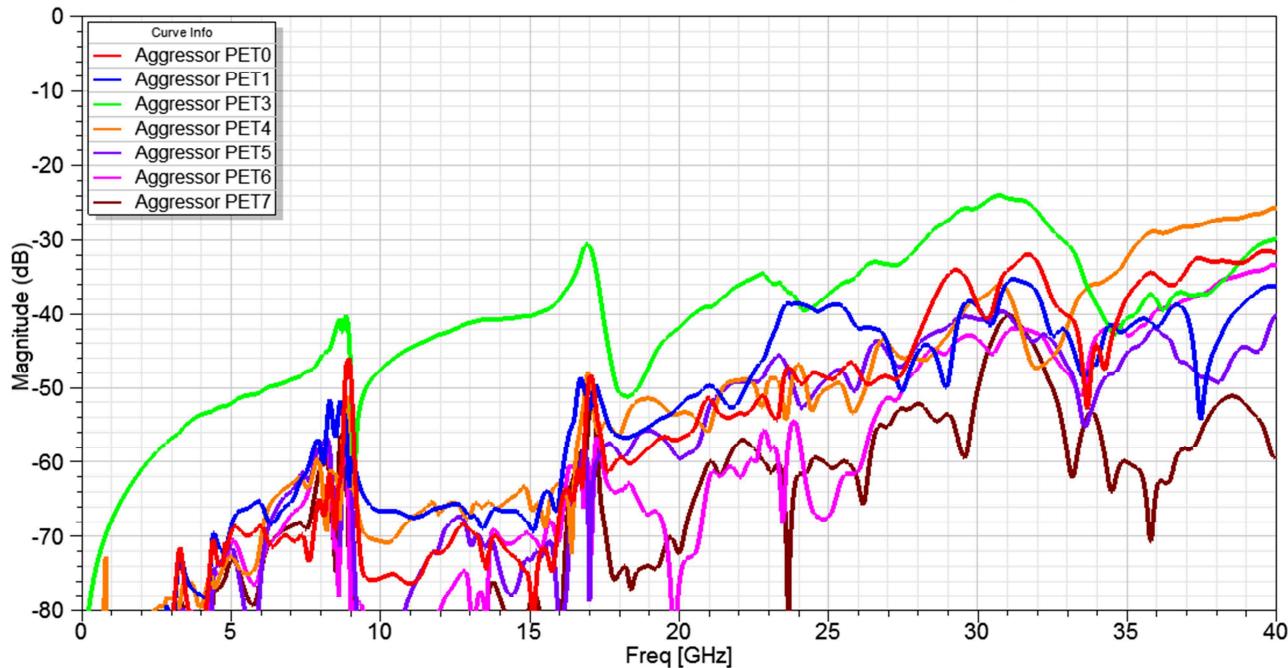


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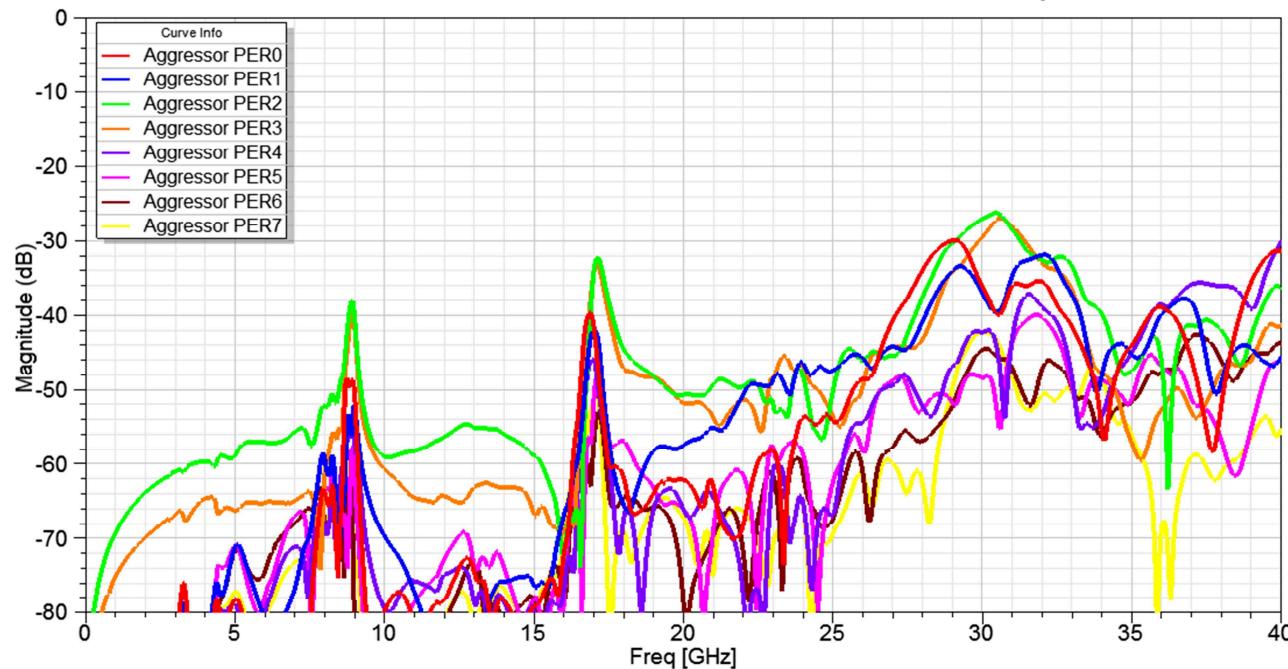
REFERENCE RESULTS

Frequency Domain (continued)

Far-end Differential Crosstalk at the Terminal (PET2) in Row B as shown on page 5



Near-end Differential Crosstalk at The Terminal (PET2) in Row B as shown on page 5



REVISION:	ECN INFORMATION: EC No: UCP2016-3784 DATE: 3/23/2016	TITLE: Nano-Pitch IO Vertical to Straddle 85Ohm 80ckt Connector Electrical Model Documentation	SHEET No. 7 of 11
DOCUMENT NUMBER:	EE-173162-0010	CREATED BY: K. Chen	REVIEWED BY: P. Phuyal
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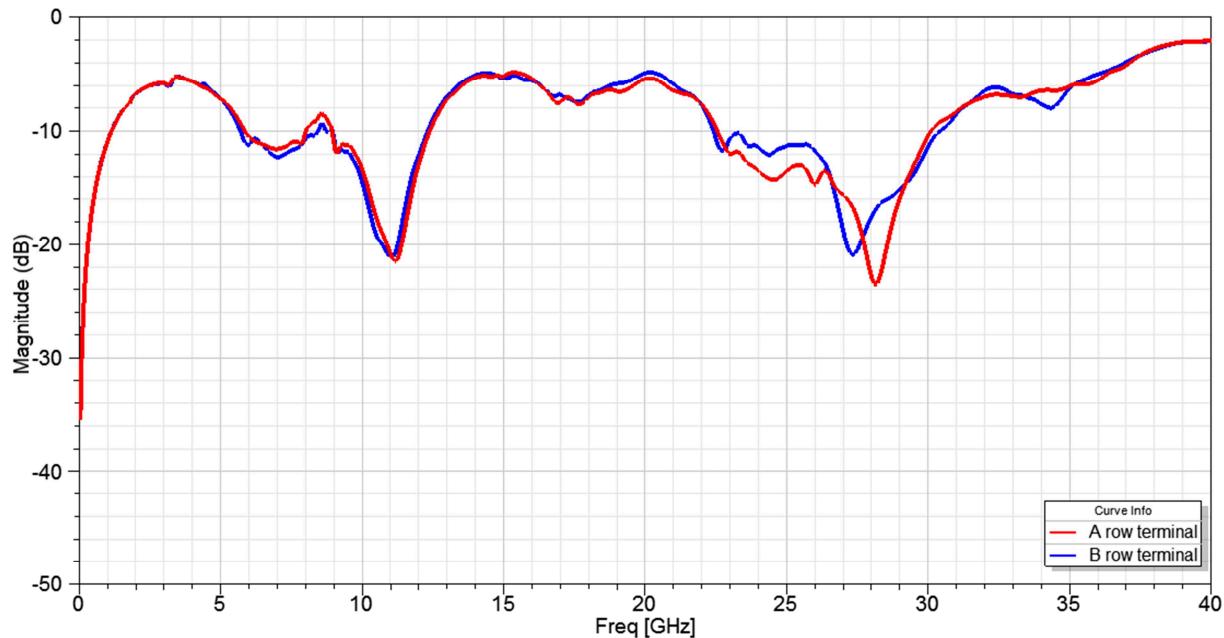


ELECTRICAL MODEL DOCUMENTATION

REFERENCE RESULTS

Frequency Domain (continued)

Common Mode Return Loss



REVISION: A	ECN INFORMATION: EC No: UCP2016-3784 DATE: 3/23/2016	TITLE: Nano-Pitch IO Vertical to Straddle 85Ohm 80ckt Connector Electrical Model Documentation	SHEET No. 8 of 11
DOCUMENT NUMBER: EE-173162-0010	CREATED BY: K. Chen	REVIEWED BY: P. Phuyal	APPROVED BY: J. Dambach

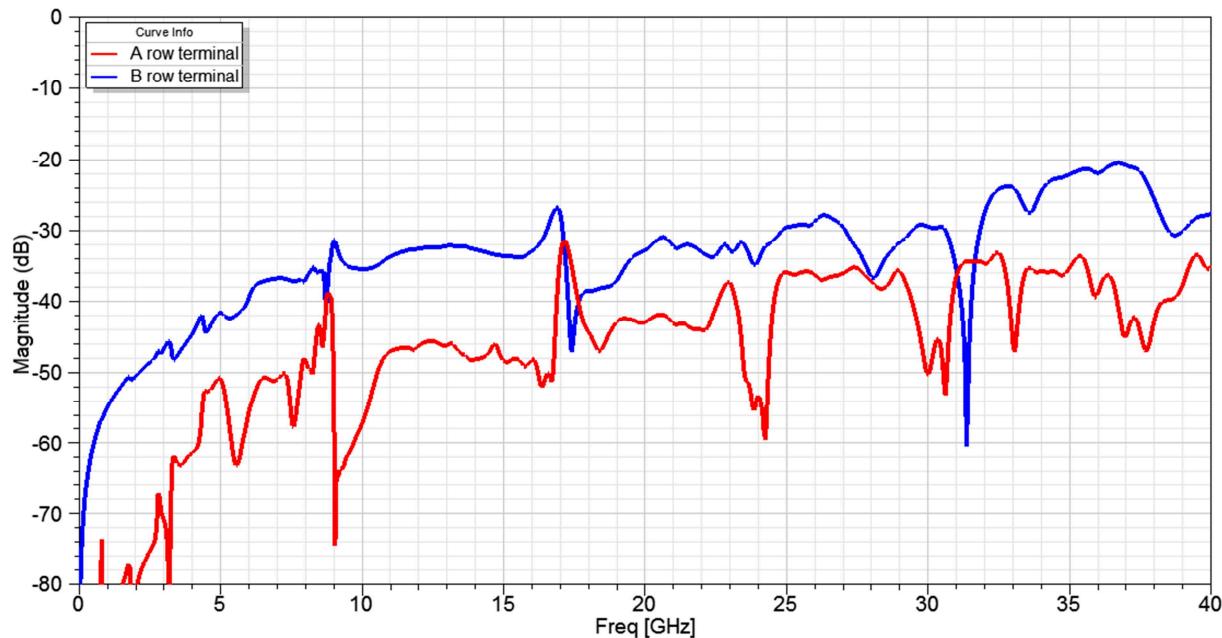


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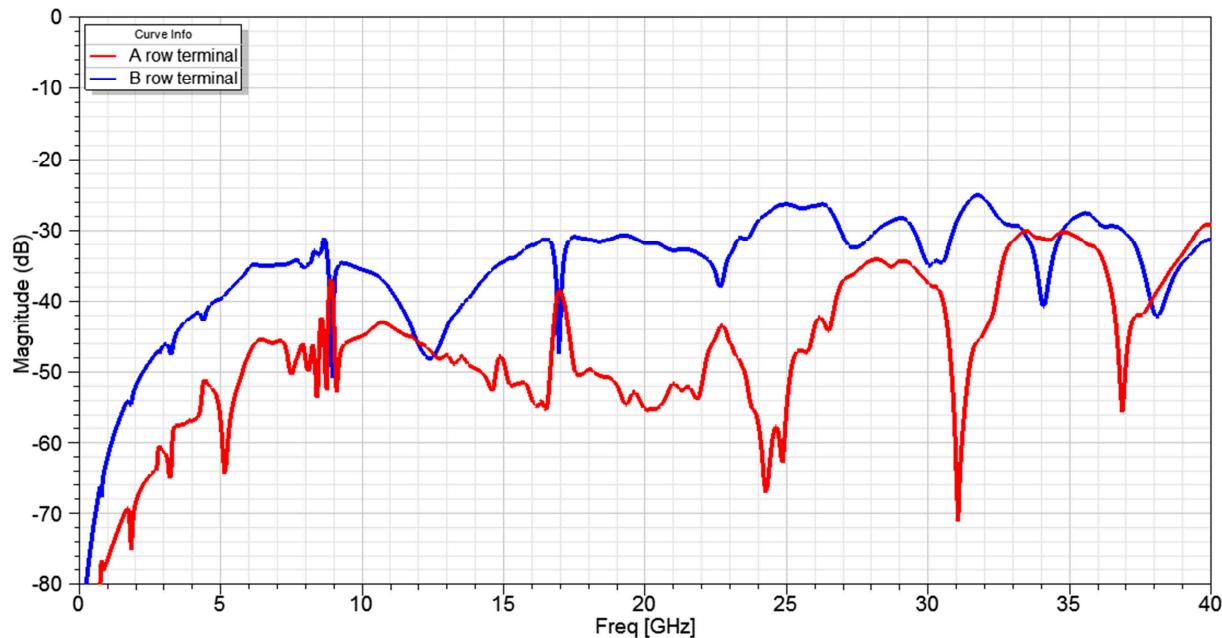
REFERENCE RESULTS

Frequency Domain (continued)

Differential-to-Common Mode Thru Conversion



Differential-to-Common Mode Reflected Conversion



REVISION: A	ECN INFORMATION: EC No: UCP2016-3784 DATE: 3/23/2016	TITLE: Nano-Pitch IO Vertical to Straddle 85Ohm 80ckt Connector Electrical Model Documentation	SHEET No. 9 of 11
DOCUMENT NUMBER: EE-173162-0010	CREATED BY: K. Chen	REVIEWED BY: P. Phuyal	APPROVED BY: J. Dambach

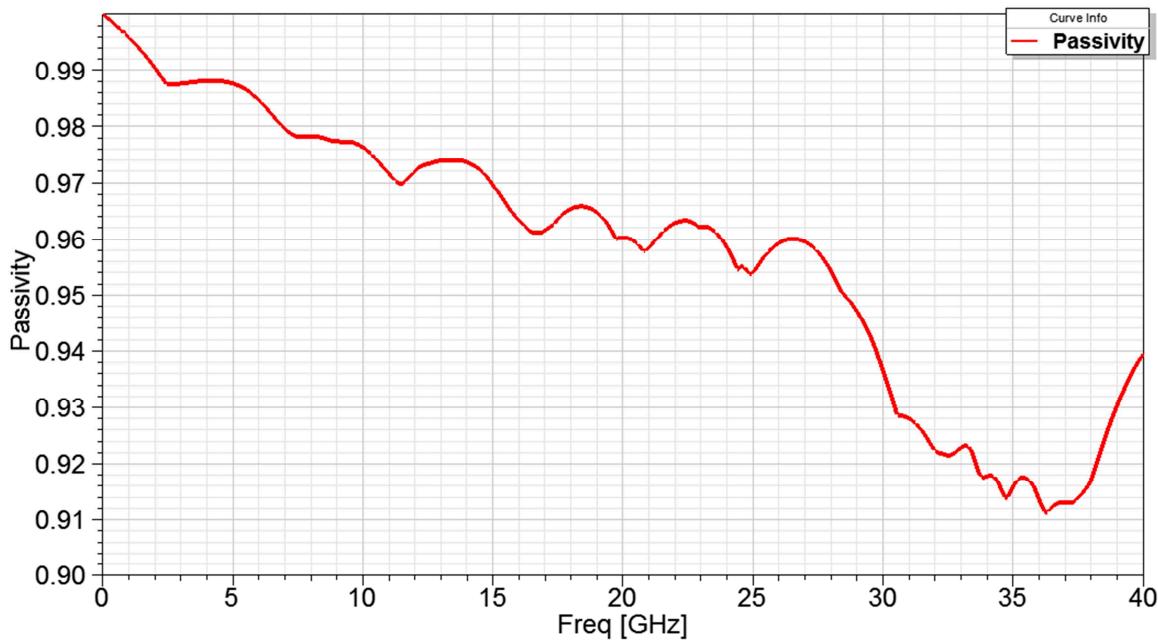


ELECTRICAL MODEL DOCUMENTATION

REFERENCE RESULTS

Frequency Domain (continued)

The passivity of the model, unlike S-parameter results, does not indicate the expected electrical performance of the simulated connector. Rather, it is one of a number of ways to determine the accuracy of the S-parameter model in describing the connector's electrical performance. Since (unless specifically designed to incorporate active components) all connectors are passive devices, the associated model should also be passive at all frequencies. While small non-passivity at isolated frequencies within a model does not necessarily mean that the S-parameters generated are without validity. The presence of non-passivity within a model does suggest caution in its use and closer investigate of the results.



The model is passive at all frequencies based on Ansys HFSS passivity checker. Other methods of checking passivity may return different results based on the methods used. Very small passivity issues should have a negligible impact on the electrical simulation results.

REVISION: A	ECN INFORMATION: EC No: UCP2016-3784 DATE: 3/23/2016	TITLE: Nano-Pitch IO Vertical to Straddle 85Ohm 80ckt Connector Electrical Model Documentation	SHEET No. 10 of 11
DOCUMENT NUMBER: EE-173162-0010	CREATED BY: K. Chen	REVIEWED BY: P. Phuyal	APPROVED BY: J. Dambach



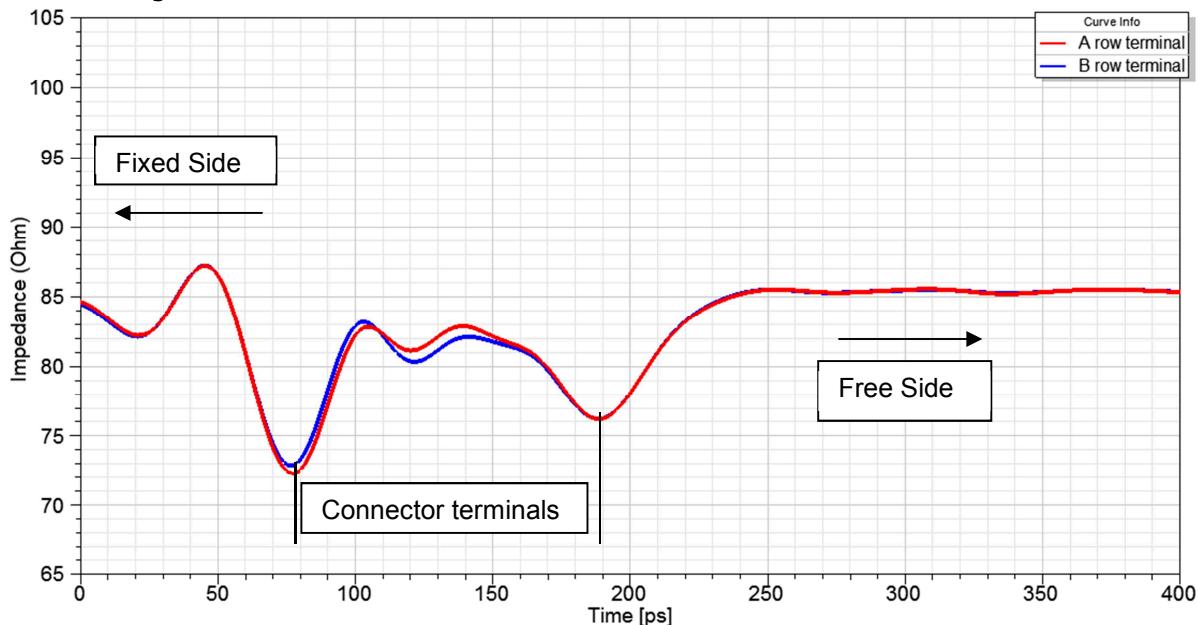
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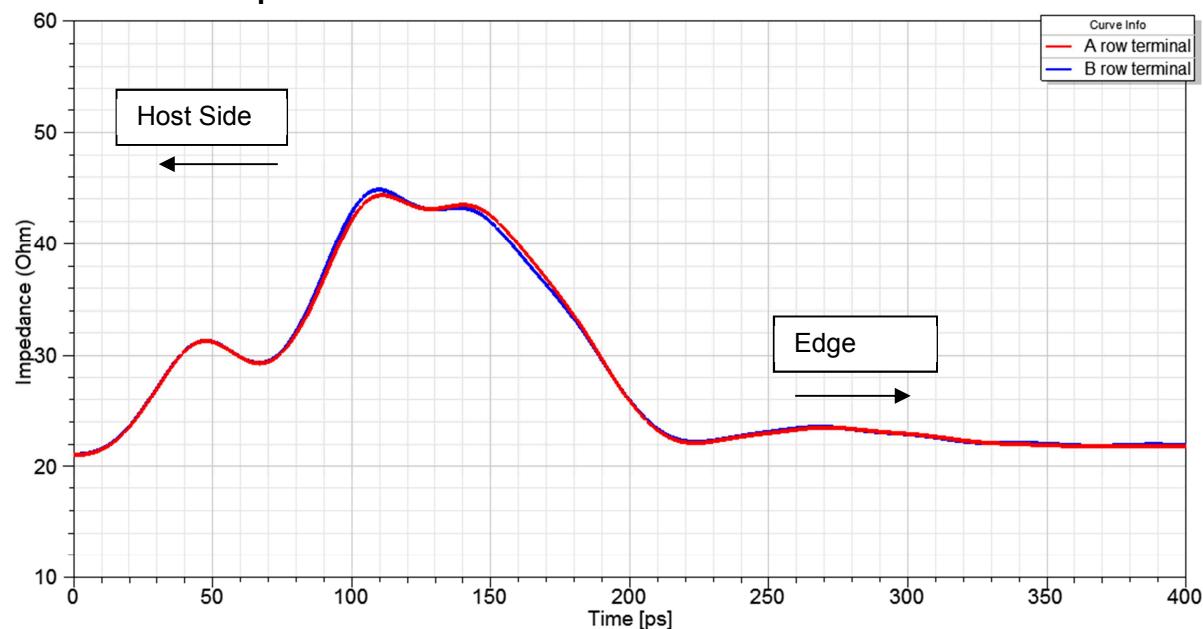
Time Domain

Differential TDR Response

- Based on frequency-to-time domain transformation within Ansys HFSS application
- Rise-time of 20ps (10-90%) at connector launch to provide high resolution of performance
- Looking from the Host Side



Common Mode TDR Response



REVISION: A	ECN INFORMATION: EC No: UCP2016-3784 DATE: 3/23/2016	TITLE: Nano-Pitch IO Vertical to Straddle 85Ohm 80ckt Connector Electrical Model Documentation	SHEET No. 11 of 11
DOCUMENT NUMBER: EE-173162-0010	CREATED BY: K. Chen	REVIEWED BY: P. Phuyal	APPROVED BY: J. Dambach