UNIVERSITY OF BRISTOL

ADVANCED COMPUTER ARCHITECTURE

DESIGNING A SUPERSCALAR PROCESSOR (FIRST FORMATIVE ASSIGNMENT)

INSTRUCTION SET AND CLOCK CYCLES TO EXECUTE

Data Transfer

LI - **1** cycle
LA - **1** cycle
LW - **1** cycle
SW - **1** cycle

Arithmetic

ADD - **1** cycle
ADDI - **1** cycle
MUL - **2** cycles
DIV - **4** cycles
SUB - **1** cycle

Control

BEQ - **2** cycles
BNE - **2** cycles
BGE - **2** cycles
BLT - **2** cycles
J - **1** cycle
JR - **1** cycle

Floating Point

FADD - **4** cycles
FSUB - **4** cycles
FMUL - **6** cycles
FDIV - **20** cycles
FSQRT - **10** cycles
MADD - **10** cycles

Other

NOP - **1** cycle
ECALL - **1** cycle

QUESTION TO PROF: IS THIS REALISTIC?

BASELINE PROGRAMS

Vector Addition
Factorial
Calculate sigmoid function for vector
Matrix multiplication
One Convolution operation
Backpropagation algorithm

DESIGN OF THE ARCHITECTURE

General

32 general purpose registers
32 floating point registers

Five stage pipeline

1) Fetch
2) Decode
3) Execute
4) Memory
5) Write back

Execution units

4 ALUs, 1 Branch Unit
Question to prof: What other execution units can we add?

Approaches

1) Tomasulos algorithm for out of order execution

Branch prediction

1) Static
2) Dynamic
3) Speculative
4) Neural network

ANALYSIS TO BE CONDUCTED

Types of analysis

- CPI for different algorithms
- CPI for different branch prediction approaches
- State how many way super scalar the processor is
- Analyze the impact of using a neural predictor for branch prediction
- Analyze the impact of pipelining
- Break down of percentage usage of instruction types

What other types of analysis can we perform?