The Art Thief:

This project, THE ART THIEF, represents the amalgamation of theoretical concepts from ECE 3300 with practical application using the Nexys A7 FPGA board. It simulates the decoding of a 3-digit padlock within a time limit to reveal an image. Using Verilog, it manages game progression, initiates timers, interprets switch inputs, and synchronizes game elements.

Power Consumption and Temperature:

Total On-Chip Power	0.214 W
Static Power	0.098 W
Dynamic Power	0.116 W
Junction Temperature	26°C

Project Implementation Overview:

Specification	Utilization
LUT	0.25%
FF	0.08%
BRAM	8.89%
IO	25.24%
PLL	16.67%

Project Timing Results:

Timing Category	Time
Worst Negative Slack	6.19 ns
Total Negative Slack	0 ns
Worst Hold Slack	0.175 ns
Total Hold Slack	0 ns