Low-Power High-Performance Reconfigurable Computing using FPGA (LPHP-RC)

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Abstract

As the demand for computational power increases, the need to develop cost efficient methods for computing is constantly rising. To help solve this issue, our research is dedicated towards developing low power computational technology while being a cost-efficient solution compared to other resources. The project is aimed towards using Field Programmable Gate Array (FPGA) platforms that can be reconfigured to run applications that can be used in image processing, cyber security, encryption, and high-performance applications for Defense. The objective is to run an application on the FPGA board using a softcore processor (Microblaze) that will be able to efficiently run the C code. Our main test was aimed towards benchmarking using various encryptions on the soft core processor to generate encryption keys. The next objective is to design communication interfaces to connect multiple low-power FPGA platforms for rapid scalability. This allows the FPGA boards to be used at large scale projects and support the high computational demand for the power-hungry applications.

Microblaze

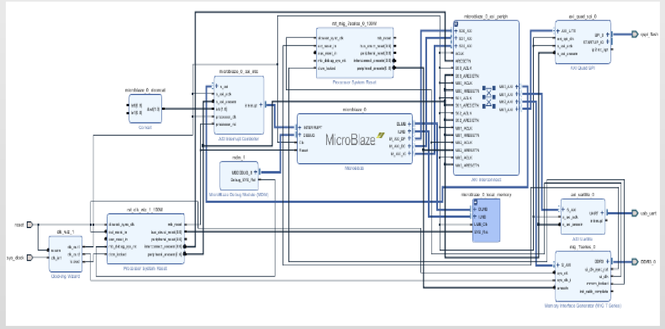


Figure 1: Block Diagram for Microblaze

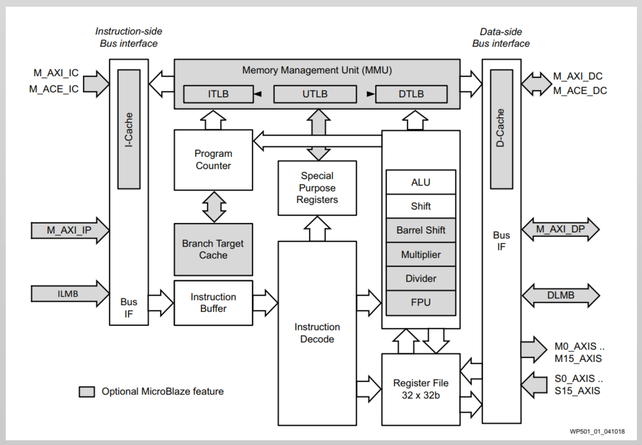
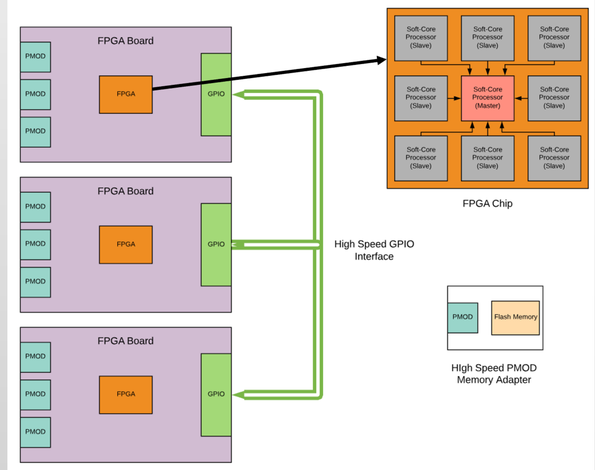
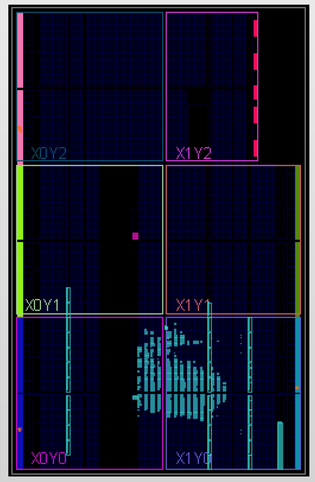


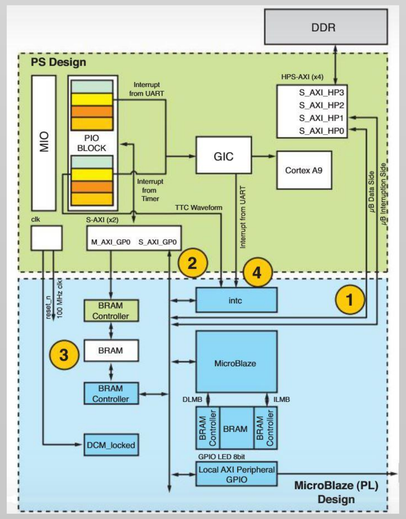
Figure 2: Microblaze Block Diagram

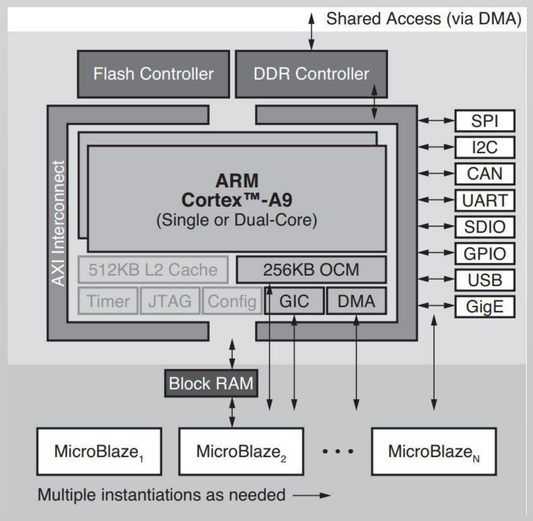
Github QR Code

Multicore Implementation









Encryption Benchmarks

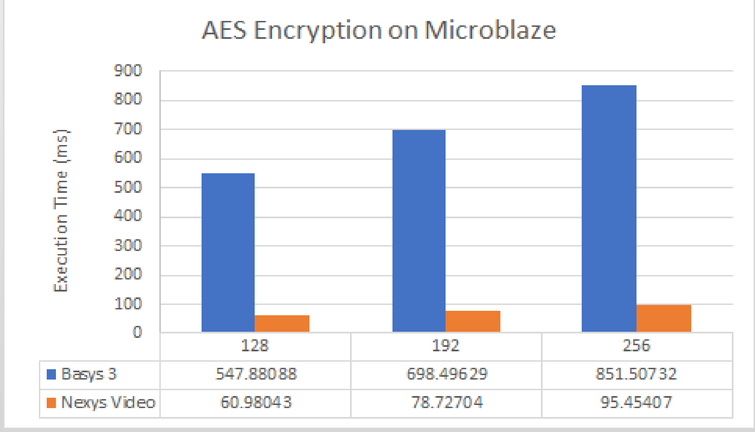


Figure 3: AES 128, 192, 256bit implementation results

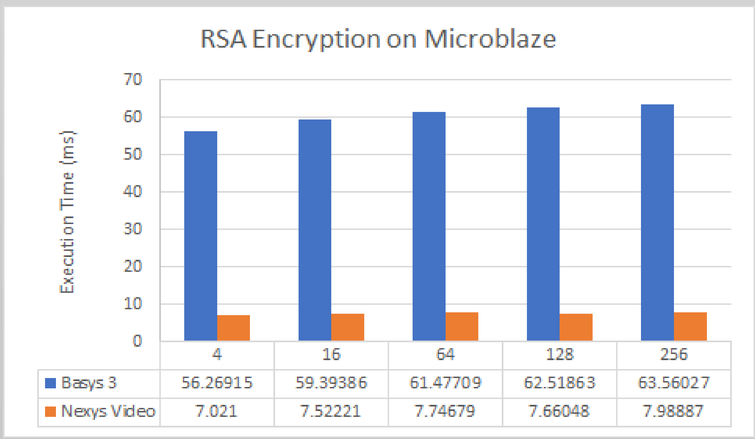


Figure 4: RSA Encryption results