Reference Design for Alpha Data ADM-PCIE-KU3 2DDR v3.0 (Kintex UltraScale KU060)

The Xilinx SDAccel 2DDR reference design v3.0 for the Alpha Data ADM-PCIE-KU3 board targets the Kintex UltraScale KU060 device, and is the design which was also used to create the corresponding .dsa file provided with this release of SDAccel software.

Block diagram

The refdesign_xilinx_adm-pcie-ku3_2ddr_3_0 project block diagram's top level of hierarchy contains two cells: base_region, which contains IP primarily related to host interaction with base platform and logic to isolation partial reconfiguration; and expanded_region, which contains IP primarily associated with the reconfigurable region, including the ocl_block IP core.

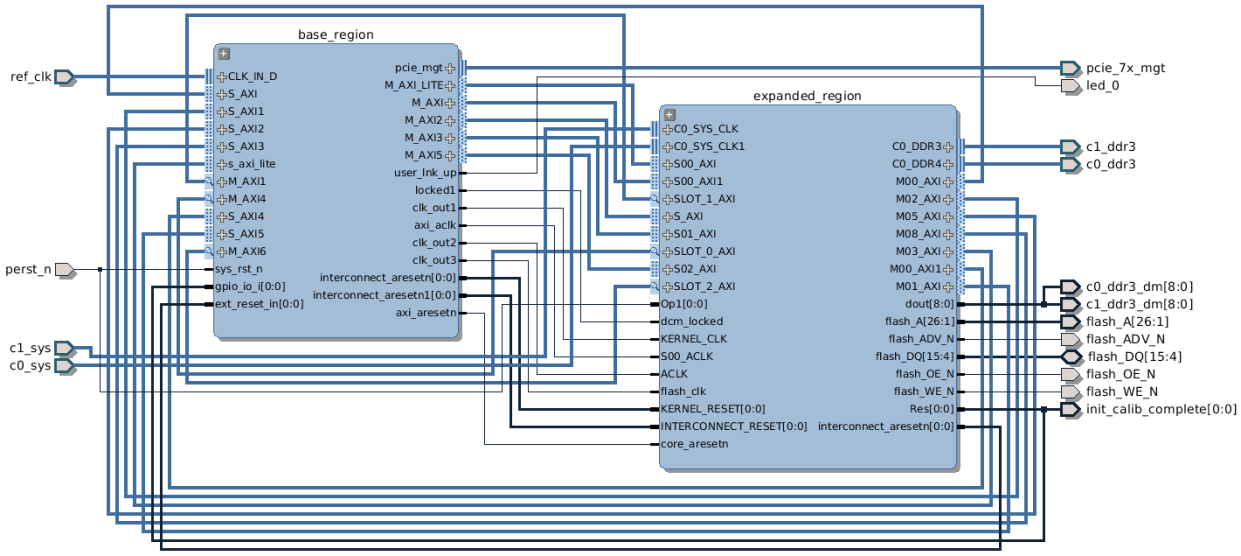

Figure: refdesign_xilinx_adm-pcie-ku3_2ddr_3_0 top level of hierarchy

The base_region level of hierarchy contains the following hierarchical cells and IP:

- base_clocking: contains clocking IP for the system and kernels
- pr_isolation_limited: contains IP related to partial reconfiguration of expanded_region/u_ocl_region
- featureid: contains IP used to represent the device's feature ID
- base_tieoffs: contains IP to tie off various inputs
- dma_pcie: an IP subsystem containing the PCI Express and XDMA IP cores

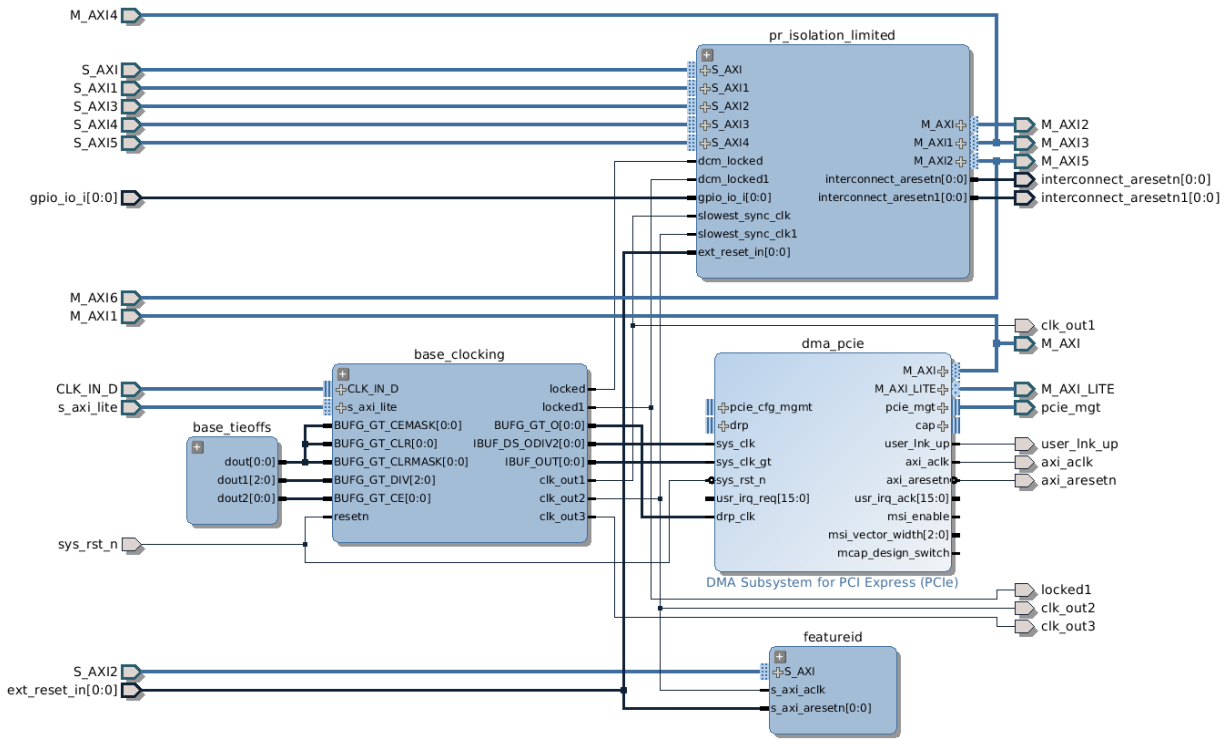

Figure: refdesign_xilinx_adm-pcie-ku3_2ddr_3_0 base_region level of hierarchy

The expanded_region level of hierarchy contains the following hierarchical cells and IP:

- apm_sys: contains IP used to implement the hardware necessary for system profiling
- expanded_resets: contains IP used to reset portions of the design
- memory: contains IP for DDR external memory control
- pr_support_limited: contains IP used to support partial reconfiguration and related functions
- interconnect_aximm: SmartConnect IP for AXI4-MM communications between host, kernels, and DDR memory
- interconnect_axilite: AXI interconnect IP for AXI4-Lite interface communication from host
- u_ocl_region: contains training kernel(s) and interconnect which is replaced using partial reconfiguration during the SDAccel compilation flow

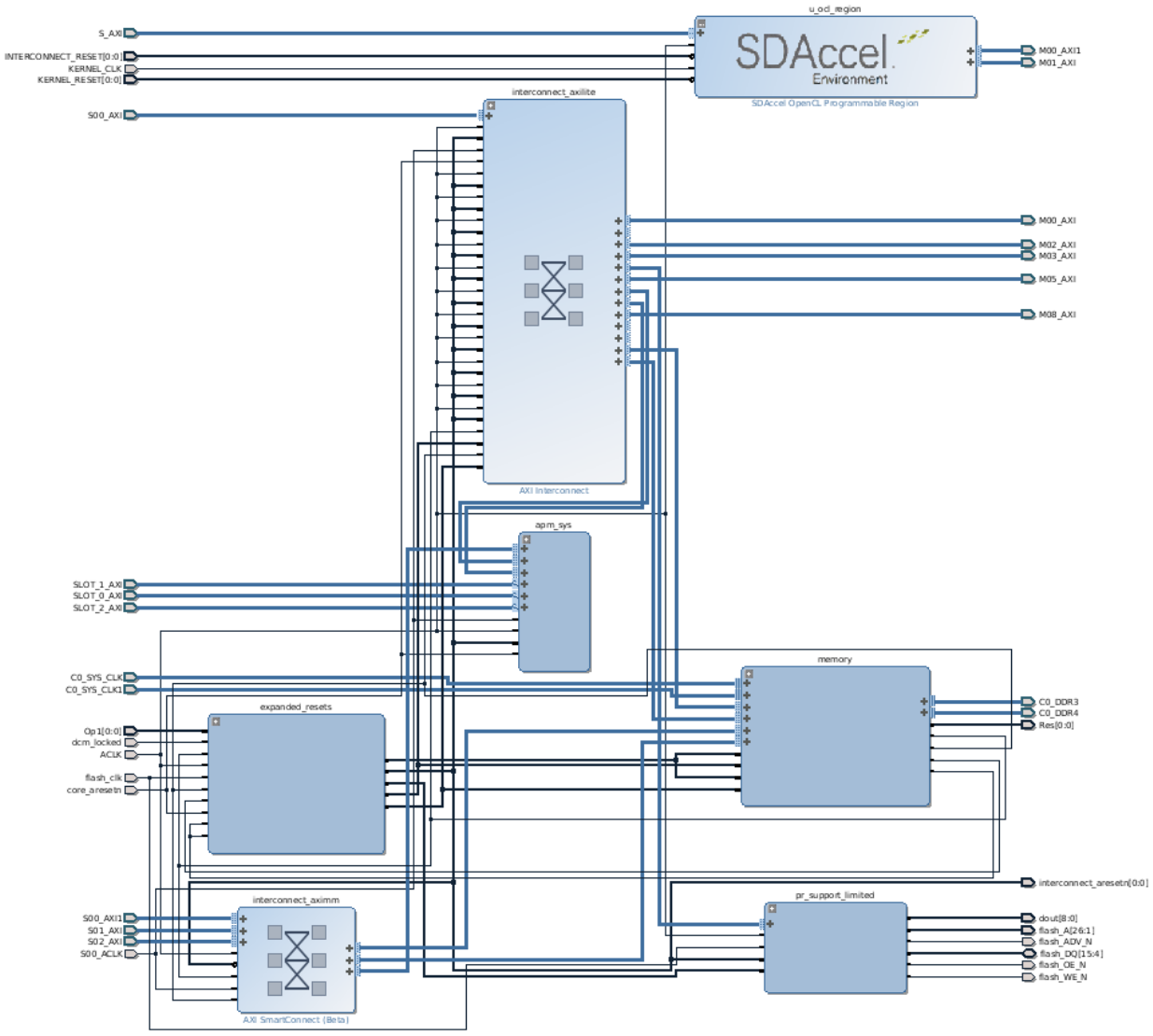

Figure: refdesign_xilinx_adm-pcie-ku3_2ddr_3_0 expanded_region level of hierarchy

Addresses

The address mapping for the refdesign_xilinx_adm-pcie-ku3_2ddr_3_0 project is as follows.

Cell	Slave Interface	Base Name	Offset Address	Range	High Address
base_region/dma_pcie					
M_AXI (64 address bits : 16E)					
expanded_region/apm_sys/xilmonitor_fifo0	S_AXI_FULL	Mem1	0x0000_0020_0000_0000	4G	0x0000_0020_FFFF_FFFF
expanded_region/memory/ddrmem	C0_DDR3_S_AXI	C0_DDR3_ADDRESS_BLOCK	0x0000_0000_0000_0000	8G	0x0000_0001_FFFF_FFFF
expanded_region/memory/ddrmem_2	C0_DDR3_S_AXI	C0_DDR3_ADDRESS_BLOCK	0x0000_0002_0000_0000	8G	0x0000_0003_FFFF_FFFF
M_AXI_LITE (32 address bits : 4G)					
base_region/pr_isolation_limited/gate_pr	S_AXI	Reg	0x0003_0000	4K	0x0003_0FFF
base_region/featureid/gpio_featureid	S_AXI	Reg	0x0003_1000	4K	0x0003_1FFF
base_region/pr_isolation_limited/ddr_calib_status	S_AXI	Reg	0x0003_2000	4K	0x0003_2FFF
expanded_region/apm_sys/xilmonitor_apm	S_AXI	Reg	0x0010_0000	64K	0x0010_FFFF
expanded_region/apm_sys/xilmonitor_fifo0	S_AXI	Mem0	0x0011_0000	4K	0x0011_0FFF
expanded_region/pr_support_limited/flash_programmer	S_AXI	reg0	0x0004_0000	64K	0x0004_FFFF
expanded_region/u_ocl_region	S_AXI	Reg0	0x0000_0000	64K	0x0000_FFFF
expanded_region/u_ocl_region	S_AXI	Reg1	0x0001_0000	64K	0x0001_FFFF
base_region/base_clocking/clkwiz_kernel	s_axi_lite	Reg	0x0005_0000	64K	0x0005_FFFF
expanded_region/memory/ddrmem	C0_DDR3_S_AXI_CTRL	C0_REG	0x0006_0000	64K	0x0006_FFFF
expanded_region/memory/ddrmem_2	C0_DDR3_S_AXI_CTRL	C0_REG	0x0007_0000	64K	0x0007_FFFF
expanded_region/u_ocl_region					
M_AXI (32 address bits : 4G)					
M00_AXI (38 address bits : 256G)					
expanded_region/memory/ddrmem	C0_DDR3_S_AXI	C0_DDR3_ADDRESS_BLOCK	0x00_0000_0000	8G	0x01_FFFF_FFFF
expanded_region/memory/ddrmem_2	C0_DDR3_S_AXI	C0_DDR3_ADDRESS_BLOCK	0x02_0000_0000	8G	0x03_FFFF_FFFF
Excluded Address Segments (1)					
expanded_region/apm_sys/xilmonitor_fifo0	S_AXI_FULL	Mem1	0x20_0000_0000	4G	0x20_FFFF_FFFF
M01_AXI (38 address bits : 256G)					
expanded_region/memory/ddrmem	C0_DDR3_S_AXI	C0_DDR3_ADDRESS_BLOCK	0x00_0000_0000	8G	0x01_FFFF_FFFF
expanded_region/memory/ddrmem_2	C0_DDR3_S_AXI	C0_DDR3_ADDRESS_BLOCK	0x02_0000_0000	8G	0x03_FFFF_FFFF
Excluded Address Segments (1)					
expanded_region/apm_sys/xilmonitor_fifo0	S_AXI_FULL	Mem1	0x20_0000_0000	4G	0x20_FFFF_FFFF