ACCRA TECHNICAL UNIVERSITY

FACULTY OF APPLIED SCIENCES

COMPUTER SCIENCE DEPARTMENT

Computer Organization and Architecture
BCP 203

COMPUTER FUNCTION AND INTERCONNECTION

Presentation Content

1. Computer Components and Functions
2. Interconnection Structures
3. Bus Interconnections
4. Point-to-point Interconnect
5. PCI Express

1. Computer Components

- Today's version of the stored-program machine architecture satisfies at least the following characteristics:

- Consists of three hardware systems: A central processing unit (CPU) with a control unit, an arithmetic logic unit (ALU), registers (small storage areas), and a program counter; a main memory system, which holds programs that control the computer's operation; and an I/O system.

- Has the capacity to carry out sequential instruction processing.

1. Computer Components

- Contains a single path, either physically or logically, between the main memory system and the control unit of the CPU, forcing alternation of instruction and execution cycles.

- This single path is often referred to as the von Neumann bottleneck.

- The Harvard architecture and the modified Harvard architecture addressed this bottleneck.

1. Computer Components

- A computer processes stuff in one of two ways:
  1. Arithmetic
  2. Logic
- A configuration of logic components could be *customized* to perform a computation.
  - Think of the process of connecting the various components into the desired configuration as programming.
  - The resulting program is a form of hardware; termed ***hardwired program***
- A *general-purpose* hardware with a segment that can accept a code and generate control signals makes programming easier.

1. Computer Components

- This method of programming using a sequence of codes or instructions is called ***software***
- A *means* of interaction with external environment is needed. Taken together these are known as ***I/O components***
- Operations on data may require access to more than one element at a time.
- A place to store temporarily both instructions and data is called ***memory*** or ***main memory***

1.1 Computer Components

- CPU uses two internal registers to exchange data with ***memory***
  1. **Memory Address Register** (MAR) – specifies address in memory for the next read or write
  2. **Memory Buffer Register** (MBR) – contains data to be written to memory or receives data read from memory
- An **I/O Address Register** (I/OAR) – specifies a particular I/O device
- An **I/O Buffer Register** (I/OBR) – used for exchange of data between an I/O module and the CPU

1.1 Computer Components

- A memory module consists of a set of locations, defined by sequentially numbered addresses

- Each location contains a binary number that can be interpreted as an instruction or data

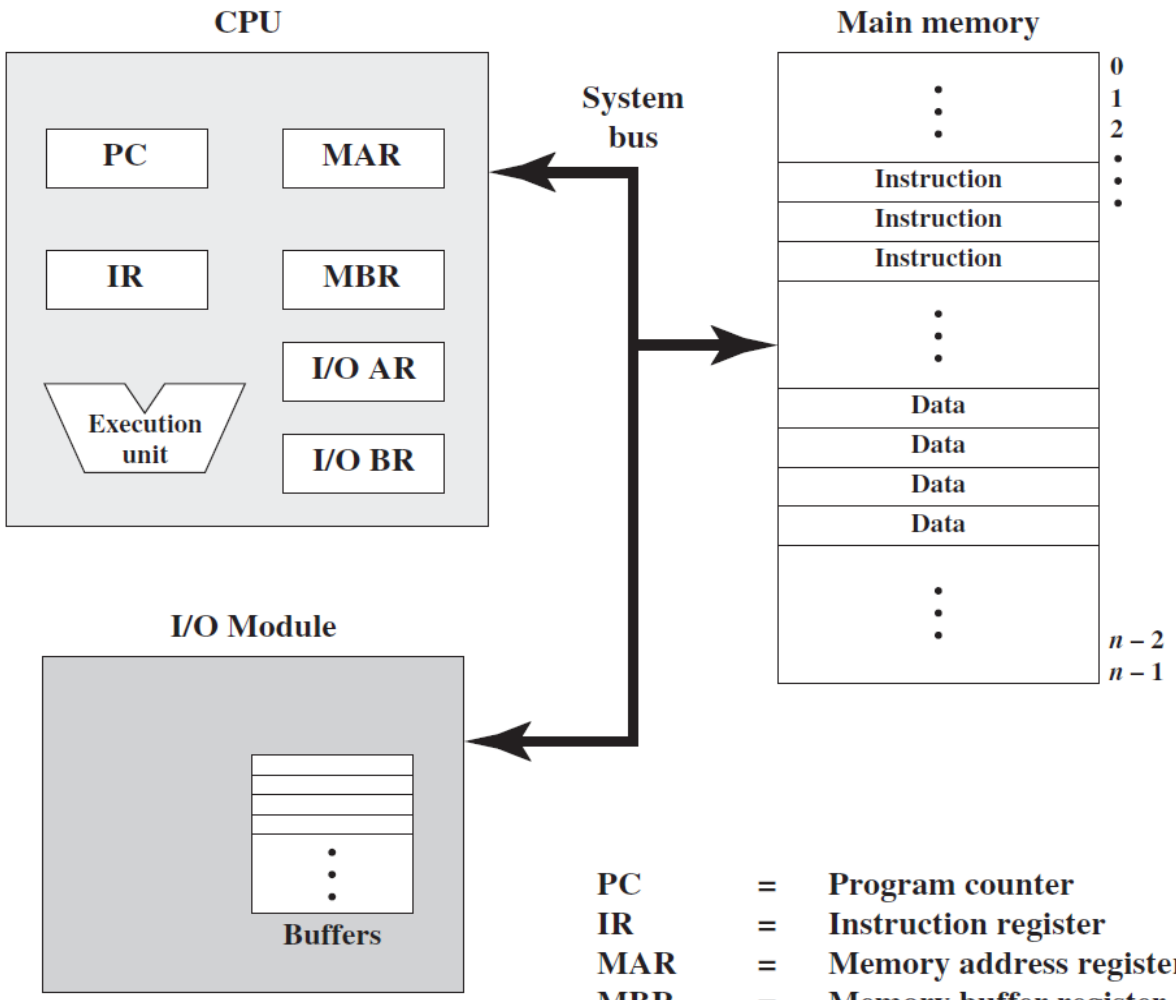
1.2 Computer Functions

- The basic function of the computer is the execution of a ***program*** *(a set of instructions stored in memory)* carried out in two steps:
  1. Fetch instructions from memory one at a time
  2. Execute each instruction
- The processing required for a single instruction is called the *instruction cycle*
- In a typical CPU a register called ***program counter*** (PC) holds the address of the next instruction to be fetched

1.2 Computer Functions

- The fetched instruction is loaded in a register in the CPU called ***instruction register*** (IR)
- Virtually all computers provide a mechanism by which other modules (I/O, memory) may interrupt the normal operation of the processor
- To accommodate interrupts, an *interrupt cycle* is added to the instruction cycle

1.2 Computer Functions



PC = Program counter
IR = Instruction register
MAR = Memory address register
MBR = Memory buffer register
I/O AR = Input/output address register
I/O BR = Input/output buffer register

2. Interconnection Structures

- In effect a computer is a network of basic modules and there must be ***paths*** for connecting these modules
- The collection of paths connecting these modules is called the ***interconnection structure***
- The interconnection structure must support the following types of transfers:
  1. Memory to processor
  2. Processor to memory
  3. I/O to processor
  4. Processor to I/O
  5. I/O to or from memory
- Over the years a number of interconnection structures have been tried

3. Bus Interconnections

- By far the most common is the ***bus*** and ***various multiple-bus structures***
- A bus is a communication pathway connecting two or more devices
- Typically, a bus consists of multiple communication pathways or lines; each line capable of transmitting signals representing a binary 1 or 0.
  - For example, an 8-bit unit of data can be transmitted over 8 bus lines
- A bus that connects major computer components (processor, memory, I/O) is called a ***system bus***
- The most common computer interconnection structures are based on one or more system buses

3. Bus Interconnections

- A typical system bus may consist of, from about 50 to hundreds of separate lines
- The system bus is actually a number of parallel electrical conductors
- In a classic bus arrangement, these conductors are metal lines etched in a card or board (printed circuit board)

3.1 Bus Structure

- Bus lines can be classified into three functional groups:
  1. Data lines
  2. Address lines
  3. Control lines
- Data lines provide a path for moving data among system modules and are collectively called ***data bus***
- ***Data bus*** may consist of 32, 64, 128 or even more data lines. Number of lines is referred to as the ***width*** of the bus
- ***Address lines*** are used to designate the source or destination of data-on-data bus.

3.1 Bus Structure

- The width of the address bus determines the maximum possible memory capacity of the system
- ***Control lines*** are used to control access to, and the use of data lines and address lines since data lines and address lines are shared by all components
- Control signals transmit *command* and *timing* information among system modules
- ***Timing signals***: indicate validity of data and address information
- ***Command signals***: specify operations to be performed

3.1 Elements of Bus Design

Type	**Bus Width**
Dedicated	Address
Multiplexed	Data
Method of Arbitration	**Data Transfer Type**
Centralized	Read
Distributed	Write
Timing	Read-modify-write
Synchronous	Read-after-write
Asynchronous	Block

4. Point-to-point Interconnect

- The connection between an I/O module and the computer system can be point-to-point or multi-point
- A point-to-point interface provides a dedicated line between I/O module and the external device
- On small systems (PCs, workstations) typical point-to-point links include those to the keyboard, printer and modem

5. PCI Express

- The Peripheral Component Interconnect bus is a popular high-bandwidth, processor independent bus that can function as a mezzanine or peripheral bus

- Intel began work on PCI in 1990 for Pentium based systems and released all patents to the public domain

- Because it is in the public domain products built by different vendors are compatible

5. PCI Express

- The PCI is designed to support a variety of microprocessor-based configurations: both single and multiprocessor systems

- It serves
  - ❑ Graphic display adapters
  - ❑ Network adapters
  - ❑ Disk controllers and so on