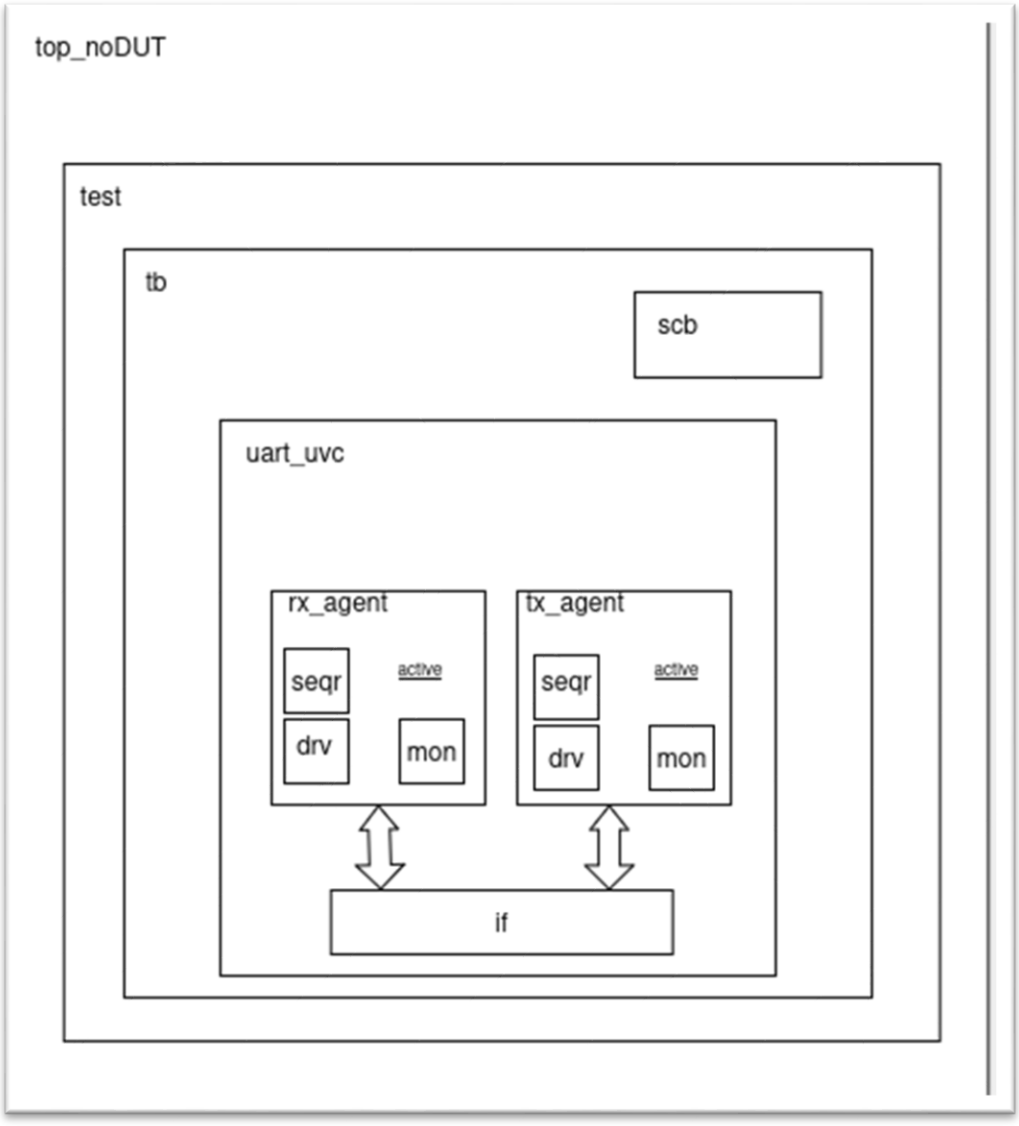
Verification Plan

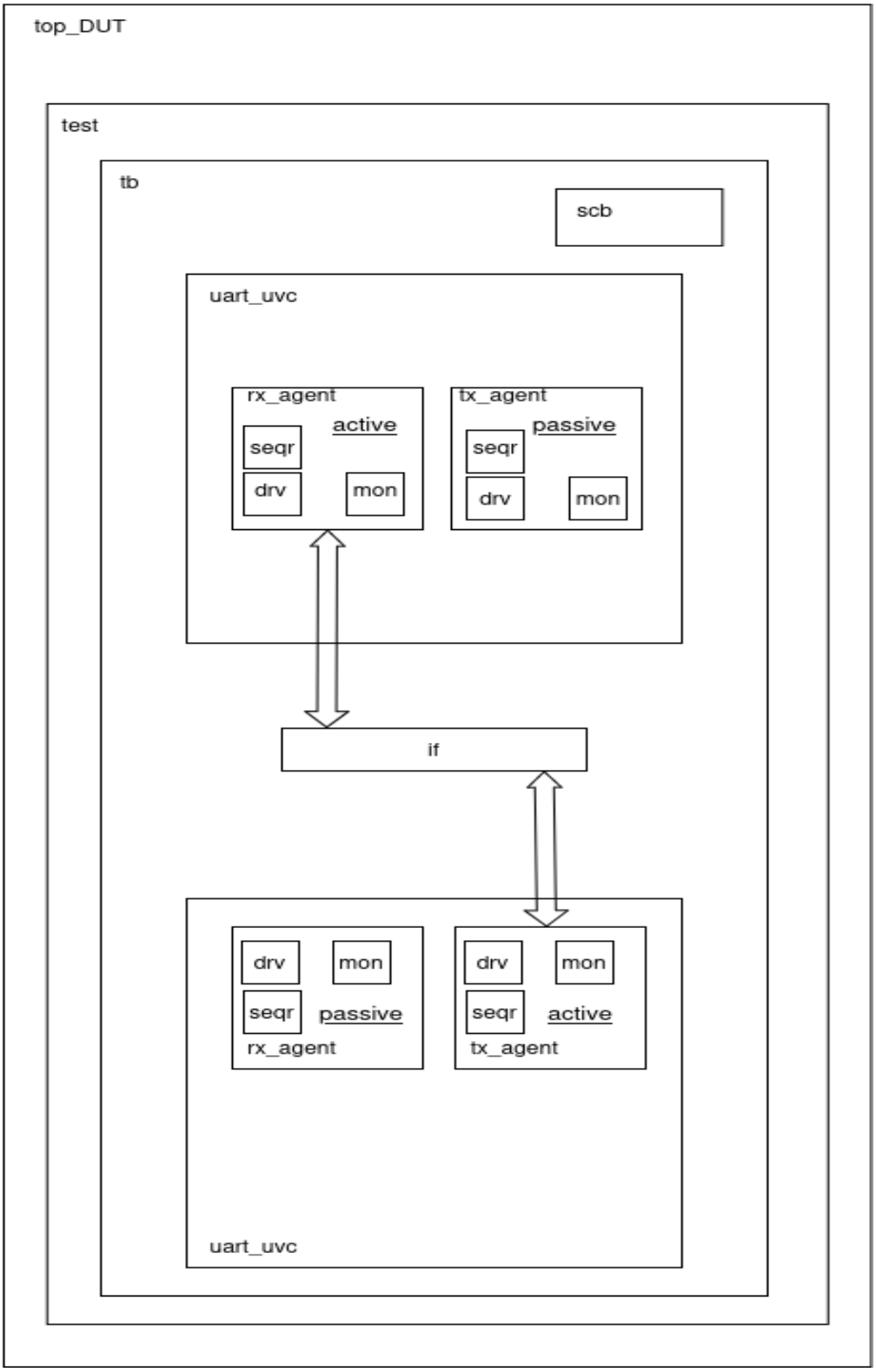
The goal of the UART verification plan is to make sure the UART works correctly. This includes checking that it follows the UART rules (like how data is sent and received), makes sure data is sent and received without mistakes, and works well with other parts of the system. We want to test everything, make sure it’s fast and reliable, and handle tough situations like errors or heavy us

Testbench Architecture:

Phase 1: UART UVC Without DUT



Phase 2: UART UVC With DUT



Verification Plane:

UVM_TEST=	Test case	Test Description	Test type
uart_base_test	Single 0xFF send	Send 0xFF from TX and verify reception via RX agent monitor.	Directed
uart_idle_test	Idle line check	Keep TX idle for a while, then send data (RX should not detect garbage).	Directed
uart_overflow_test	Overflow test	Send more than 8 bits to check RX buffer handling.	Directed
uart_parity_test	Parity test	Send correct & incorrect parity and check RX detection.	Directed
uart_dual_send_test	Send from both agents	TX and RX both send fixed values, and data is verified.	Directed
uart_rand_dual_send_test	Send both agents random	TX and RX both send random data, and RX verifies reception.	Randomized
uart_loopback_test	Loopback test	TX sends a fixed value, and RX must echo it back correctly.	Directed
uart_back_to_back_test	Back-to-back transmission	Send multiple bytes without gaps to check RX buffer stability.	Directed
uart_interrupt_test	Interrupt data	Send data mid-transmission to check RX behavior (overwrite/drop?).	Directed
uart_rand_test	Rand_test	All inputs (except clk) are randomized.	Randomized