A Tactile Sensor Interface Formed by Two TFTs and One Capacitor to Enable Dynamic and Static Force Sensing

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Abstract

In this article, we propose an interface circuit formed by thin film transistor(TFT) for tactile sensing applications. This interface circuit is composed of two TFTs and a capacitor, in connection with a polyvinylidenefluoride (PVDF) transducer for force sensing. An analytical model is presented to explain the working principle of the interface circuit, and an experimental study of a 10×10 tactile sensing array is built to evaluate the feasibility of the circuit. Our study shows such interface circuit is promising to obtain the dynamic and static force sensing.

Keywords

TFT; Tactile sensor; PVDF; Dynamic and static force sensing

1. Introduction

With the popularity of intelligent systems and human machine interfaces, flexible electronic products shows a promising market prospect[1].Tactile sensors are types of electronic devices that enables the friendly interaction between a machine and a human being or between machines. In wearable electronics, personal healthcare and edge computing, flexible tactile sensors are advantageous in terms of flexibility, weight and cost [3]. Therefore, most of the research attempt to improve the performance of the tactile sensor from the perspective of material and process. Deformable electrodes have been considered to achieve high sensitivity in force sensors, often on polymeric substrates incorporated with nanomaterials, ionic liquids, and conducting polymers[4-6]. Deformable structures are also implemented in pressure sensors using hollow and porous structures or arrays of micro sized structures, such as domes and pyramids[7-10].

However, a majority of these force sensors can only detect transient deformation because of the intermittence nature of piezoelectric and triboelectric effects. Although a few tactile sensors can detect both transient and static deformation[11-12]. Large-area integration of sensors and signal process electronics in a pixel array format remain challenging.

In order to tackle these challenges, a tactile sensor interface circuit that consists of two thin-film transistors (TFT) and one capacitor is proposed to enable both dynamic and static force sensing and in addition such an interface circuit array will address and read sensing signal sequentially. In this work, a piezoelectric sensor is used as a sensor or transducer. Due to the piezoelectric nature, it cannot sense static force signal being a great disadvantage. But the proposed interface circuit can provide a dynamic storage function to handle a quasi-static signal. To demonstrate its viability, a 10×10 pixelated polyvinylidenefluoride (PVDF) tactile sensor array is formed, as shown in Fig.1. Design of tactile sensors with ultra-sensitivity, rapid response speed, long-term stability, and low cost is a key factor to fulfill electronic skin applications.

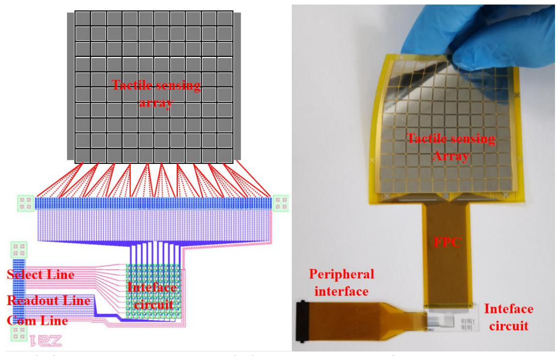


Fig. 1. (a) Layout design; (b) Prototype of a 10×10 tactile sensing array

2. Methods

A. Device Architecture and Fabrication

The tactile sensor interface circuit is in an array format where each pixel is composed of an auto-biased TFT for piezoelectric signal rectification, a switching TFT for row select, and a capacitor for charge storage as plotted in Figure 2. To receive the piezoelectric signal, a diode-connected TFT is used where its drain and gate are shorted, as such, the piezoelectric signal which is an AC voltage, is rectified to a half-wave DC voltage signal which is then sampled by a storage capacitor and a switching TFT. We name it a "2T1C" circuit.

Fig. 3 depicts the fabrication process of the interface circuit. Firstly, 200nm aluminum (Al) and 80 nm molybdenum (Mo) layer are sputtered on the glass substrate. After sputtering, the metal is further patterned by photolithography and wet etching, acted as the gate electrode of TFT and the storage capacitor bottom plate. Secondly, a 300 nm silicon nitride(SiNx) is deposited as bottom gate dielectric layer by chemical vapor deposition(CVD). Thirdly, a 150 nm hydrogenated amorphous silicon (a-Si:H) active layer and

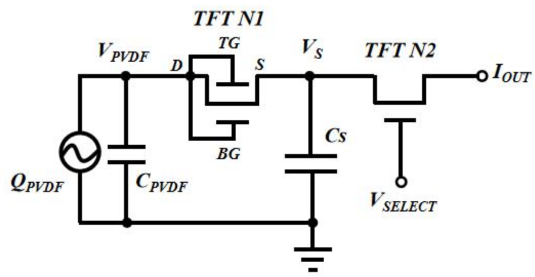


Fig. 2. 2T1C circuit diagram in each pixel of the interface circuit array

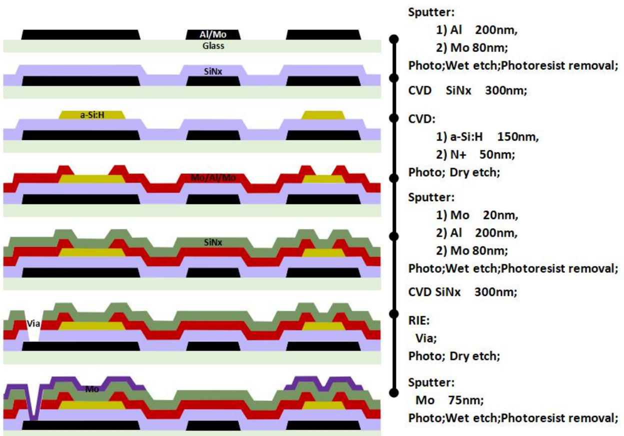


Fig.3. Process flow of interface circuit

50nm N+ a-Si:H are deposited by CVD at 300℃ consecutively. After that, the active layer is patterned by photolithography and dry etching. Fourthly, 20nm Mo, 200nm Al, and 80nm Mo are sequentially deposited and patterned as the drain or source electrode of TFT and store capacitor top plate. Fifthly, the top 300 nm SiNx dielectric layer is deposited. Sixthly, Via is created by selective dry etching. Lastly, a thickness of 75 nm Mo is sputtered.

The multilayered design layout and the corresponding fabrication process of tactile sensing array presented in Fig. 4. The 10×10 tactile sensor array includes Polyimide film(PI) with patterned copper electrode array, low temperature lamination anisotropic conductive Film (LTL ACF), PVDF film with patterned molybdenum electrode array, carbon conductive glue(CCG), aluminum coated (one side) polyimide film. Firstly, PVDF sheet (Measurement Specialties Inc. S06260-3 model)[13] chooses 110um thickness film with better pressure response, and uses metal mask to sputter 100nm molybdenum metal. Secondly, the PVDF film with the electrode pattern array and the PI film with patterned electrode array are aligned and laminated through LTL ACF (Teamchem Materials Company). The process conditions are vacuum degree 50 mTorr, pressure bonding temperature 90°C, 0.5 MPa, and duration 10 minutes. Finally, a carbon conductive adhesive (Nisshin-em Co. Ltd) was used to bond the other side of the PVDF film without patterned and Al film covered on the PI film.

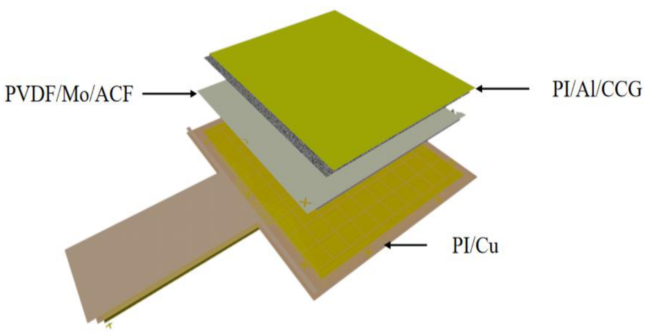


Fig.4. Schematic layout of Tactile sensing array

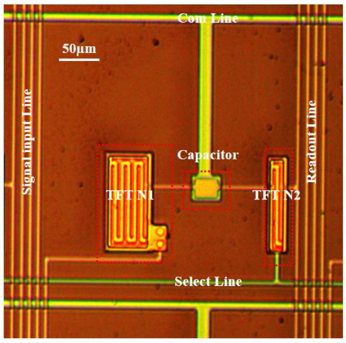


Fig.5. Microscopic image of the fabricated tactile sensing interface circuit, while TFT N1=516μm/3.2μm, TFT N2=102μm/3.2μm, and Cs=1.0pf

B. Device Modeling and Characterization

The principle of piezoelectric sensor is based on piezoelectric effects that electrical charges that occur in certain types of solid materials under pressure[14]. In a piezoelectric energy converter based on PVDF film, the piezoelectric layer works in a transfer mode and it is governed by the following equations written in the stress-charge format[15]:

$$Q_{PVDF} = d_{33} \cdot F_{33} + \frac{l}{t} d_{31} \cdot F_{31} \tag{1}$$

F is the applied force, l is the length and t is the thickness of PVDF film. The d31 and d33 is known as the transverse and longitudinal coefficient, respectively. Therefore, the piezoelectric effect means that the dipole forms a polarization when pressure is applied to the materials, and this polarization is proportional to the applied pressure.

Upon the applied force, the gate bias will be a function of piezoelectric-generated charges(Q_{PVDF}) from the PVDF film and the total capacitance C_{TOTAL}. And the top gate and bottom gate electrode connected to the drain electron of TFT N1, then the change generated by the PVDF film is shared with the drain electrode.

$$V_{PVDF} = V_{TG} = V_{BG} = \frac{Q_{PVDF}}{C_{TOTAL}} = \frac{d_{33} \cdot F_{33} + \frac{l}{t} d_{31} \cdot F_{31}}{C_{PVDF} + C_{TOP} + C_{BOTTOM} + C_{CHANNEL}} \tag{2}$$

C_{PVDF} is the equivalent capacitance of PVDF film. C_{CHNNEL} is the channel capacitance, C_{TOP} and C_{BOTTOM} is the capacitance of the top and bottom capacitance of the dual-gate TFT. Since the force is weak, the gate bias voltage smaller than the subthreshold voltage but greater than zero. Hence, the device works in the deep sub-threshold regime and the output current is given as below[16]:

$$I_{DS} = I_{D0} \exp\left(\frac{q[(1+\gamma)V_{TG} - V_{TH}]}{\beta \cdot kT}\right) \times \left[1 - \exp\left(\frac{-q \cdot (V_{PVDF} - V_S)}{kT}\right)\right] \tag{3}$$

The current of the storage capacitor is related to time and can be obtained :

$$C_S \cdot \frac{dV_S}{dt} = I_{DS} \tag{4}$$

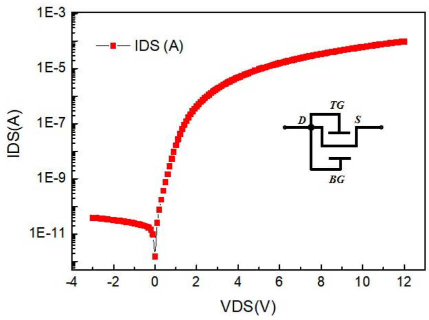


Fig.6. Current variation under small bias voltages of dual-gate a-Si:H TFT N1

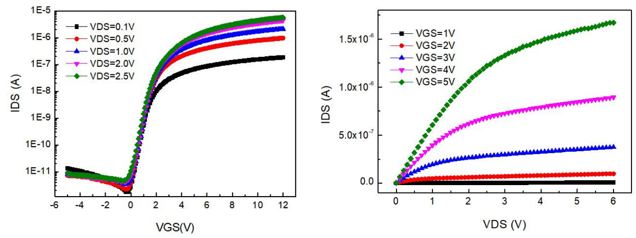


Fig.7. Characterization of results for single gate a-Si:H TFT N2 (a) Transfer characteristics; (b)Output characteristics

Where I_{D0} is the output current when $V_{BG}=V_{TH1}$ and $(V_{PVDF}-V_S)$<<-kT/q. Here, q is the electron charge, k is the Boltzmann's constant, T is the absolute temperature in Kelvin, S is the sub-threshold swing, and β is related to S, $\beta = q \cdot S / [(\ln 10) \cdot kT]$. When the force is applied, the generated bias voltages(V_{PVDF}) is less than hundreds of millivolts, thus the $[1-\exp\frac{-q(V_{PVDF}-V_S)}{kT}]$ term is approximately equal to unity. Additionally, the PVDF mainly generates the transversal stress, hence making piezoelectic charges in the d31 direction negligible. Accordingly, the voltage of store capacitor can be further simplified as:

$$V_S = \frac{I_{D0}}{C_S} \exp\left(\frac{q[(1+\gamma)(\frac{d_{33} \cdot F_{33}}{C_{PVDF}+C_{TOP}+C_{BOTTOM}+C_{CHANNEL}}) - V_{TH1}]}{\beta \cdot kT}\right) \cdot t \tag{5}$$

When t is closely related to the time constant. Elimination of τ gives $\tau = R_T C_S$. The theoretical relationship between R_T, the total channel resistance(R_{ch}), the total contact resistance(R_{SD}), and the total resistance of capacitor(R_{cap}) is given by

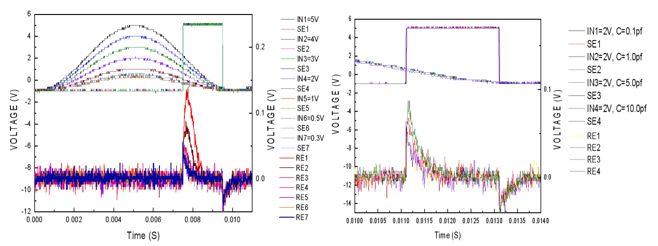
$$R_T = R_{ch} + R_{SD} + R_{cap} \tag{6}$$

When the select line is in the ON state, $V_{SELECT}>V_{TH2}$, the TFT N2 in the saturation region, and the output current I_{OUT} can be written as [17]:

$$I_{OUT} = \mu C_G \frac{W}{L}(V_G - V_{TH2})^2 \tag{7}$$

μ the effective field effect mobility, W and L are the effective channel width and length, respectively. C_G is the gate dielectric capacitance per unit area, V_{TH2} is the threshold voltage of TFT N2.

Hence, as seen from theoretical analysis, the tactile signal is related to the design of the double-gate TFT N1, signal gate TFT N2 and the storage capacitor C_S. The interface circuit needs a compromise design, between acquisition speed and signal sensitivity.



(a) (b)

Fig.8. "2T1C" pixel circuit signal analysis (IN/SE signal uses the left coordinate, RE signal uses the right coordinate)

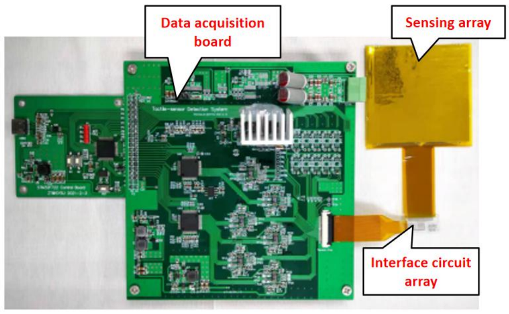


Fig.9. Data acquisition system to evaluate 10×10 tactile sensor array

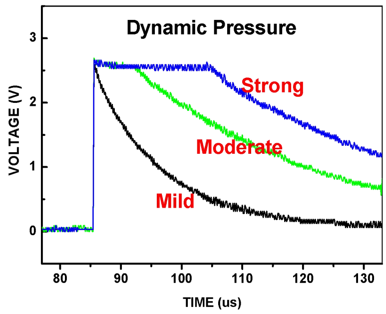


Fig. 10. Response signal both dynamic and static forces.

3. Results and Discussion

We have designed and fabricated a highly sensitive 10×10 tactile sensor array, which includes a PVDF tactile sensor array on a PI substrate and a "2T1C" sensor interface circuit array based on a-Si TFT glass substrate. The fabricated interface circuit is shown in Figure 5. Each pixel of 10×10 tactile sensor array including rectifying TFT, storage capacitor, switching TFT, as well as signal input lines, select lines, readout lines and common lines. Figure 6 shows the IV characteristic curve of a diode-connected dual-gate TFT N1(W=516μm, L=3.2μm). When a slight force applied at PVDF film, TFT N1 obtain a weak bias voltage, larger Ids current can be generated, because of a large transconductance in the subthreshold region (gm≈1.4×10^{-9} Simens). Figure 7 shows the transfer and output characteristics of a single-gate TFT N2 (W=100μm, L=3.2μm) as a switch.

In addition, the storage capacitance also affects the collection of tactile signals. Through theoretical analysis, the larger the storage capacitor value, the more charges that can be stored, but if the capacitor value is too large, the conversion gain is low leading to a very low voltage which is not resolved by the peripheral electronics. On the other hand, the charge injection from the switching TFT causes an undesirable drop in the signal voltage stored on the Cs when the switching TFT is turned off, and the leakage also makes the charge on the Cs gradually leak out over the frame time [18]. Thus, there are optimal design values for the storage capacitor in the interface circuit.

Figure 8 is the experimental result of the interface circuit, include TFT N_1, TFT N_2, and Cs. When the input signal(INn) is a sine signal(0~5V,1Hz), the switch selection signal(SEn) is a square wave signal(0-5V,10Hz), we can found that the larger the storage capacitance and the force sensing signal, the higher the readout signal (Fig.8 (a) and (b)). In addition, the charge injection effect has great impact on readout-circuit, resulting in sharp pulses.

In order to evaluate the feasibility of the interface circuit, a data acquisition system was built to collect and visualize the tactile signals, as shown in Figure 9. The dynamic force signal can be distinguished in one pixel observing the output pulse voltage values and the static force can be correlated with the relaxation time. When the tactile sensor array detects the dynamic pressure, the output amplified voltage will be higher as the force increases, and then it will return to the stress-free state, as shown in Fig.10.

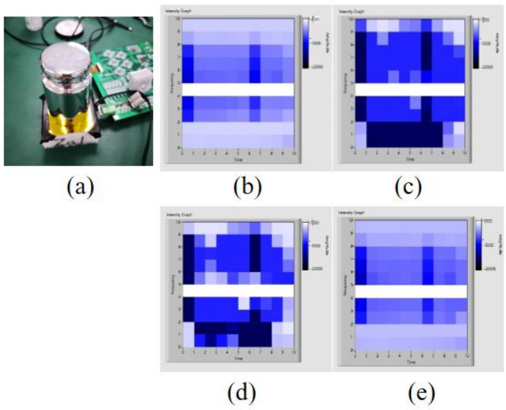


Fig.11. (a) The experimental design where an object is placed at the sensor array, (b)–(e) are the force mapping of the whole sensor array at four different time periods of 0s, 0.53s, 0.80s, and 5.40s.

Compared with the traditional PVDF system directly connected to the external electronics. the interface circuit can monitor the release time of force and initially sense the pressure because of storage-readout circuit. When mild, moderate and strong force are separately applied to the PVDF, the release time is 0.53s, 1.36s and 1.93s, respectively as shown in Fig.10. Fig. 11 presents the temporal response of the array upon a static load. Due to the storage function of the interface circuit, the storage capacitor in each pixel is charged and discharged over time which can be visualized by the array.

4. Conclusion

A "2T1C" sensor interface circuit is used to integrate with the PVDF transducer to form a tactile sensor. The 10 by 10 tactile sensor array has demonstrated its capability to detect and visualize both dynamic and static forces.

Acknowledgment

The authors would like to thank the staff of the State Key Laboratory of Optoelectronic Materials and Technologies of Sun Yat-Sen University, for their help on device fabrication. This work was funded by National Key R&D Program of China (2019YFA0706100).

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