B5-X300 Quickstart Guide

This quickstart guide takes you through the steps for creating and compiling a new project with the Xilinx ISE WebPACK 7.1i design software.

1. Install the ISE WebPACK Software.

Either download ISE WebPACK from the Xilinx website, or obtain an ISE WebPACK CD from your local Xilinx distributor or directly from Xilinx.

This tutorial gives installation instructions on how to download and install the WebPACK software from the Xilinx website (current version at time of updating this document is 4.2WP3.0).

Using your web browser, go to http://www.xilinx.com
Click on the Download link at the top of the page.
Click on the Free ISE WebPACK 7.1i link.

If you have not yet registered with Xilinx, click on the Order & Register button. If you are registered, click on the Download button and log in.

Use the Xilinx WebInstall program to download the WebPACK software as follows:
Right click on "Microsoft Windows XP/2000" and save the WebPACK_71i_installer.exe file to your hard disk drive.
In windows explorer, double click on the installer executable that you have just downloaded. This starts the installer program.
Tick the "Accept" box and click Next.
Click "Accept" and Next three times to accept the terms of the software licenses.
Click Next, Next, Next, Next, Next, Install.
The install progress bar will appear while the install program downloadsand installs all of the modules. This can take a long time, and may be an "overnight" task for machines with a slow internet connection.
The "Setup Complete" dialog box will pop up. It asks if you would like to chck for software updates. Click Yes.
Another dialog box will then pop up with the message "Install has completed". Click OK.

You will now have two new icons on your desktop "Xilinx ISE 7.1i" and "Xilinx MySupport".

At this stage we recommend that you restart your computer.

Listing 1: FLASHe.vhd VHDL Code

```
Library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity FLASHe is
   Port (
      Clk : in STD_LOGIC;
      Rst_n : in STD_LOGIC;
      LED : out STD_LOGIC
   );
end FLASHe;

architecture RTL of FLASHe is
signal FlashCount : STD_LOGIC_VECTOR(23 downto 0);
signal Rst : STD_LOGIC;
begin
   Rst <= not Rst_n;
   process (Clk)
   begin
      if (Rst = '1') then
         FlashCount <= (others => '0');
      elsif (Clk'event and Clk='1') then
         FlashCount <= FlashCount + 1;
      end if;
   end process;
   LED <= std_logic(FlashCount(23));
end RTL;
```

2. Create a new project.

Start Xilinx ISE 7.1i by double clicking on the desktop icon.

Do:
File
New Project

Enter a Name & Location for the project:
FLASHe
C:\Projects\FLASHe

Select the top-level module:
HDL

Click Next

Select the device & design flow:
Device family = Spartan2E
Device = xc2s300e
Package = pq208
Speed Grade = -6

Other values are:
HDL
XST (VHDL/Verilog)
Modelsim
VHDL

Click Next

Skip the Create New Source dialog box by clicking Next (we will add the source file to the project after project creation).

Click Next.

Click Finish.

Do:
Project
New Source…
VHDL Module
File Name = FLASHe

Click Next.

Fill in:
Architecture Name = RTL
(RTL stands for Register Transfer Level)

Fill in the table with
CLK in
Rst_n in
LED out

Click, next, finish

A window will pop up with the start of the new FLASHe.vhd code. Modify it so that it looks like the code in Listing 1.

Do:
File
Save

3. Assign the pinouts of the device.

You will now need to tell the compiler which pins you want associated with which signals in your design. The compiler reads the UCF (user constraints file) file to get this information. You can use the Assign Package Pins process to enter the information that is written to the UCF file. In the following procedure, you will write the pinout / location information into the UCF file, using the Assign Package Pins process.

Single click on the FLASHe.vhd item in the "Sources in Project" box, on the top left of the design environment.

The "Processes for Source" box on the bottom left of your design environment now contains all of the processes that can operate on this design. Expand out the User Constraints processes so that you can see the Assign Package Pins process.

Double click on the Assign Package Pins process.

The compiler will run, and the Xilinx PACE tool window will then open.

In the Design Object List – I/O Pins window, click in the Loc fields, and fill them in with the following pad numbers:

Clk	P77
LED	P82
Rst_n	P57

Do:
File
Save

The Bus Delimiter dialog box will pop up.

Select:
XST Default <>

Click OK.

Close the Xilinx PACE program.

You can now have a look at your new UCF file by double clicking on the Edit Constraints (Text) process. Have a look at the UCF file, and then close this window.

Single click on the "flashe-rtl (FLASHe.vhd)" source in the "Sources in Project" window, to make sure that this source is selected.

Double click on the Implement Design process. You should get green-ticks on all of the Translate, Map and Place & Route process items, as these processes complete.

You may get a yellow exclamation mark on some processes. This is OK. It just means that a warning has been generated in a process. Warnings are not necessarily design errors. You can view the warnings in the transcript window (do View, then tick Transcript).

Your design has now been implemented. All that remains is the creation of the programming file for downloading, and the hardware configuration.

4. Create the programming file.

Right click on the Generate Programming File process, and select Properties…

Click on the Startup Options tab.

Set:
Start-Up Clock = JTAG Clock

Click OK.

Double click on the Generate Programming File process. When the process completes, you will get a green-tick.

5. Configure the FPGA.

Connect the download pod board to the parallel port of the PC using the parallel port flat-cable.

Connect the 10 way flat-cable on the download pod board to the JTAG MODE header (J12) on the B5-X300 board.

Ensure that header M1 on the CONFIG MODE SEL header block, located in the corner of the B5-X300 board near slots B and C, is shorted with a header shunt. This sets the FPGA configuration mode to JTAG.

Check that your regulated DC power supply is +5V, before you connect it to your B5-X300 board. Connect the supply to your board.

Ensure that the red LED on the download pod board, labelled "LOCKED", is off. The toggle switch on the download pod board controls the lock / unlock function. When the system is unlocked, the FPGA can be configured through the cable.

Double click on the Configure Device (iMPACT) process. This will start the iMPACT device configuration tool.

In the Configure Devices Dialog box select:
Boundary-Scan Mode

Click Next.

Select:
Automatically connect to the cable…

Click Finish.

You will see a message that one device has been detected. Click OK.

Select the file:
flashe.bit

A dialog box with the following message will pop up:
"A BIT file describing an xc2s300e is about to be assigned to a device previously identified as an xcv300e. Are you sure you want to do this?"

Click Yes.
The reason for this message is that the ID code for the xcv300e device is the same as for the xc2s300e device.

Right click on the Xilinx FPGA icon, and select Program…

A dialog box will pop up. Make sure that the Verify checkbox is unticked. Click OK.

A progress bar indicator will pop up, which shows the progress of the download of the FPGA configuration bitstream. When finished, you will get a "Programming Succeeded" message, and the LED on your B5-X300 board will be flashing at a rate of about 2.9Hz (the factory setting of the header programmable oscillator is 48MHz). If you hold down the reset switch on the board, the flashing will stop. If you release the reset switch, the LED will flash.

That completes the quickstart exercise. If you wish, try modifying the code to flash the LED at a faster rate, and running through the procedure again. You will then be ready to try your own designs, or move onto one of the more advanced tutorials. There are links to resources on the BurchED website at http://www.BurchED.com.au/resources.html , which you can use as references for designing your own projects.

6. Support.

Please email Tony Burch, tony@BurchED.com.au, with any questions, comments, feedback or requests for support.

Thanks for purchasing the B5-X300 board. We hope you will get much enjoyment from using it. **J**