B5-Spartan2+ Quickstart Guide

This quickstart guide takes you through the steps for creating and compiling a new project with the Xilinx ISE WebPACK Design software.

1. Install the ISE WebPACK Software

Either download ISE WebPACK from the Xilinx website, or obtain an ISE WebPACK CD from your local Xilinx distributor (or directly from Xilinx).

This tutorial gives installation instructions on how to download and install the WebPACK software from the Xilinx website (current version at time of updating this document is 4.1WP3.0).

Using your web browser, go to
http://www.xilinx.com
Click on
Products,
Design Tools Center,
Free ISE WebPACK (on the left).

If you have not yet registered with Xilinx, click on the Register for ISE WebPACK button. If you are registered, click on the Download ISE WebPACK button and log in.

Click on
Design Configurations
FPGA Design
Select Configuration

In the Your Download box (bottom right of the screen), click
Install Type = Custom

This will expand out the list of tools that you wish to download. For getting started, we recommend only the following minimum toolset. In the Design Modules column, make sure that only the following are ticked:
Design Entry
Spartan Fitter
FPGA Prog.

In the Optional Tools column, make sure that none of the items are ticked.

Click the Download button (the very bottom right of the screen).

A new window will pop up with a list of files. Download all of these files to a folder on your machine. The files are large. Depending on the speed of your internet connection, it may be an 'overnight' download.

Double click on the installer executable, that you have just downloaded. This starts the WebPACK InsallShield Wizard.

Click next, yes, next, next, next. InstallShield will install WebPACK on your machine. Click next, finish, and then restart your computer.

You will now have three new icons on your desktop
WebPACK Project Navigator
Device Programming
PROM File Formatter.

Listing 1: FLASH.vhd VHDL Code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity LEDFLASH is
    Port ( CLK : in std_logic;
           LED : out std_logic);
end LEDFLASH;
architecture behavioral of LEDFLASH is
signal countL : std_logic_vector(23 downto 0);
begin
  increment: process (CLK) begin
    if(clk'event and clk = '1') then
      countL <= countL + 1;
    end if;
  end process;
  LED <= std_logic(countL(23));
end behavioral;
```

2. Create a new project

Start:
WebPACK Project Navigator

Type in a new Project name:
FLASH

Select a folder for your project eg. c:\mywebpack\FLASH
(you will need to create this new folder with Windows Explorer ie. outside the WebPACK environment).

Device Family = Spartan2
Device = 2s200-5pq208
Design Flow = XST VHDL
OK

Do:
Project
New Source…
VHDL Module
File Name = FLASH

Fill in:
Architecture Name = RTL
(RTL stands for Register Transfer Level)

Fill in the table with
CLK in
LED out

Click, next, finish

A window will pop up with the start of the new FLASH.vhd code. Modify it so that it looks like the code in Listing 1.

Do:
File
Save

3. Assign the pinouts of the device

You will now need to tell the compiler which pins you want associated with which signals in your design. The compiler reads the UCF (user constraints file) file to get this information. You can use the Constraints Editor process to enter the information that is written to the UCF file. In the following procedure, you will write the pinout / location information into the UCF file, using the Constraints Editor Process.

Single click on the FLASH.vhd item in the "Sources in Project" box, on the top left of the design environment.

The "Processes for Current Source" box on the bottom left of your design environment now contains all of the processes that can operate on this design. Expand out the processes so that you can see the Edit Implementation Constraints (Constraints Editor) process.

Double click on the Edit Implementation Constraints (Constraints Editor) process.

The compiler will run, and the Constraints Editor window will then open.

Click on the Ports tab, located towards the bottom of the window.

Fill in the Location fields with the following

clk	P77
led	P82

Do:
File
Save

A dialog box with a message about TRANSLATE will then pop up. Click OK.

Do:
File
Exit

A dialog box with a message about the UCF file will pop up.
Click Reset.

You can now have a look at your new UCF file by double clicking on the Edit Implementation Constraints File process. Have a look at the UCF file, and then close this window.

Double click on the Implement Design process. You should get green-ticks on all of the Translate, Map and Place-and-Route process items, as these processes complete.

You may get a yellow exclamation mark on some processes. This is OK. It just means that a warning has been generated in a process. Warnings are not necessarily design errors. You can view the warnings in the transcript window (do View, then tick Transcript).

Your design has now been implemented. All that remains is the creation of the programming file for downloading, and the hardware configuration.

4. Create the programming file

Right click on the Create Programming File process item and select Properties.

Click on the Startup Options tab.

Set:
Start-Up Clock = CCLK

Click OK.

Double click on the Create Programming File process. When the process completes, you will get a green tick.

5. Configure the device

Connect the download pod board to the parallel port of the PC using the parallel port flat-cable.

Connect the 10 way flat-cable on the download pod board to the SERIAL MODE header (J7) on the B5-Spartan2+ board.

Make sure that your regulated DC power supply is +5V before you connect it to your B5-Spartan2+ board.

Connect the power supply to the B5-Spartan2+ board.

Right click on the Configure Device (iMPACT) process, and select Properties…

Set:
Port to be used = Auto
Baud rate = Auto
Configuration Mode = Slave Serial
Type of Configuration File =
Bitstream File (*.bit)

In the
Configuration Filename =
field, click on the dot-dot-dot button and select the file
flashe.bit

Click OK to exit the Process Properties dialog box.

Double click on the Configure Device (iMPACT) process. This will start the iMPACT device configuration tool.

Right click on the Xilinx FPGA icon and select Program…

Your device will take several seconds to configure. You will then get a 'Programming Succeeded' message, and the LED on your B5-Spartan2+ board will be flashing at a rate of about 2.9Hz (the factory setting of the header programmable oscillator is 48MHz).

6. Support

Please email Tony Burch, tony@BurchED.com.au, with any questions, comments, feedback or requests for support.

Thanks for purchasing the B5-Spartan2+ board. We hope you will get much enjoyment from using it ☺