B3-SPARTAN2+ Quickstart Guide 1.0

This quickstart guide takes you through the steps for creating and compiling a new project with the Xilinx WebPACK ISE Design software.

1. Install the WebPACK ISE Software

Put your WebPACK ISE CD into your CDROM Drive.
Using Windows Explorer, go to that drive and double click on readme_install.html
Click on each of the install module names, in turn, for FPGA Install (run the install modules from the disc).

The minimum that you will need for this jumpstart is the following group of modules:
webpack_design_entry
webpack_spartan2

Once you have installed these, and rebooted your machine, you will have a WebPACK Project Navigator icon on your desktop.

2. Create a new project

Start:
WebPACK Project Navigator

Do:
File
New Project

Type in a new Project name:
LEDFLASH

Select a folder for your project eg. c:\mywebpack\ledflash
(you will need to create this new folder with Windows Explorer ie. outside the WebPACK environment).

Device Family = Spartan2
Device = 2S200 PQ208-5
Synthesis tool = XST VHDL
OK

Do:
Project
New Source…
VHDL Module
File Name = LEDFLASH

Fill in the table with
CLK in
LED out

Next>
Finish

A window will pop up with the start of the new LEDFLASH.vhd code. Modify it so that it looks like the code in Listing 1.

Listing 1: LEDFLASH VHDL Code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity LEDFLASH is
    Port ( CLK : in std_logic;
           LED : out std_logic);
end LEDFLASH;
architecture behavioral of LEDFLASH is
signal countL : std_logic_vector(23 downto 0);
begin
      increment: process (CLK) begin
            if(clk'event and clk = '1') then
                  countL <= countL + 1;
            end if;
      end process;
      LED <= std_logic(countL(23));
end behavioral;
```

Do:
File
Save

3. Assign the pinouts of the device

You will now need to tell the compiler which pins you want associated with which signals in your design. The compiler reads the UCF (user contraints file) file to get this information. You can use the Constraints Editor process to enter the information that is written to the UCF file. In the following procedure, you will write the pinout / location information into the UCF file, using the Constraints Editor Process.

Single click on the LEDFLASH.vhd item in the "Sources in Project" box, on the top left of the design environment.

The "Processes for Current Source" box on the bottom left of your design environment now contains all of the processes that can operate on this design. Expand out the processes so that you can see the Constraints Editor process.

Double click on the Constraints Editor process.

The compiler will run, and the Constraints Editor window will then open.

Click on the Ports tab, located towards the bottom of the window.

Fill in the Location fileds with the following
clk P77
led P49

Do:
File
Save

A dialog box with a message about TRANSLATE will then pop up.
Click OK.

Do:
File
Exit

A dialog box with a message about the UCF file will pop up.
Click Reset.

You can now have a look at your new UCF file by double clicking on the Edit UCF file process. Have a look at the UCF file, and then close this window.

Double click on the Implement Design process. You should get green-ticks on all of the Translate, Map and Place-and-Route process items, as these processes complete.

Your design has now been implemented. All that remains is the creation of the bitfile for downloading, and the downloading process itself.

4. Create the bitfile (.rbt) for downloading

Right click on the Create Programming File process item and select Properties…

Make sure the Create ASCII Configuration File checkbox is checked (this tells the bitstream creator program to write out the .rbt rawbit file, which the BEDLOAD utility reads for downloading).

Click OK.

Double click on the Create Programming File process. A .rbt file is written out to your design folder.

5. Download the .rbt file to your FPGA

Connect the download pod board to the parallel port of the PC using the parallel port flat-cable.

Connect the BED-SPARTAN2+ board to the download pod board using the 10-way flat-cable.

Make sure that your regulated DC power supply is +5V before you connect it to your BED-SPARTAN2+ board.

Connect the power supply to the BED-SPARTAN2+ board.

Run the BEDLOAD utility (free to download from the Free Downloads section of the Burch Electronic Designs website). Note that you will need to download and install port95nt.exe beforehand, if you are using Windows NT or Windows 2000.

Do:
File
Load
and select your .rbt file (eg. LEDFLASH.rbt).

If you need to, you can change the parallel port base address as appropriate for your machine.

Click on the big Download button.

Click OK to proceed with the download.

The bitstream download can take up to 30 seconds. If download is successful, a "success" dialog box will pop up. At this point, your FPGA circuit should be functioning. If you have downloaded the LEDFLASH.rbt example file, the LED on your BED-SPARTAN2+ board will be flashing at a rate of about 1.4Hz.

6. Support

Please email Tony Burch, tony@BurchED.com.au, with any questions, comments, feedback or requests for support.