B5-X300 Quickstart Guide

This quickstart guide takes you through the steps for creating and compiling a new project with the Xilinx ISE WebPACK 8.1i design software.

1. Download & Install the ISE WebPACK Software.

You can either download the ISE WebPACK from the Xilinx website, or you can obtain an ISE WebPACK CD from Xilinx or from your local Xilinx distributor.

Following are instructions on how to download and install the WebPACK software from the Xilinx website

Using your web browser, go to http://www.xilinx.com

Click on the ISE WebPACK™ (FREE download) link, which is on the left, underneath **Design Tools »**

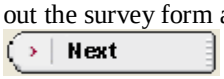
On the right of the page, click on the Download Free link.

If you have not yet created an account with Xilinx, click on

Then follow the steps to create an account and obtain a User ID and Password.

Once you have an account you can enter your User ID and Password and click on

You will then see a survey form. Fill out the survey form and click on



You will then see a Thankyou screen, informing you that you have completed the software registration process and that you have been sent a Registration ID by email.

Click on the link
Download ISE WebPACK

You may need to enter your User ID and Password again to access the download area.

Click on the WebInstall link.

Follow the instructions on the Xilinx website for WebInstall:

"…Just download and run the **WebInstall** program and select your desired installation options. The current Service Pack will be installed automatically at the same time. WebInstall allows you to resume your ISE *WebPACK* download at the point of disconnect should a network problem occur during your download."

The install progress bar will appear while the install program downloads and installs all of the modules. This can take a long time, and may be an "overnight" task depending on the speed of your internet connection.

Once you have completed the installation process you will have a new icon on your desktop:

Xilinx ISE 8.1i

Listing 1: FLASHe.vhd VHDL Code

```
Library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity FLASHe is
   Port (
      Clk : in STD_LOGIC;
      Rst_n : in STD_LOGIC;
      LED : out STD_LOGIC
   );
end FLASHe;

architecture RTL of FLASHe is
signal FlashCount : STD_LOGIC_VECTOR(23 downto 0);
signal Rst : STD_LOGIC;
begin
   Rst <= not Rst_n;
   process (Clk)
   begin
      if (Rst = '1') then
         FlashCount <= (others => '0');
      elsif (Clk'event and Clk='1') then
         FlashCount <= FlashCount + 1;
      end if;
   end process;
   LED <= std_logic(FlashCount(23));
end RTL;
```

2. Create a new project.

Start Xilinx ISE 8.1i by double clicking on the desktop icon.

Do:
File
New Project

Enter a Name & Location for the project:
FLASHe
C:\Projects\FLASHe

Top-Level Source Type = HDL

Click Next

Select the device & design flow:

Product Category = General Purpose
Device family = Spartan2E
Device = xc2s300e
Package = pq208
Speed = -6

Other values are:
HDL
XST (VHDL/Verilog)
ISE Simulator (VHDL / Verilog)
Enable Enhanced Design Summary = TICK.
All other = UNTICKED.

Click Next

Skip the Create New Source dialog box by clicking Next (we will add the source file to the project after project creation).

Click Next.

Skip the Add Existing Sources dialog box. Click Next.

Click Finish.

Do:
Project
New Source…
VHDL Module
File Name = FLASHe

Make sure the Add to Project checkbox is TICKED.

Click Next.

Fill in:
Architecture Name = RTL
(RTL stands for Register Transfer Level)

Fill in the table with
CLK in
Rst_n in
LED out

Click, next, finish

The project environment will now pop up.

In the Sources box, double click on the item
FLASHe – RTL (FLASHe.vhd)

This will pop up the window with the VHDL source code for your project.

Modify the code so that it looks like the code in Listing 1.

Do:
File
Save

3. Assign the pinouts of the device.

You will now need to tell the compiler which pins you want associated with which signals in your design. The compiler reads the UCF (user constraints file) file to get this information. You can use the Assign Package Pins process to enter the information that is written to the UCF file. In the following procedure, you will write the pinout / location information into the UCF file, using the Assign Package Pins process.

The "Processes " box on the bottom left of your design environment now contains all of the processes that can operate on this design.

Single click on the "+" next to User Constraints in the Processes window to expand out the processes.

Double click on the "Assign Package Pins" process.

A Project Navigator dialog box will pop up, asking you if you would like the Project Navigator to automatically create a UCF file and add it to the project. Click Yes.

The compiler will run, and the Xilinx PACE tool window will then open.

In the Design Object List – I/O Pins window, click in the Loc fields, and fill them in with the following pad numbers:

Clk	P77
LED	P82
Rst_n	P57

Do:
File
Save
The Bus Delimiter dialog box will pop up.

Select:
XST Default <>

Click OK.

Close the Xilinx PACE program.

You can now have a look at your new UCF file by double clicking on the Edit Constraints (Text) process. Have a look at the UCF file, and then close this window.

Single click on the "FLASHe – RTL (FLASHe.vhd)
" source in the "Sources in Project" window, to make sure that this source is selected.

Single click on the "+" next to Implement Design in the Processes window so that you can see the Translate, Map and Place & Route processes.

Double click on the Implement Design process. You should get green-ticks on all of the Translate, Map and Place & Route process items, as these processes complete.

You may get a yellow exclamation mark on some processes. This is OK. It just means that a warning has been generated in a process. Warnings are not necessarily design errors. You can view the warnings

in the transcript window (do View, then tick Transcript).

Your design has now been implemented. All that remains is the creation of the programming file for downloading, and the hardware configuration.

4. Create the programming file.

Right click on the Generate Programming File process, and select Properties…

Click on the Startup Options category.

Set:
FPGA Start-Up Clock = JTAG Clock

(If you are using the B5-X300 in the Sydney-X1, Sydney-X2 or with a B5-X-Flash-Config PROM module, then the FPGA Start-Up Clock must be set to CCLK. In this case you will need to generate a PROM programming file, using the Generate PROM, ACE or JTAG file process.)

Click OK.

Double click on the Generate Programming File process. When the process completes, you will get a green-tick.

You should also see the message in the Transcript window:
"Process "Generate Programming File" completed successfully"

5. Configure the FPGA.

Connect the download pod board to the parallel port of the PC using the parallel port flat-cable.

Connect the 10 way flat-cable on the download pod board to the JTAG MODE header (J12) on the B5-X300 board.

(In the Sydney-X1 or Sydney-X2 the download pod board is connected to B5-X-Flash-Config module and you will actually be programming the XCF02S device instead of the FPGA directly).

Ensure that header M1 on the CONFIG MODE SEL header block, located in the corner of the B5-X300 board near slots B and C, is shorted with a header shunt. This sets the FPGA configuration mode to JTAG.

(In the Sydney-X1 or Sydney-X2 the jumpers are factory set for you).

Check that your regulated DC power supply is +5V, before you connect it to your B5-X300 board. Connect the supply to your board.

Ensure that the green LED on the download pod board, labelled "PROG", is on. The pushbutton switches on the download pod board control the PROG / LOCK function. When the download board is in PROG mode, the FPGA can be configured through the cable.

Double click on the Configure Device (iMPACT) process.

The iMPACT – Welcome to iMPACT dialog box will pop up.

Select the radio button:
Configure devices using Boundary-Scan (JTAG)
Automatically connect to a cable…

Click Finish.

The Assign New Configuration File dialog box will pop up.

Select the bit file:
flashe.bit

A dialog box with the following message will pop up:
"A BIT file describing an xc2s300e is about to be assigned to a device previously identified as an xcv300e. Are you sure you want to do this?"
Click Yes.
The reason for this message is that the ID code for the xcv300e device is the same as for the xc2s300e device.

Right click on the Xilinx FPGA icon, and select Program…

A dialog box will pop up. Make sure that the Verify checkbox is unticked.

Click OK.

A progress bar indicator will pop up, which shows the progress of the download of the FPGA configuration bitstream. When finished, you will get a "Program Succeeded" message, and the LED on your B5-X300 board will be flashing at a rate of about 2.9Hz (the factory setting of the header programmable oscillator is 48MHz).

If you hold down the reset switch on the board, the LED will go off. If you release the reset switch, the LED will begin to flash again.

That completes the quickstart exercise. If you wish, try modifying the code to flash the LED at a faster rate, and running through the procedure again. You will then be ready to try your own designs, or move onto one of the more advanced tutorials. There are links to resources on the BurchED website at http://www.BurchED.com.au/resources.html , which you can use as references for designing your own projects.

6. Support.

Please email Tony Burch, tony@BurchED.com.au, with any questions, comments, feedback or requests for support.

Thanks for purchasing the B5-X300 board. We hope you will get much enjoyment from using it. **J**