CPLD SVF File Descriptions

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1.0 About this design

This document briefly mentions the SVF files we have used and created. Where an SVF was provided from XESS just the svf file is given. For ones we have created, the source, ucf and svf files are given.

2.0 SVF formats

dwlndpar.svf

The default file from XESS. Allows programming of the FPGA and connects the parallel port to the FPGA through the lines that also connect to the hex displays. Also controls bargraph LEDs 0 and 1 to indicate download status.

flashprg.svf

This file provided by XESS is used to program the Flash memory through the parallel port. This file is automatically downloaded when an EXO file is dropped into GXSLOAD.

flashcfg.svf

This file provided by XESS is used so that the CPLD will configure the FPGA when power is applied to the board. This should be used after an EXO is programmed to the flash memory to allow the board to always configure the FPGA on start-up and is automatically programmed into the CPLD after an EXO file is dropped into GXSLOAD.

dwnldhex.svf, dwnldhex.vhd, dwnldhexpins.ucf

A file we altered from dwnldpar.svf to allow programming through the CPLD but not connect the parallel port afterwards. The output of the CPLD to the bargraph leds was also removed. It eliminates the contention we would have with the hex displays and bargraph LEDs otherwise. This file, or one like it, should be used if access to the hex displays and bargraph LEDs 0 and 1 are required.

cpldnet.svf, cpldnet.vhd, cpldnetpins.ucf

A file we created for configuring the Ethernet chip and output Ethernet chip output data. Must be used for the network project. The parallel port is still passed through the CPLD to the FPGA and the SVF will still allow downloading of new bitstreams.