UNS Analog Computer – Hardware Architecture Overview

1. System Overview

The UNS Analog Computer is organized as a **modular, hierarchical analog processing system**, where each circuit board contributes a distinct layer of functionality. The system architecture allows arbitrary combinations of computation, input, and output elements to form continuous, programmable UNS networks.

Primary Hardware Layers

Layer	Function	Description
Backplane	Power, interconnect, and configuration bus	Hosts up to 8 slots for interchangeable tiles, provides power distribution, signal buses, and configuration control.
Processing Tile	Core computation node	Each tile performs one UNS operation (e.g., MERGE, MIX, CANCEL) continuously and in parallel with others.
Input/Output Modules	External interface	Translate sensor and actuator signals into UNS domain and vice versa.
Configuration Plane	Defines operation and routing	Determines which operation each tile performs, and how inputs/outputs connect.
Control Interface (optional)	Digital configuration	Provides PC, MCU, or FPGA control via I^2C/SPI/UART.

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2. Architectural Goals

1. **Fully modular composition** – every functional block can be added, removed, or replaced independently.
2. **Continuous-time computation** – all analog operations occur simultaneously, not clocked sequentially.
3. **Programmable topology** – network connectivity and operator selection are defined by configuration plane.
4. **Stable normalization** – global feedback enforces total signal normalization across tiles.
5. **Differential signal integrity** – all critical analog lines use balanced pairs for noise immunity.

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3. System Components

3.1 Backplane Board

The **backplane** provides the physical and electrical foundation for the UNS analog computer.

Functions: - Distributes ±12 V power and +3.3 V logic rail. - Carries shared analog buses (READ±, NORM±, ALPHA±). - Hosts 8 tile slots with keyed connectors. - Provides configuration and I/O ports. - Includes differential buffering for signal preservation between backplanes.

Typical Specifications: - Size: ~200×200 mm (8-slot layout) - Layers: 4-layer PCB (power + analog + digital separation) - Bus impedance: 100 Ω differential pairs - Power rating: 12 V @ 2 A per backplane

Connectors: - 20-pin edge connector per tile slot - 2× differential bus extension ports (for chaining backplanes) - Dedicated Input/Output headers (8×8 analog channels)

3.2 Processing Tile

Each **tile** implements a single UNS operator, physically embodying one transformation in the computation graph.

Core Features: - Dual-mode configuration (manual DIPs + EEPROM) - Reconfigurable analog core using op-amps, OTAs, and analog switches - Optional α(t) modulation input and ψ(t) readout buffer - Status LED indicating configuration load state

Electrical Summary: - Power: ±12 V analog, +3.3 V logic - Input range: ±9 V differential - Bandwidth: DC–500 kHz (operator dependent) - Power draw: ~50 mA per rail

Supported UNS Operations: | Opcode | Operation | Function | |--------|------------|-----------| | 0x00 | MERGE | Weighted summation + normalization | | 0x01 | CANCEL | Differential subtraction | | 0x02 | MIX | Weighted interpolation with α(t) | | 0x03 | MASK | Threshold mask generation | | 0x04 | OVERLAP | Overlap (shared magnitude) detection | | 0x05 | DIST_L1 | Absolute difference metric | | 0x06 | DOT | Correlation (dot product) | | 0x07 | NORM | Normalization feedback node |

Each tile is one continuous, self-contained computation node.

3.3 Input and Output Modules

Input and Output Modules (IOMs) provide direct connections to the physical world.

Type	Description	Ports
Input Module (UIN)	Accepts analog or converted digital sensor signals and scales them into UNS input voltages.	Up to 8 analog input channels

Type	Description	Ports
Output Module (UOUT)	Drives analog actuators or indicators using UNS readout voltages.	Up to 8 analog output channels

Each module connects via the **dedicated backplane I/O ports**, not occupying computation tile slots.

I/O modules include isolation, gain control, and protection circuits for field robustness.

3.4 Configuration Plane

The **Configuration Plane** defines the logical wiring and operational mode of every tile.

Key features: - Each tile contains a small EEPROM storing its operational configuration. - Manual override switches and potentiometers provide standalone programmability. - AUTO/MANUAL jumper selects between digital or physical configuration. - I^2C bus connects EEPROMs to the PC or controller for configuration upload.

This allows each tile to “know” its operation without software execution — configuration *is* the program.

3.5 Signal Buses

All tiles communicate through shared differential analog buses.

Bus	Function	Voltage Range	Bandwidth
READ±	Readout signal bus for ψ(t) propagation	±9 V diff	DC–100 kHz
NORM±	Normalization feedback bus (Σ	ψ	^{2})
ALPHA±	Modulation and control input bus	±9 V diff	DC–50 kHz
SYNC±	Timing reference (optional)	±2 V diff	50 kHz

Each bus is impedance-matched and buffered across backplanes to ensure consistent performance.

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4. System Interconnect Topologies

Mode	Description	Use Case
Single Backplane	One backplane hosting up to 8 tiles with I/O modules attached	Compact system, local computation

Mode	Description	Use Case
Chained Backplanes	Backplanes linked via differential bus extensions	Expands tile count; minimal latency
Star Configuration	Backplanes connected via central hub	Ideal for mixed analog/digital hybrid setups

Each topology maintains coherent α(t) synchronization and normalization feedback across all modules.

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5. Example System Layout

4 Sensors → 3 Compute Tiles → 1 Output Example:

```
[Sensors] → [Input Module] → [Backplane]
    │          │
    ▼          ▼
  Tile 1  (MERGE)
  Tile 2  (CANCEL)
  Tile 3  (MIX)
    ▼          ▼
 [Output Module] → LED/Buzzer
```

This simple setup continuously computes:

```
ψ_out = MIX( CANCEL( MERGE(S1, S2), MERGE(S3, S4) ), α )
```

Each operation is performed by its respective tile, all running concurrently.

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6. Backplane Power and Signal Summary

Signal	Description	Distribution
±12 V	Analog power rails	Power plane pair across slots
+3.3 V	Logic power	For EEPROM and analog switches
GND	Common ground	Star-grounded to PSU entry
READ±, NORM±, ALPHA±	Differential buses	Routed as matched pairs
SDA/SCL	I^2C configuration bus	Shared across all tiles
SYNC±	Synchronization line	Differential pair

7. Expandability

- Each backplane supports up to 8 tiles.
- Multiple backplanes can be chained to increase computation depth.
- I/O modules can scale independently (1 to 8 channels each).
- Digital configuration supports addressing up to 64 tiles (8 backplanes).

Next Document: UNS Tile Design Specification – detailed description of the reconfigurable tile hardware and configuration logic.