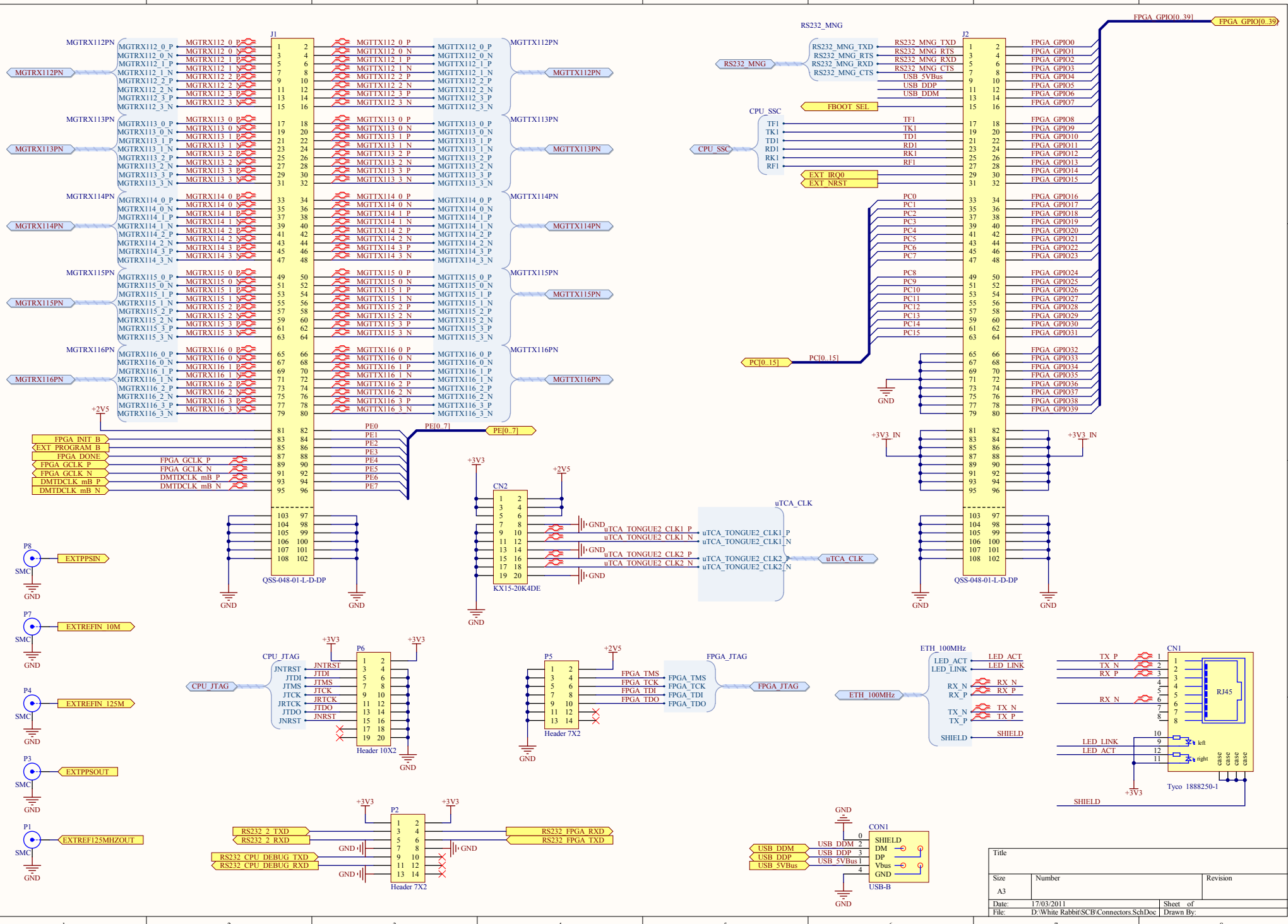
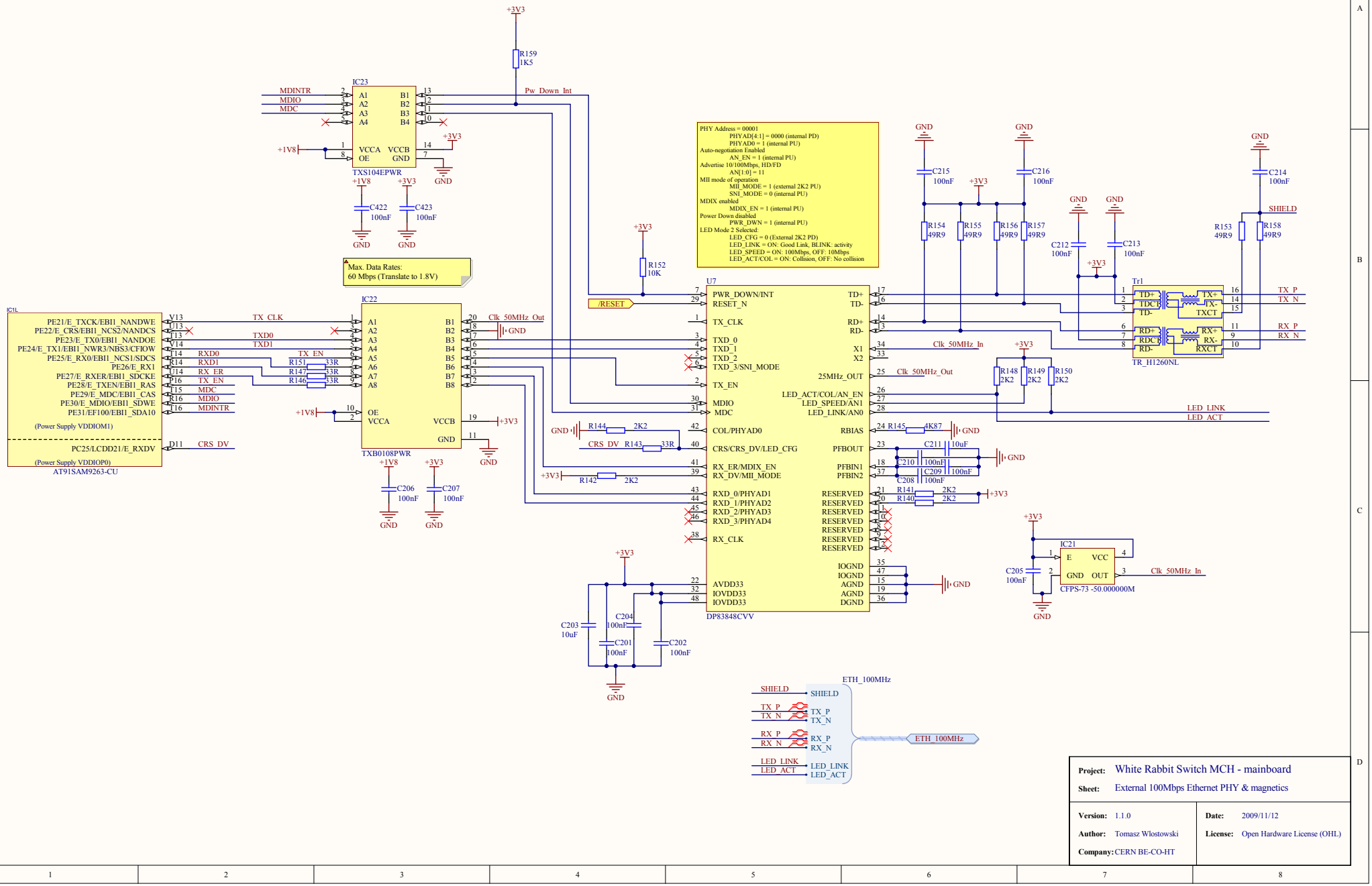
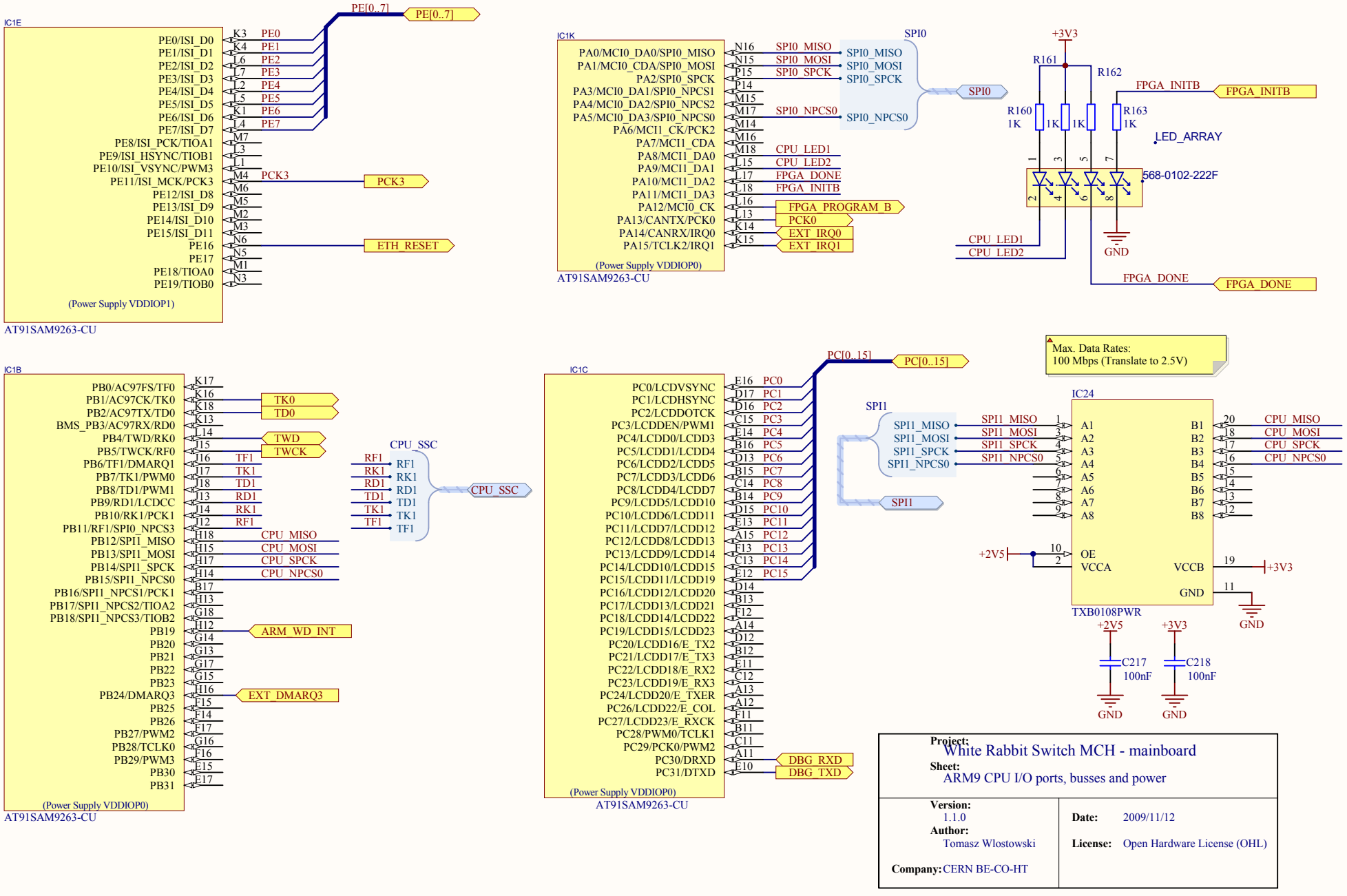
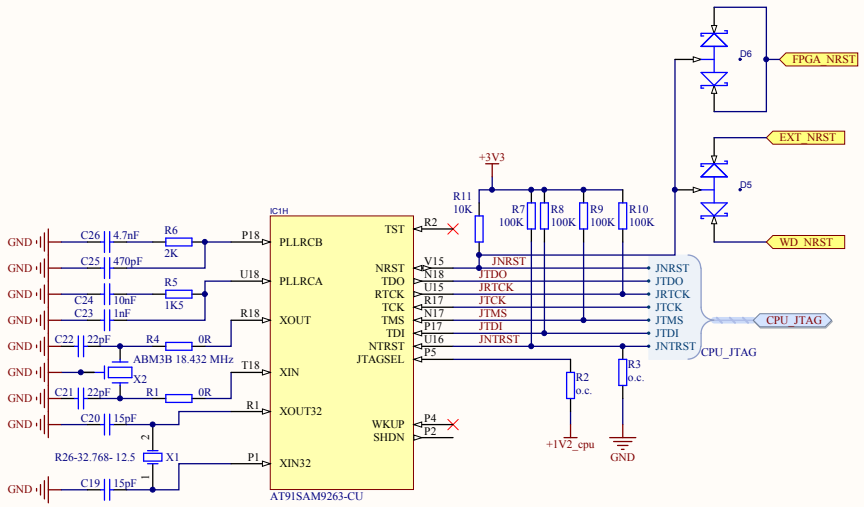
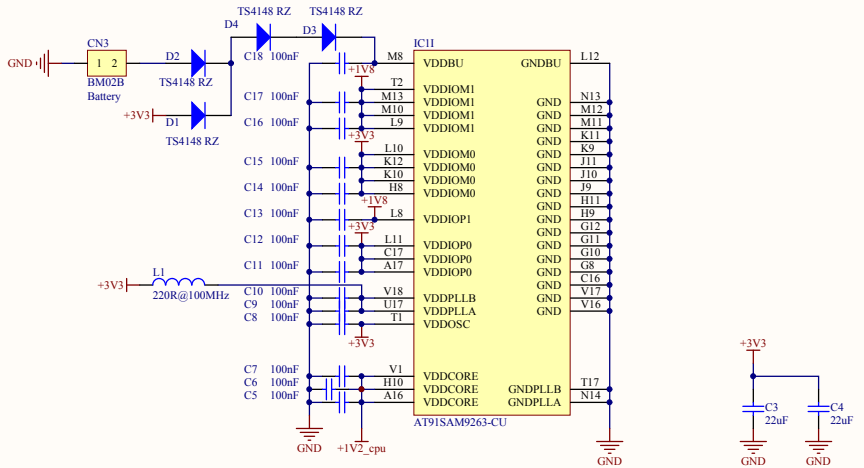
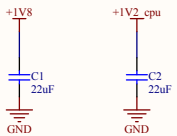

J1
J2
QSS-048-01-L-D-DP
KX15-20K4DE
CN2
P8
P7
P4
P3
P1
P6
P5
P2
CON1
CN1
RJ45
Tyco 1888250-1
USB-B
Header 10X2
Header 7X2
MGTRX112PN
MGTTX112PN
MGTRX113PN
MGTTX113PN
MGTRX114PN
MGTTX114PN
MGTRX115PN
MGTTX115PN
MGTRX116PN
MGTTX116PN
RS232_MNG
CPU_SSC
CPU_JTAG
FPGA_JTAG
ETH_100MHz
uTCA_CLK
FPGA_GPIO[0..39]
PE[0..7]
PC[0..15]
EXTPPSIN
EXTREFIN_10M
EXTREFIN_125M
EXTPPSOUT
EXTREF125MHZOUT
FBOOT_SEL
EXT_IRQ0
EXT_NRST
FPGA_INIT_B
EXT_PROGRAM_B
FPGA_DONE
FPGA_GCLK_P
FPGA_GCLK_N
DMTDCLK_mB_P
DMTDCLK_mB_N
RS232_2_TXD
RS232_2_RXD
RS232_CPU_DEBUG_TXD
RS232_CPU_DEBUG_RXD
RS232_FPGA_RXD
RS232_FPGA_TXD
USB_DDM
USB_DDP
USB_5VBus
LED_ACT
LED_LINK
SHIELD
+2V5
+3V3
+3V3_IN
GND
Title
Size
A3
Number
Revision
Date:
17/03/2011
Sheet of
File:
D:\White Rabbit\SCB\Connectors.SchDoc
Drawn By:


PHY Address = 00001
PHYAD[4:1] = 0000 (internal PD)
PHYAD0 = 1 (internal PU)
Auto-negotiation Enabled
AN_EN = 1 (internal PU)
Advertise 10/100Mbps, HD/FD
AN[1:0] = 11
MII mode of operation
MII_MODE = 1 (external 2K2 PU)
SNI_MODE = 0 (internal PU)
MDIX enabled
MDIX_EN = 1 (internal PU)
Power Down disabled
PWR_DWN = 1 (internal PU)
LED Mode 2 Selected:
LED_CFG = 0 (External 2K2 PD)
LED_LINK = ON: Good Link, BLINK: activity
LED_SPEED = ON: 100Mbps, OFF: 10Mbps
LED_ACT/COL = ON: Collision, OFF: No collision
Max. Data Rates:
60 Mbps (Translate to 1.8V)
IC23
TXS104EPWR
IC22
TXB0108PWR
U7
DP83848CVV
IC1L
AT91SAM9263-CU
Tr1
TR_H1260NL
IC21
CFPS-73 -50.000000M
ETH_100MHz
Project: White Rabbit Switch MCH - mainboard
Sheet: External 100Mbps Ethernet PHY & magnetics
Version: 1.1.0
Date: 2009/11/12
Author: Tomasz Wlostowski
License: Open Hardware License (OHL)
Company: CERN BE-CO-HT


IC1E
PE0/ISI_D0
PE1/ISI_D1
PE2/ISI_D2
PE3/ISI_D3
PE4/ISI_D4
PE5/ISI_D5
PE6/ISI_D6
PE7/ISI_D7
PE8/ISI_PCK/TIOA1
PE9/ISI_HSYNC/TIOB1
PE10/ISI_VSYNC/PWM3
PE11/ISI_MCK/PCK3
PE12/ISI_D8
PE13/ISI_D9
PE14/ISI_D10
PE15/ISI_D11
PE16
PE17
PE18/TIOA0
PE19/TIOB0
(Power Supply VDDIOP1)
AT91SAM9263-CU
PE[0..7]
PCK3
ETH_RESET
IC1K
PA0/MCI0_DA0/SPI0_MISO
PA1/MCI0_CDA/SPI0_MOSI
PA2/SPI0_SPCK
PA3/MCI0_DA1/SPI0_NPCS1
PA4/MCI0_DA2/SPI0_NPCS2
PA5/MCI0_DA3/SPI0_NPCS0
PA6/MCI1_CK/PCK2
PA7/MCI1_CDA
PA8/MCI1_DA0
PA9/MCI1_DA1
PA10/MCI1_DA2
PA11/MCI1_DA3
PA12/MCI0_CK
PA13/CANTX/PCK0
PA14/CANRX/IRQ0
PA15/TCLK2/IRQ1
(Power Supply VDDIOP0)
AT91SAM9263-CU
SPI0_MISO
SPI0_MOSI
SPI0_SPCK
SPI0_NPCS0
CPU_LED1
CPU_LED2
FPGA_DONE
FPGA_INITB
FPGA_PROGRAM_B
PCK0
EXT_IRQ0
EXT_IRQ1
SPI0
+3V3
R161
R162
R160
1K
R163
LED_ARRAY
568-0102-222F
GND
FPGA_INITB
FPGA_DONE
IC1B
PB0/AC97FS/TF0
PB1/AC97CK/TK0
PB2/AC97TX/TD0
BMS_PB3/AC97RX/RD0
PB4/TWD/RK0
PB5/TWCK/RF0
PB6/TF1/DMARQ1
PB7/TK1/PWM0
PB8/TD1/PWM1
PB9/RD1/LCDCC
PB10/RK1/PCK1
PB11/RF1/SPI0_NPCS3
PB12/SPI1_MISO
PB13/SPI1_MOSI
PB14/SPI1_SPCK
PB15/SPI1_NPCS0
PB16/SPI1_NPCS1/PCK1
PB17/SPI1_NPCS2/TIOA2
PB18/SPI1_NPCS3/TIOB2
PB19
PB20
PB21
PB22
PB23
PB24/DMARQ3
PB25
PB26
PB27/PWM2
PB28/TCLK0
PB29/PWM3
PB30
PB31
(Power Supply VDDIOP0)
AT91SAM9263-CU
TK0
TD0
TWD
TWCK
CPU_MISO
CPU_MOSI
CPU_SPCK
CPU_NPCS0
ARM_WD_INT
EXT_DMARQ3
CPU_SSC
RF1
RK1
RD1
TD1
TK1
TF1
IC1C
PC0/LCDVSYNC
PC1/LCDHSYNC
PC2/LCDDOTCK
PC3/LCDDEN/PWM1
PC4/LCDD0/LCDD3
PC5/LCDD1/LCDD4
PC6/LCDD2/LCDD5
PC7/LCDD3/LCDD6
PC8/LCDD4/LCDD7
PC9/LCDD5/LCDD10
PC10/LCDD6/LCDD11
PC11/LCDD7/LCDD12
PC12/LCDD8/LCDD13
PC13/LCDD9/LCDD14
PC14/LCDD10/LCDD15
PC15/LCDD11/LCDD19
PC16/LCDD12/LCDD20
PC17/LCDD13/LCDD21
PC18/LCDD14/LCDD22
PC19/LCDD15/LCDD23
PC20/LCDD16/E_TX2
PC21/LCDD17/E_TX3
PC22/LCDD18/E_RX2
PC23/LCDD19/E_RX3
PC24/LCDD20/E_TXER
PC26/LCDD22/E_COL
PC27/LCDD23/E_RXCK
PC28/PWM0/TCLK1
PC29/PCK0/PWM2
PC30/DRXD
PC31/DTXD
(Power Supply VDDIOP0)
AT91SAM9263-CU
PC[0..15]
DBG_RXD
DBG_TXD
SPI1
SPI1_MISO
SPI1_MOSI
SPI1_SPCK
SPI1_NPCS0
Max. Data Rates:
100 Mbps (Translate to 2.5V)
IC24
A1
A2
A3
A4
A5
A6
A7
A8
B1
B2
B3
B4
B5
B6
B7
B8
OE
VCCA
VCCB
GND
TXB0108PWR
+2V5
+3V3
C217
100nF
C218
100nF
Project:
White Rabbit Switch MCH - mainboard
Sheet:
ARM9 CPU I/O ports, busses and power
Version:
1.1.0
Author:
Tomasz Wlostowski
Company: CERN BE-CO-HT
Date: 2009/11/12
License: Open Hardware License (OHL)







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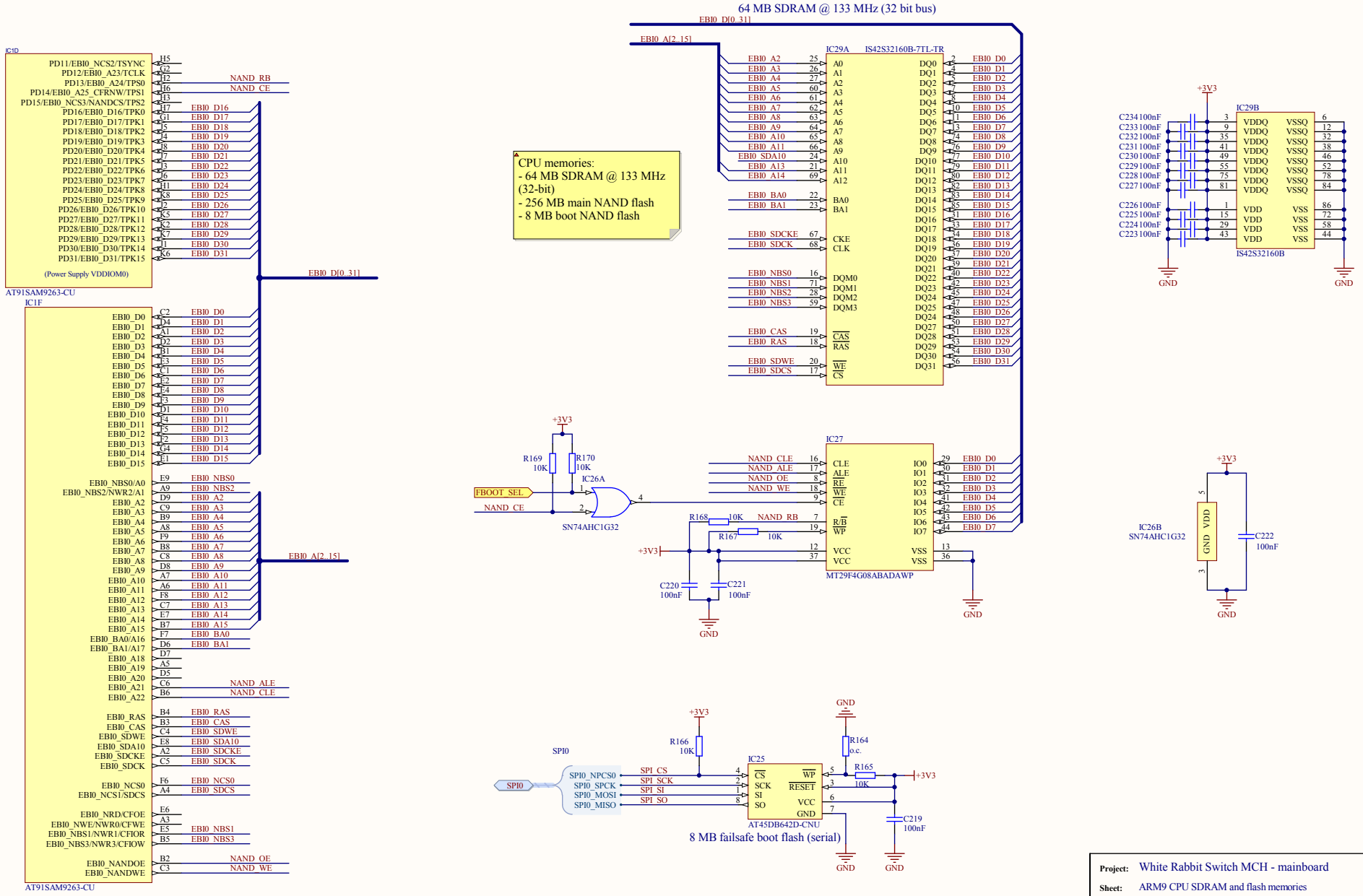
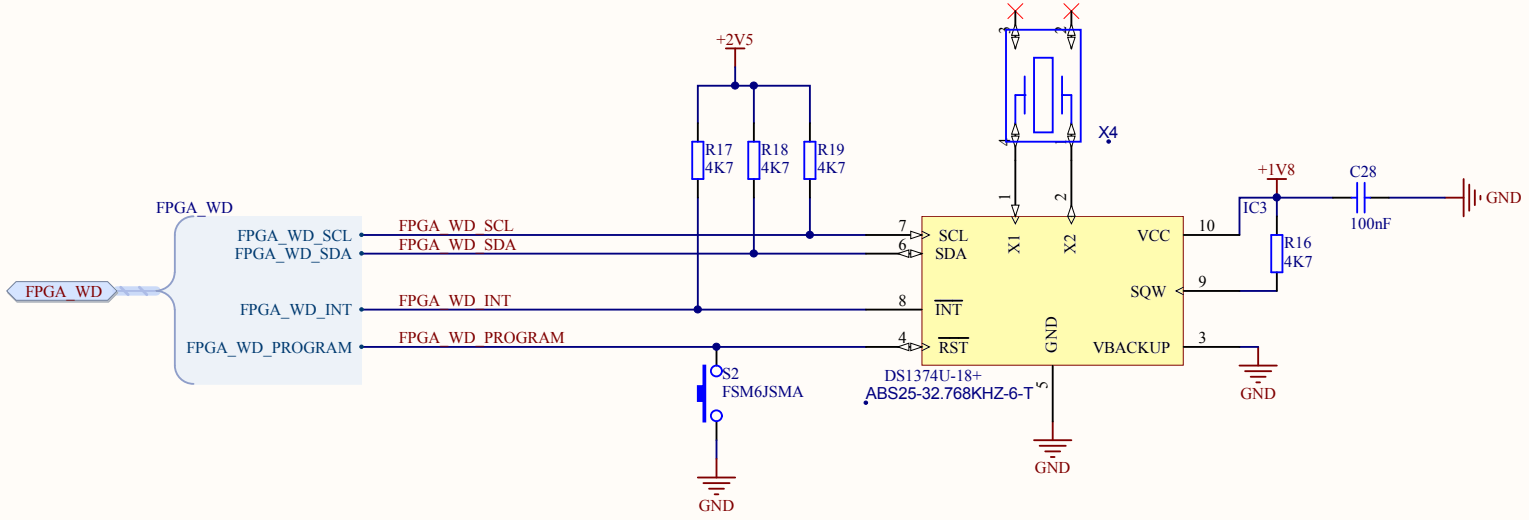
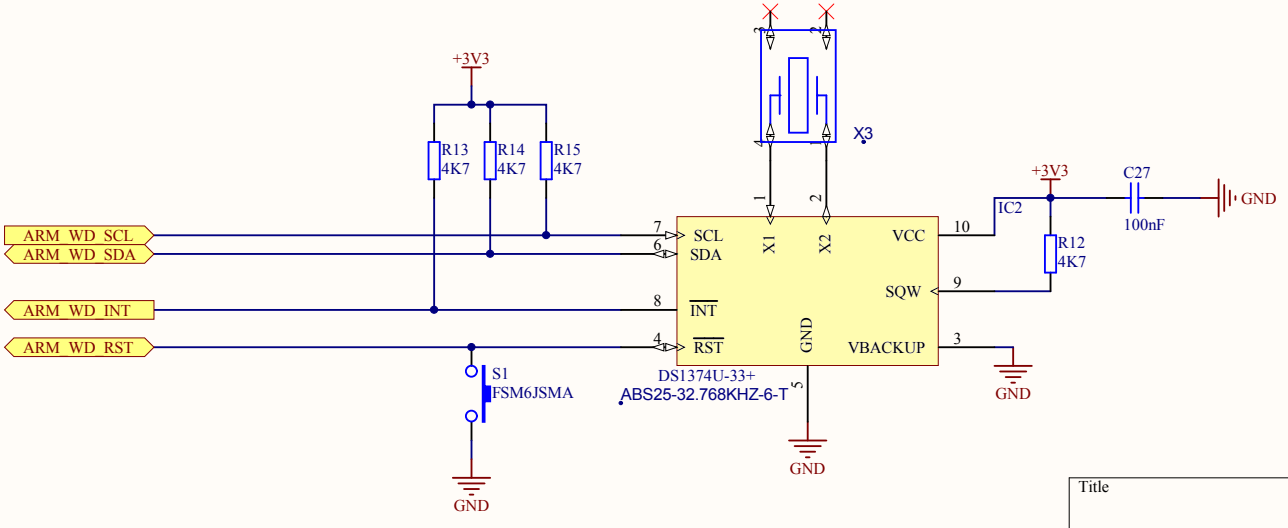


Project:	White Rabbit Switch MCH - mainboard
Sheet:	ARM9 CPU SDRAM and flash memories
Version:	1.1.0
Date:	2009/11/12
Author:	Tomasz Wlostowski
License:	Open Hardware License (OHL)
Company:	CERN BE-CO-HT





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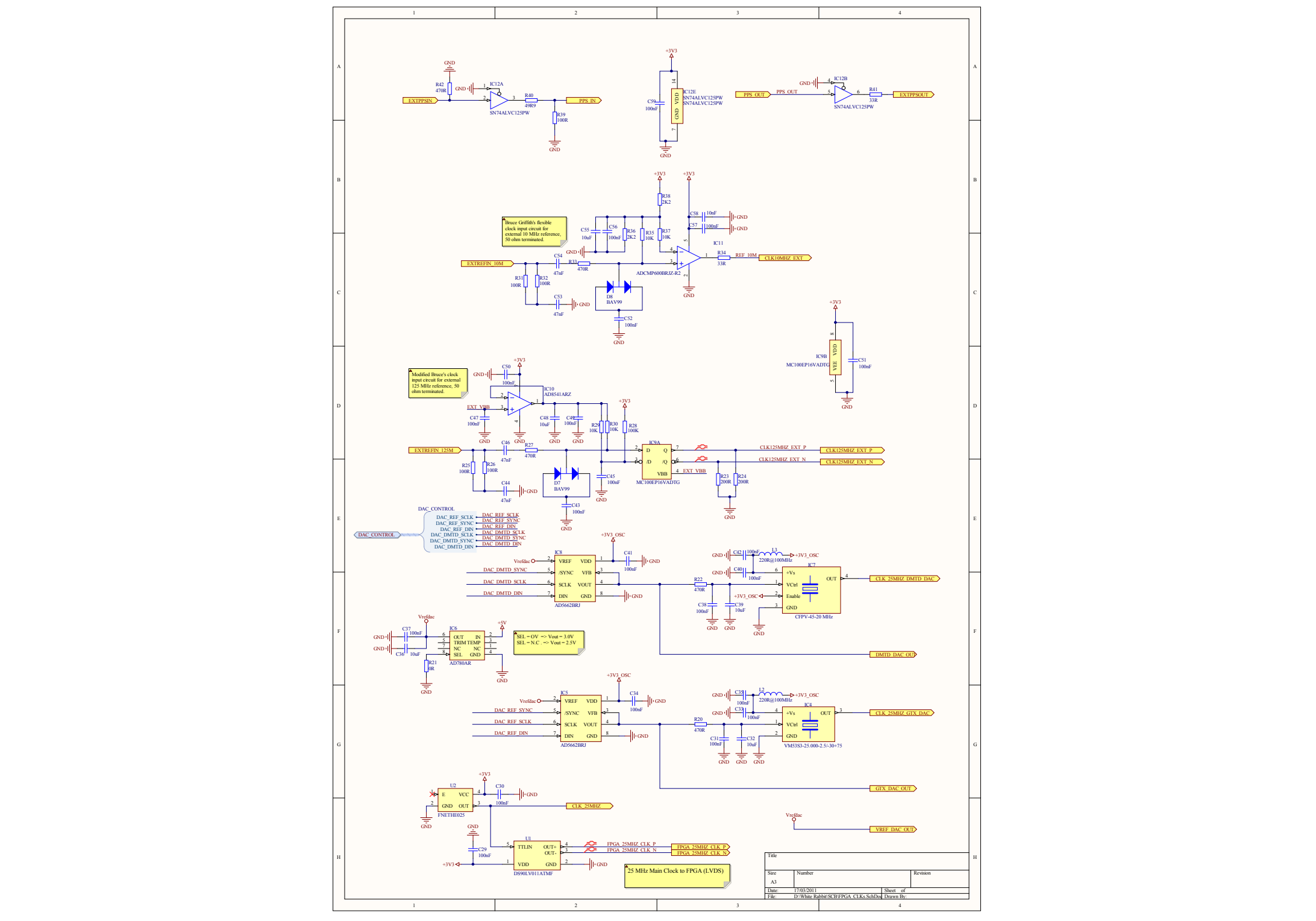
EXTPPSIN
R42 470R
IC12A
SN74ALVC125PW
R40 49R9
R39 100R
PPS_IN
IC12E SN74ALVC125PW
C59 100nF
PPS_OUT
IC12B
R41 33R
EXTPPSOUT
Bruce Griffith's flexible clock input circuit for external 10 MHz reference, 50 ohm terminated.
R38 2K2
C55 10uF
C56 100nF
R36 2K2
R35 10K
R37 10K
C58 10nF
C57 100nF
IC11
ADCMP600BRJZ-R2
EXTREFIN_10M
C54 47nF
R33 470R
R34 33R
REF_10M
CLK10MHZ_EXT
R31 100R
R32 100R
C53 47nF
D8 BAV99
C52 100nF
IC9B MC100EP16VADTG
C51 100nF
Modified Bruce's clock input circuit for external 125 MHz reference, 50 ohm terminated.
C50 100nF
IC10 AD8541ARZ
EXT_VBB
C47 100nF
C48 10uF
C49 100nF
R29 10K
R30 10K
R28 100K
EXTREFIN_125M
C46 47nF
R27 470R
R25 100R
R26 100R
C44 47nF
D7 BAV99
C43 100nF
C45 100nF
IC9A MC100EP16VADTG
CLK125MHZ_EXT_P
CLK125MHZ_EXT_N
R23 200R
R24 200R
DAC_CONTROL
DAC_REF_SCLK
DAC_REF_SYNC
DAC_REF_DIN
DAC_DMTD_SCLK
DAC_DMTD_SYNC
DAC_DMTD_DIN
IC8 AD5662BRJ
C41 100nF
C42 100nF
L3 220R@100MHz
C40 100nF
IC7 CFPV-45-20 MHz
R22 470R
C38 100nF
C39 10uF
CLK_25MHZ_DMTD_DAC
DMTD_DAC_OUT
Vrefdac
IC6 AD780AR
C37 100nF
C36 10uF
R21 0R
+5V
SEL = OV => Vout = 3.0V
SEL = N.C. => Vout = 2.5V
IC5 AD5662BRJ
C34 100nF
C35 100nF
L2 220R@100MHz
C33 100nF
IC4 VM53S3-25.000-2.5/-30+75
R20 470R
C31 100nF
C32 10uF
CLK_25MHZ_GTX_DAC
GTX_DAC_OUT
U2 FNETHE025
C30 100nF
CLK_25MHZ
U1 DS90LV011ATMF
C29 100nF
FPGA_25MHZ_CLK_P
FPGA_25MHZ_CLK_N
25 MHz Main Clock to FPGA (LVDS)
VREF_DAC_OUT
Title
Size A3
Number
Revision
Date: 17/03/2011
Sheet of
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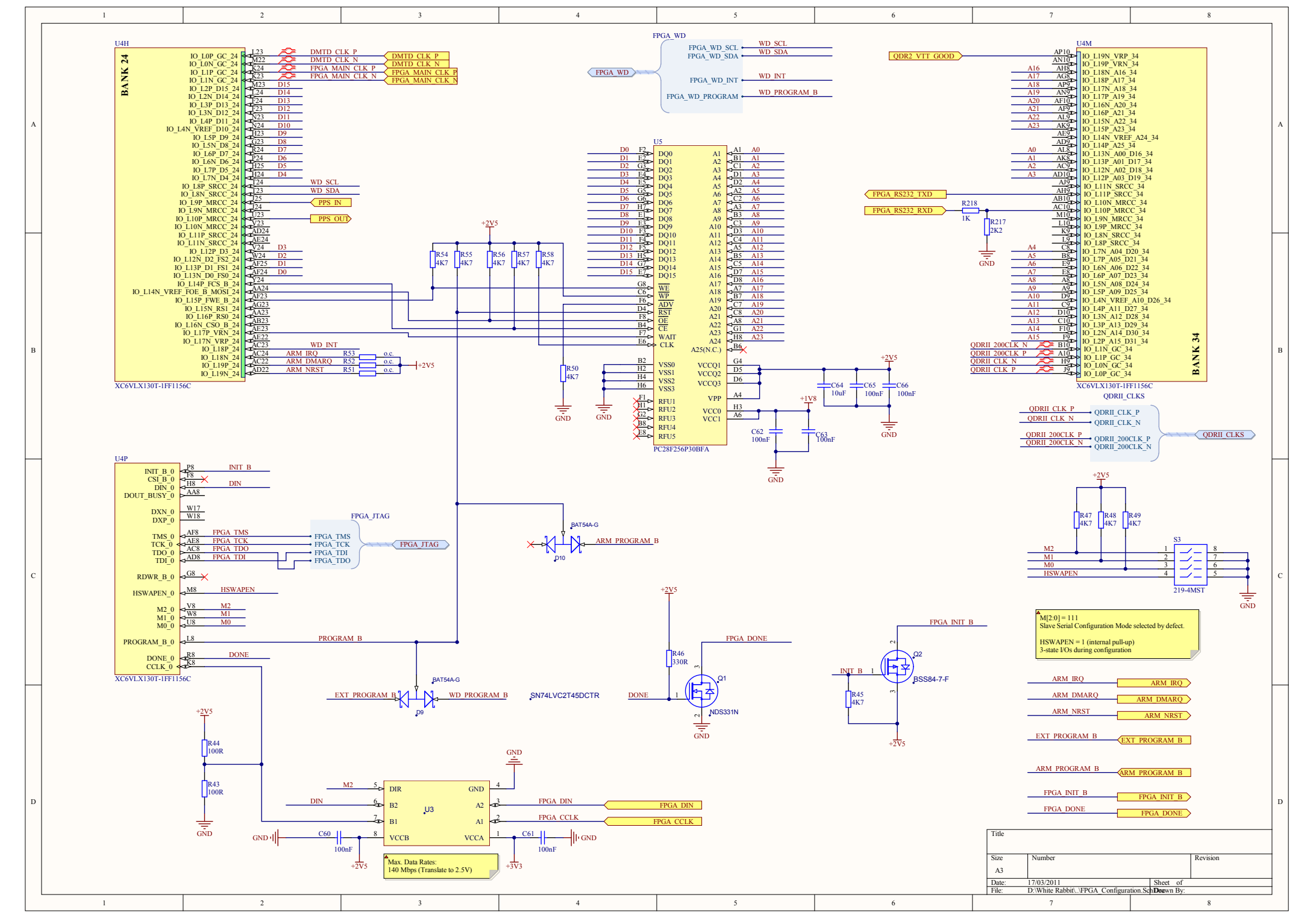
U4H
BANK 24
XC6VLX130T-1FF1156C
DMTD_CLK_P
DMTD_CLK_N
FPGA_MAIN_CLK_P
FPGA_MAIN_CLK_N
WD_SCL
WD_SDA
PPS_IN
PPS_OUT
WD_INT
ARM_IRQ
ARM_DMARQ
ARM_NRST
R53
R52
R51
o.c.
+2V5
FPGA_WD
FPGA_WD_SCL
FPGA_WD_SDA
FPGA_WD_INT
FPGA_WD_PROGRAM
WD_PROGRAM_B
U5
PC28F256P30BFA
R54
R55
R56
R57
R58
4K7
R50
GND
C64
C65
C66
10uF
100nF
C62
C63
+1V8
U4M
BANK 34
QDR2_VTT_GOOD
FPGA_RS232_TXD
FPGA_RS232_RXD
R218
1K
R217
2K2
QDRII_200CLK_N
QDRII_200CLK_P
QDRII_CLK_N
QDRII_CLK_P
QDRII_CLKS
QDRII_200CLK_P
QDRII_200CLK_N
U4P
INIT_B
DIN
PROGRAM_B
DONE
HSWAPEN
FPGA_JTAG
FPGA_TMS
FPGA_TCK
FPGA_TDI
FPGA_TDO
BAT54A-G
D10
ARM_PROGRAM_B
R47
R48
R49
S3
219-4MST
M[2:0] = 111
Slave Serial Configuration Mode selected by defect.
HSWAPEN = 1 (internal pull-up)
3-state I/Os during configuration
R46
330R
FPGA_DONE
Q1
NDS331N
SN74LVC2T45DCTR
EXT_PROGRAM_B
WD_PROGRAM_B
D9
FPGA_INIT_B
Q2
BSS84-7-F
R45
4K7
R44
100R
R43
100R
U3
DIR
B2
B1
VCCB
GND
A2
A1
VCCA
FPGA_DIN
FPGA_CCLK
C60
C61
100nF
+3V3
Max. Data Rates:
140 Mbps (Translate to 2.5V)
Title
Size
A3
Number
Revision
Date:
17/03/2011
Sheet of
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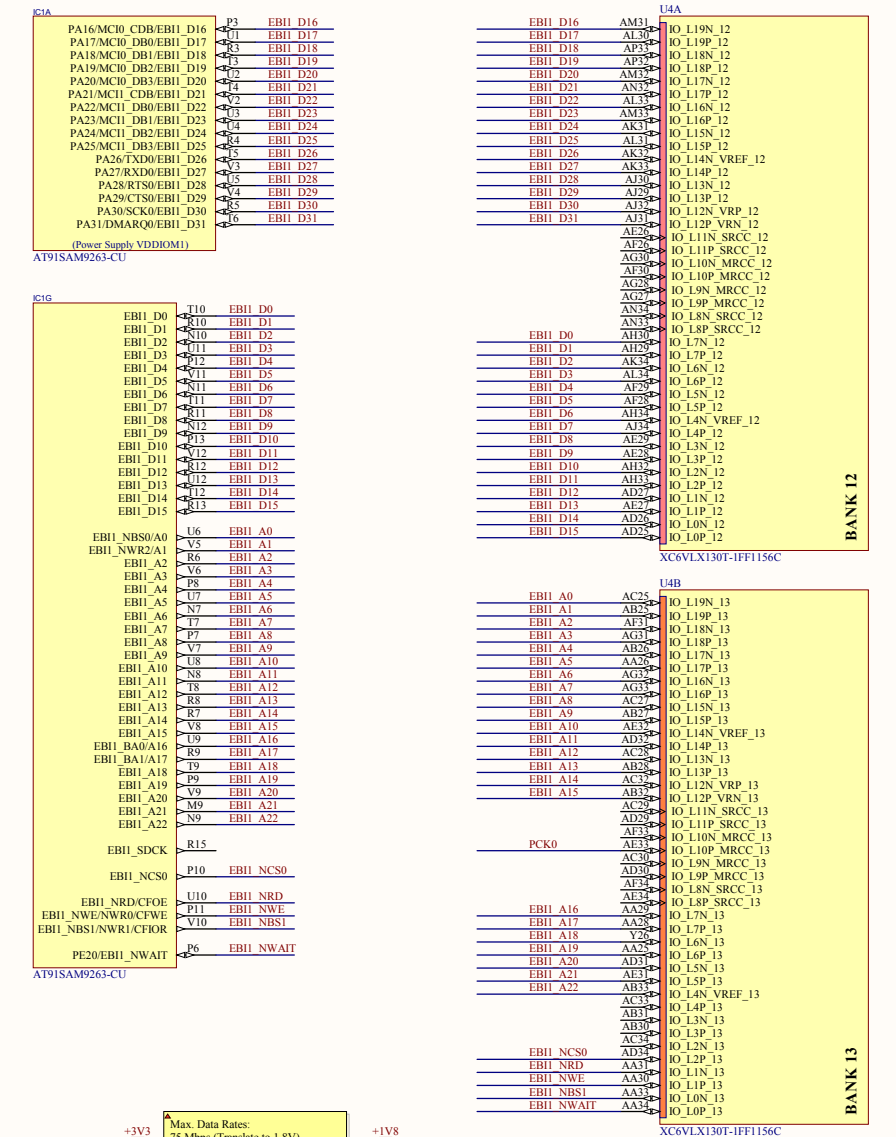
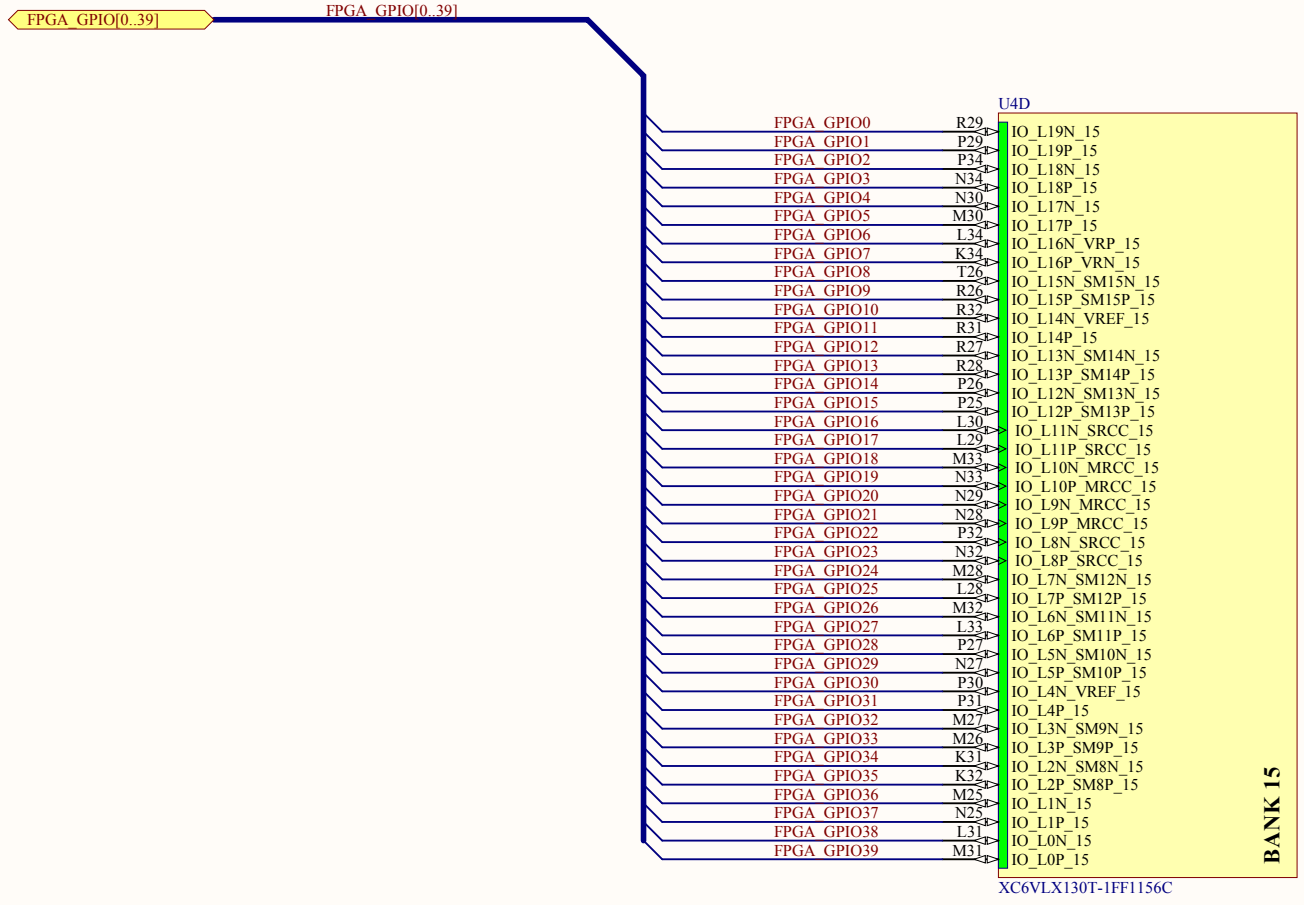
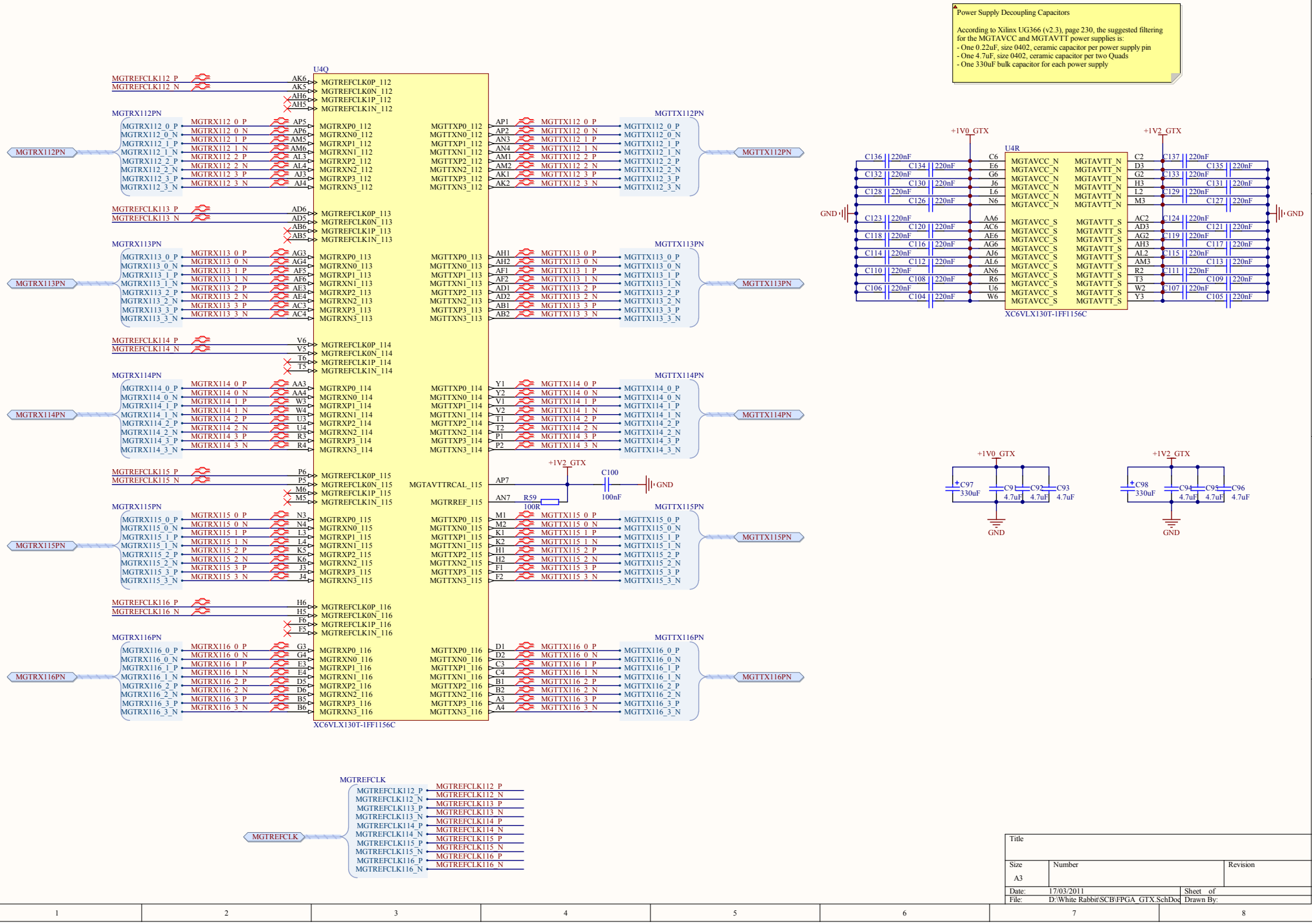
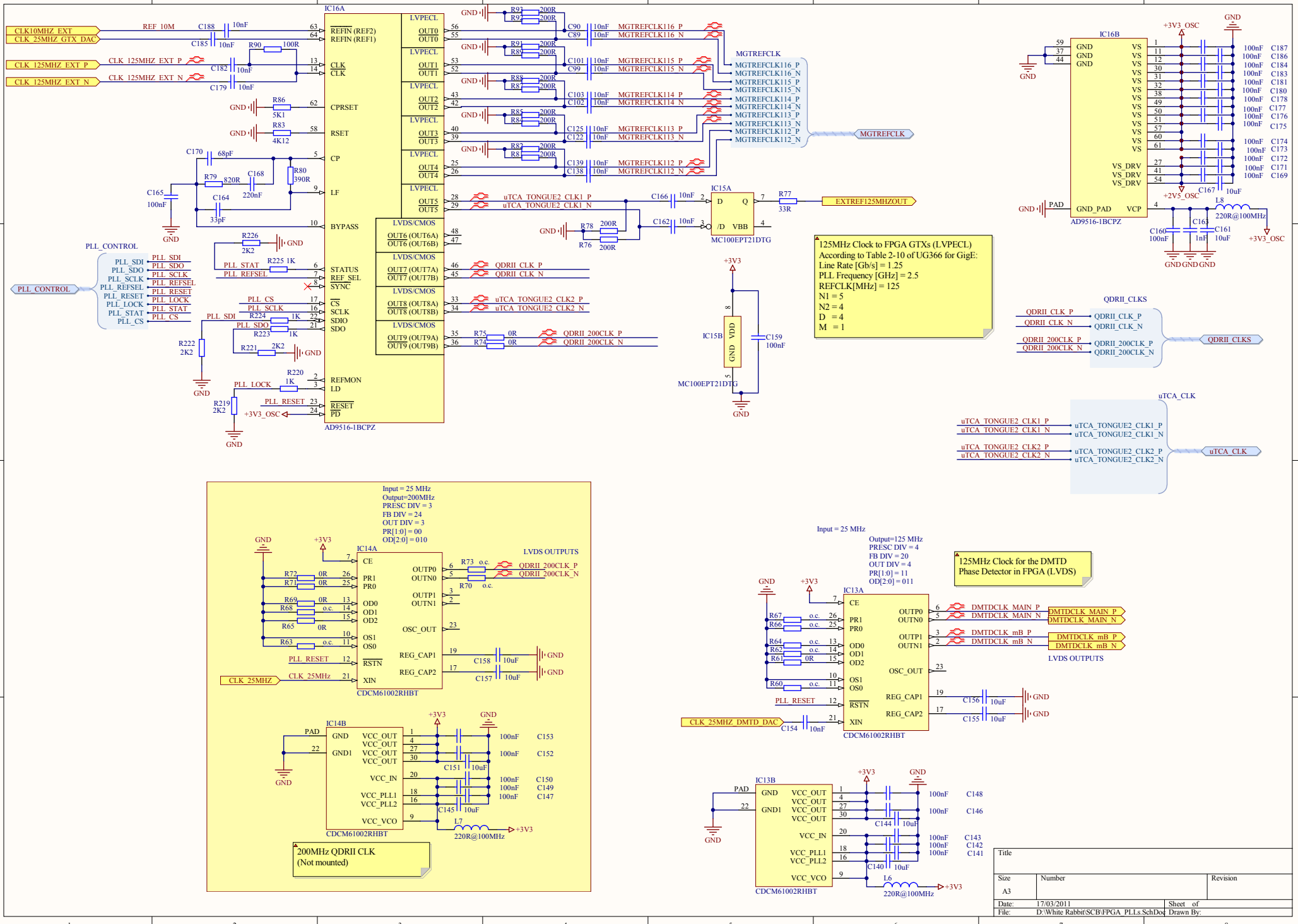
D:\White Rabbit\...\FPGA_Configuration.SchDoc
Drawn By:

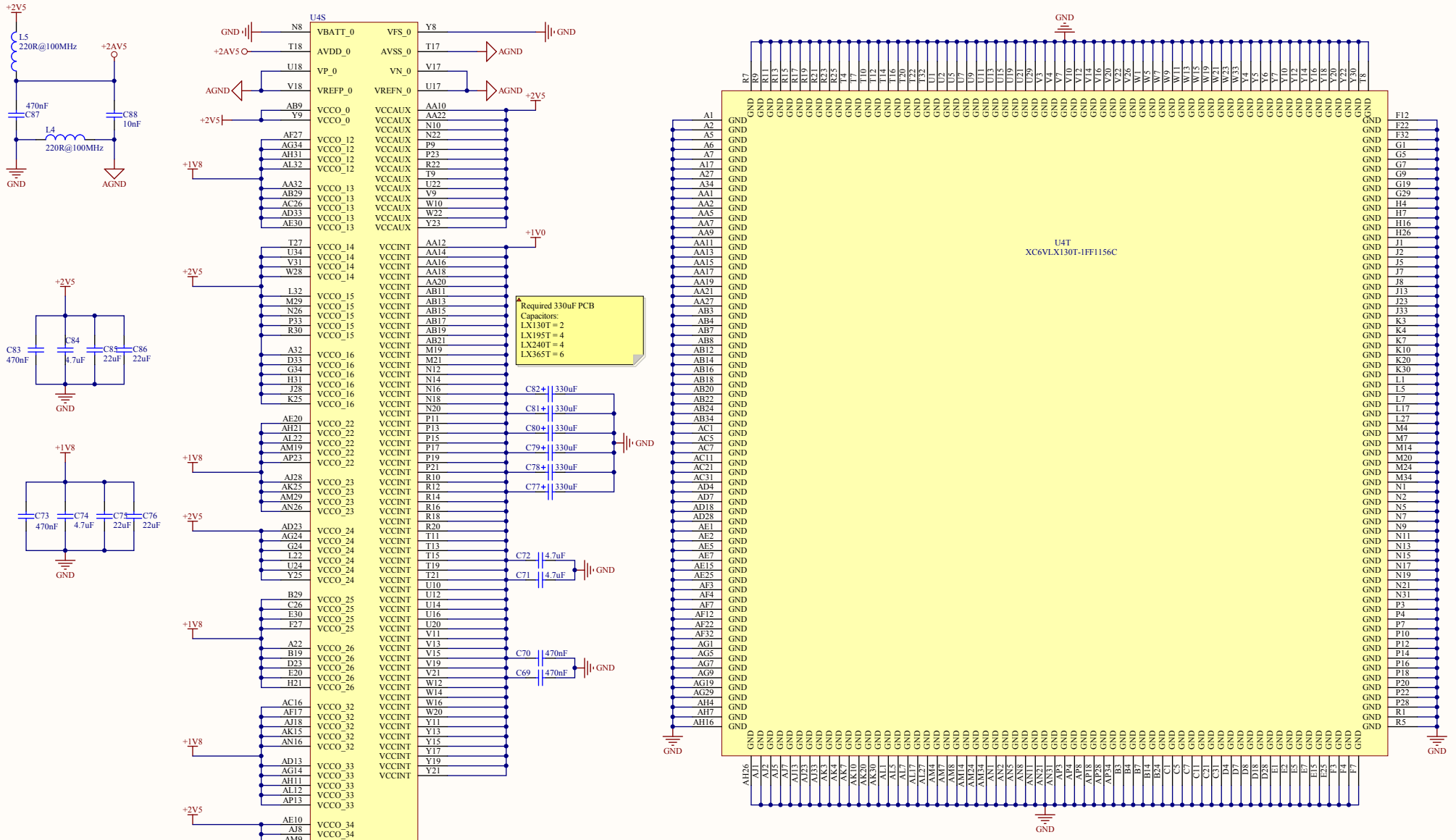

IC1A
PA16/MCI0_CDB/EBI1_D16
PA17/MCI0_DB0/EBI1_D17
PA18/MCI0_DB1/EBI1_D18
PA19/MCI0_DB2/EBI1_D19
PA20/MCI0_DB3/EBI1_D20
PA21/MCI1_CDB/EBI1_D21
PA22/MCI1_DB0/EBI1_D22
PA23/MCI1_DB1/EBI1_D23
PA24/MCI1_DB2/EBI1_D24
PA25/MCI1_DB3/EBI1_D25
PA26/TXD0/EBI1_D26
PA27/RXD0/EBI1_D27
PA28/RTS0/EBI1_D28
PA29/CTS0/EBI1_D29
PA30/SCK0/EBI1_D30
PA31/DMARQ0/EBI1_D31
(Power Supply VDDIOM1)
AT91SAM9263-CU
IC1G
EBI1_D0
EBI1_D1
EBI1_D2
EBI1_D3
EBI1_D4
EBI1_D5
EBI1_D6
EBI1_D7
EBI1_D8
EBI1_D9
EBI1_D10
EBI1_D11
EBI1_D12
EBI1_D13
EBI1_D14
EBI1_D15
EBI1_NBS0/A0
EBI1_NWR2/A1
EBI1_A2
EBI1_A3
EBI1_A4
EBI1_A5
EBI1_A6
EBI1_A7
EBI1_A8
EBI1_A9
EBI1_A10
EBI1_A11
EBI1_A12
EBI1_A13
EBI1_A14
EBI1_A15
EBI1_BA0/A16
EBI1_BA1/A17
EBI1_A18
EBI1_A19
EBI1_A20
EBI1_A21
EBI1_A22
EBI1_SDCK
EBI1_NCS0
EBI1_NRD/CFOE
EBI1_NWE/NWR0/CFWE
EBI1_NBS1/NWR1/CFIOR
PE20/EBI1_NWAIT
AT91SAM9263-CU
U4A
EBI1_D16
EBI1_D17
EBI1_D18
EBI1_D19
EBI1_D20
EBI1_D21
EBI1_D22
EBI1_D23
EBI1_D24
EBI1_D25
EBI1_D26
EBI1_D27
EBI1_D28
EBI1_D29
EBI1_D30
EBI1_D31
IO_L19N_12
IO_L19P_12
IO_L18N_12
IO_L18P_12
IO_L17N_12
IO_L17P_12
IO_L16N_12
IO_L16P_12
IO_L15N_12
IO_L15P_12
IO_L14N_VREF_12
IO_L14P_12
IO_L13N_12
IO_L13P_12
IO_L12N_VRP_12
IO_L12P_VRN_12
IO_L11N_SRCC_12
IO_L11P_SRCC_12
IO_L10N_MRCC_12
IO_L10P_MRCC_12
IO_L9N_MRCC_12
IO_L9P_MRCC_12
IO_L8N_SRCC_12
IO_L8P_SRCC_12
IO_L7N_12
IO_L7P_12
IO_L6N_12
IO_L6P_12
IO_L5N_12
IO_L5P_12
IO_L4N_VREF_12
IO_L4P_12
IO_L3N_12
IO_L3P_12
IO_L2N_12
IO_L2P_12
IO_L1N_12
IO_L1P_12
IO_L0N_12
IO_L0P_12
BANK 12
XC6VLX130T-1FF1156C
U4B
EBI1_A0
EBI1_A1
EBI1_A2
EBI1_A3
EBI1_A4
EBI1_A5
EBI1_A6
EBI1_A7
EBI1_A8
EBI1_A9
EBI1_A10
EBI1_A11
EBI1_A12
EBI1_A13
EBI1_A14
EBI1_A15
PCK0
EBI1_A16
EBI1_A17
EBI1_A18
EBI1_A19
EBI1_A20
EBI1_A21
EBI1_A22
EBI1_NCS0
EBI1_NRD
EBI1_NWE
EBI1_NBS1
EBI1_NWAIT
IO_L19N_13
IO_L19P_13
IO_L18N_13
IO_L18P_13
IO_L17N_13
IO_L17P_13
IO_L16N_13
IO_L16P_13
IO_L15N_13
IO_L15P_13
IO_L14N_VREF_13
IO_L14P_13
IO_L13N_13
IO_L13P_13
IO_L12N_VRP_13
IO_L12P_VRN_13
IO_L11N_SRCC_13
IO_L11P_SRCC_13
IO_L10N_MRCC_13
IO_L10P_MRCC_13
IO_L9N_MRCC_13
IO_L9P_MRCC_13
IO_L8N_SRCC_13
IO_L8P_SRCC_13
IO_L7N_13
IO_L7P_13
IO_L6N_13
IO_L6P_13
IO_L5N_13
IO_L5P_13
IO_L4N_VREF_13
IO_L4P_13
IO_L3N_13
IO_L3P_13
IO_L2N_13
IO_L2P_13
IO_L1N_13
IO_L1P_13
IO_L0N_13
IO_L0P_13
BANK 13
XC6VLX130T-1FF1156C
Max. Data Rates:
75 Mbps (Translate to 1.8V)
SN74LVC2T45DCTR
U6
VCCA
A1
A2
GND
VCCB
B1
B2
DIR
+3V3
+1V8
GND
C67
100nF
C68
100nF
ARM_CLK
PCK0
Title
Size
A4
Number
Revision
Date:
17/03/2011
Sheet of
File:
D:\White Rabbit\..\FPGA_CPU_EBI1.SchDoc
Drawn By:

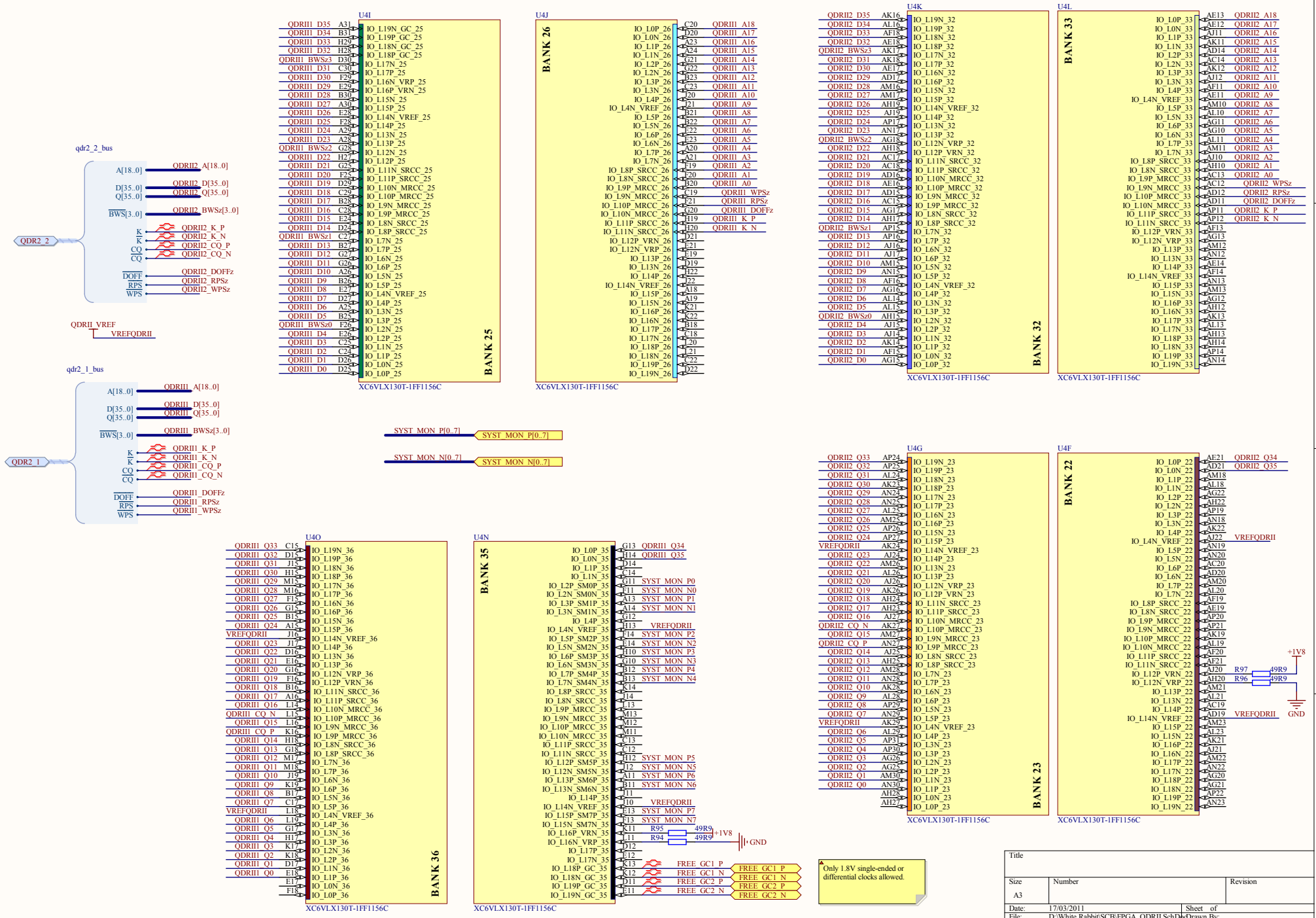


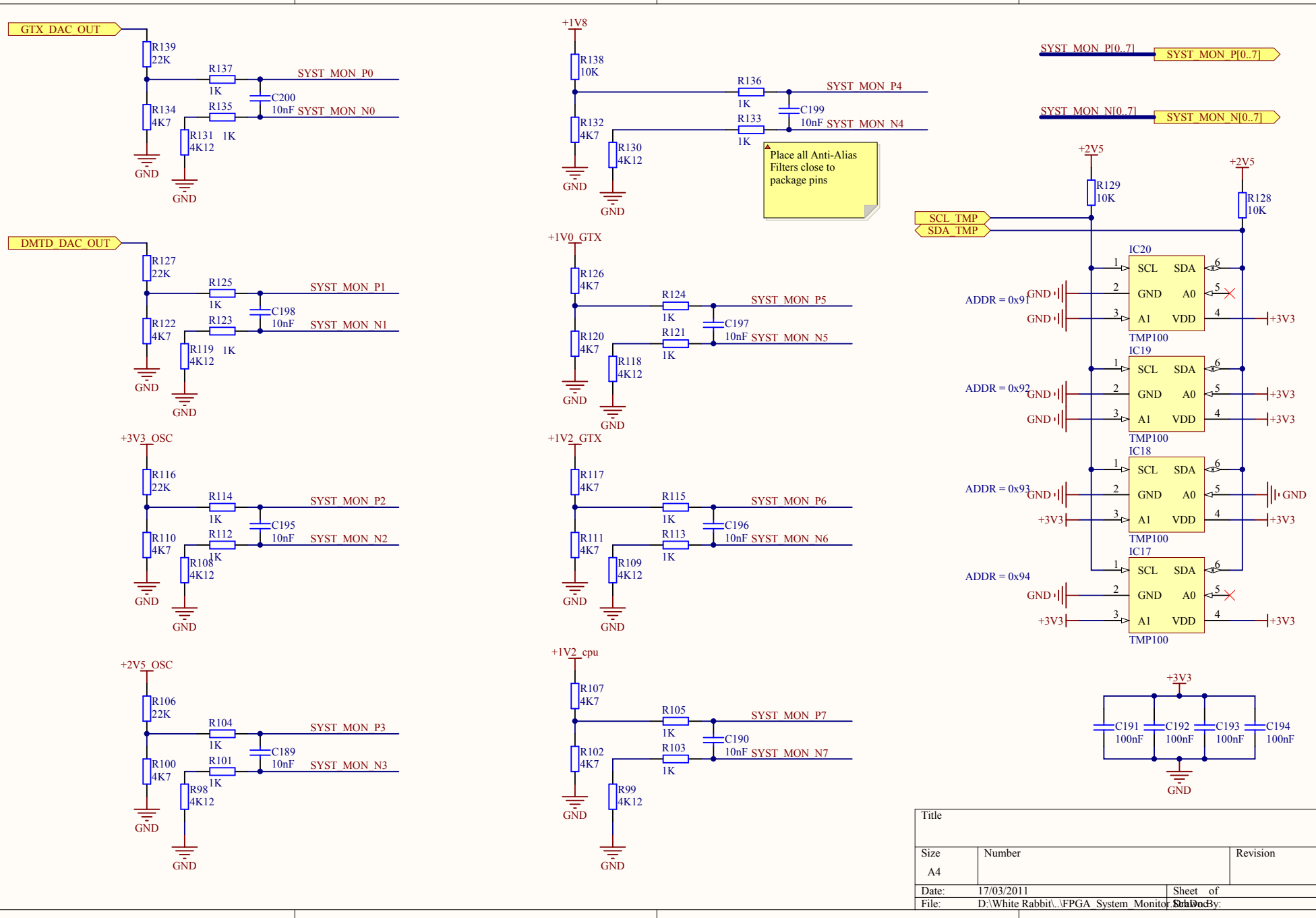
Title		
Size A4	Number	Revision
Date: 17/03/2011	Sheet of	
File: D:\White Rabbit\SCB\FPGA_GPIOs.SchDoc	Drawn By:	

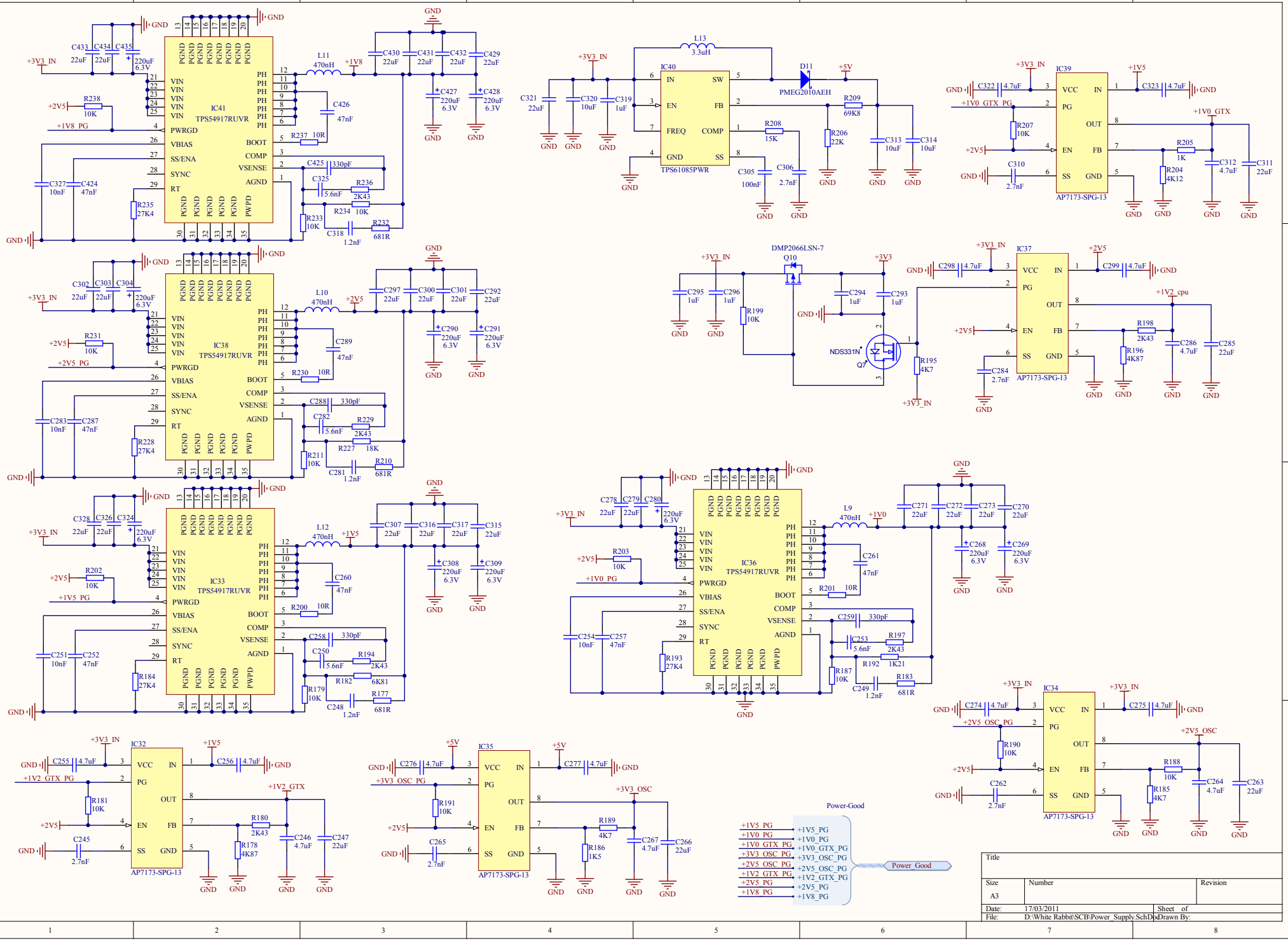

Power Supply Decoupling Capacitors
According to Xilinx UG366 (v2.3), page 230, the suggested filtering for the MGTAVCC and MGTAVTT power supplies is:
- One 0.22uF, size 0402, ceramic capacitor per power supply pin
- One 4.7uF, size 0402, ceramic capacitor per two Quads
- One 330uF bulk capacitor for each power supply
U4Q
XC6VLX130T-1FF1156C
U4R
XC6VLX130T-1FF1156C
MGTREFCLK
MGTRX112PN
MGTRX113PN
MGTRX114PN
MGTRX115PN
MGTRX116PN
MGTTX112PN
MGTTX113PN
MGTTX114PN
MGTTX115PN
MGTTX116PN
+1V0_GTX
+1V2_GTX
GND
Title
Size
A3
Number
Revision
Date: 17/03/2011
Sheet of
File: D:\White Rabbit\SCB\FPGA_GTX.SchDoc
Drawn By:

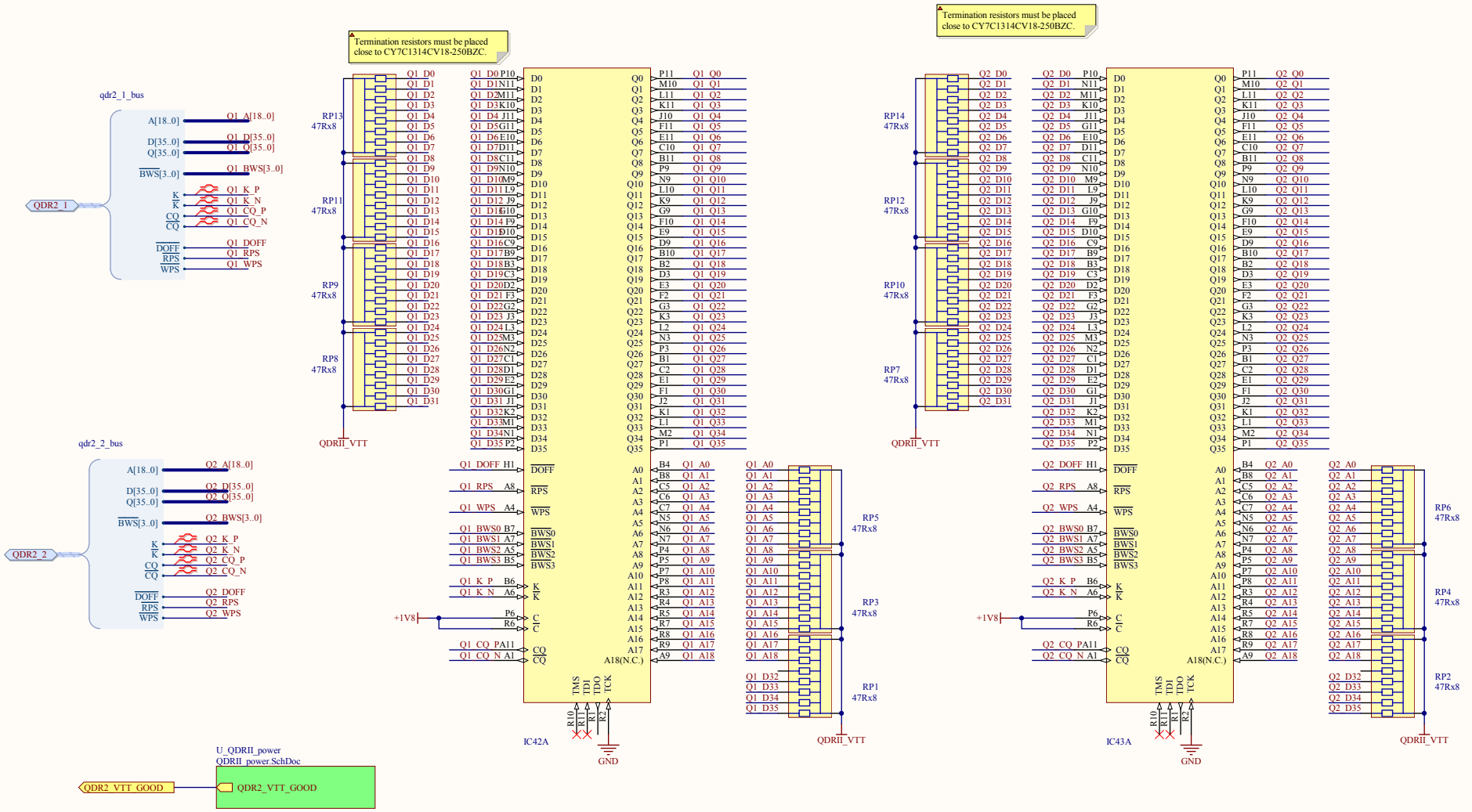

IC16A
AD9516-1BCPZ
REFIN (REF2)
REFIN (REF1)
CLK
CLK
CPRSET
RSET
CP
LF
BYPASS
STATUS
REF_SEL
SYNC
CS
SCLK
SDIO
SDO
REFMON
LD
RESET
PD
LVPECL
LVDS/CMOS
CLK10MHZ_EXT
CLK_25MHZ_GTX_DAC
CLK_125MHZ_EXT_P
CLK_125MHZ_EXT_N
REF_10M
MGTREFCLK
MGTREFCLK116_P
MGTREFCLK116_N
MGTREFCLK115_P
MGTREFCLK115_N
MGTREFCLK114_P
MGTREFCLK114_N
MGTREFCLK113_P
MGTREFCLK113_N
MGTREFCLK112_P
MGTREFCLK112_N
uTCA_TONGUE2_CLK1_P
uTCA_TONGUE2_CLK1_N
uTCA_TONGUE2_CLK2_P
uTCA_TONGUE2_CLK2_N
QDRII_CLK_P
QDRII_CLK_N
QDRII_200CLK_P
QDRII_200CLK_N
EXTREF125MHZOUT
PLL_CONTROL
PLL_SDI
PLL_SDO
PLL_SCLK
PLL_REFSEL
PLL_RESET
PLL_LOCK
PLL_STAT
PLL_CS
MC100EPT21DTG
125MHz Clock to FPGA GTXs (LVPECL)
According to Table 2-10 of UG366 for GigE:
Line Rate [Gb/s] = 1.25
PLL Frequency [GHz] = 2.5
REFCLK[MHz] = 125
N1 = 5
N2 = 4
D = 4
M = 1
IC16B
AD9516-1BCPZ
+3V3_OSC
+2V5_OSC
VS_DRV
GND_PAD
VCP
PAD
220R@100MHz
QDRII_CLKS
uTCA_CLK
Input = 25 MHz
Output=200MHz
PRESC DIV = 3
FB DIV = 24
OUT DIV = 3
PR[1:0] = 00
OD[2:0] = 010
IC14A
CDCM61002RHBT
LVDS OUTPUTS
CLK_25MHZ
PLL_RESET
OSC_OUT
REG_CAP1
REG_CAP2
IC14B
VCC_OUT
GND1
VCC_IN
VCC_PLL1
VCC_PLL2
VCC_VCO
200MHz QDRII CLK
(Not mounted)
Input = 25 MHz
Output=125 MHz
PRESC DIV = 4
FB DIV = 20
OUT DIV = 4
PR[1:0] = 11
OD[2:0] = 011
IC13A
IC13B
CLK_25MHZ_DMTD_DAC
DMTDCLK_MAIN_P
DMTDCLK_MAIN_N
DMTDCLK_mB_P
DMTDCLK_mB_N
125MHz Clock for the DMTD
Phase Detector in FPGA (LVDS)
Title
Size
A3
Number
Revision
Date:
17/03/2011
Sheet of
File:
D:\White Rabbit\SCB\FPGA_PLLs.SchDoc
Drawn By:


+2V5
L5
220R@100MHz
+2AV5
470nF
C87
C88
10nF
L4
220R@100MHz
GND
AGND
C84
4.7uF
C83
470nF
C85
22uF
C86
22uF
+1V8
C73
470nF
C74
4.7uF
C75
22uF
C76
22uF
U4S
VBATT_0
AVDD_0
VP_0
VREFP_0
VCCO_0
VCCO_12
VCCO_13
VCCO_14
VCCO_15
VCCO_16
VCCO_22
VCCO_23
VCCO_24
VCCO_25
VCCO_26
VCCO_32
VCCO_33
VCCO_34
VCCO_35
VCCO_36
VFS_0
AVSS_0
VN_0
VREFN_0
VCCAUX
VCCINT
XC6VLX130T-1FF1156C
Required 330uF PCB
Capacitors:
LX130T = 2
LX195T = 4
LX240T = 4
LX365T = 6
C82 330uF
C81 330uF
C80 330uF
C79 330uF
C78 330uF
C77 330uF
C72 4.7uF
C71 4.7uF
C70 470nF
C69 470nF
U4T
XC6VLX130T-1FF1156C
Title
Size
A3
Number
Revision
Date:
17/03/2011
Sheet of
File:
D:\White Rabbit\..\FPGA_POWER_DGND.SchDoc
Drawn By:

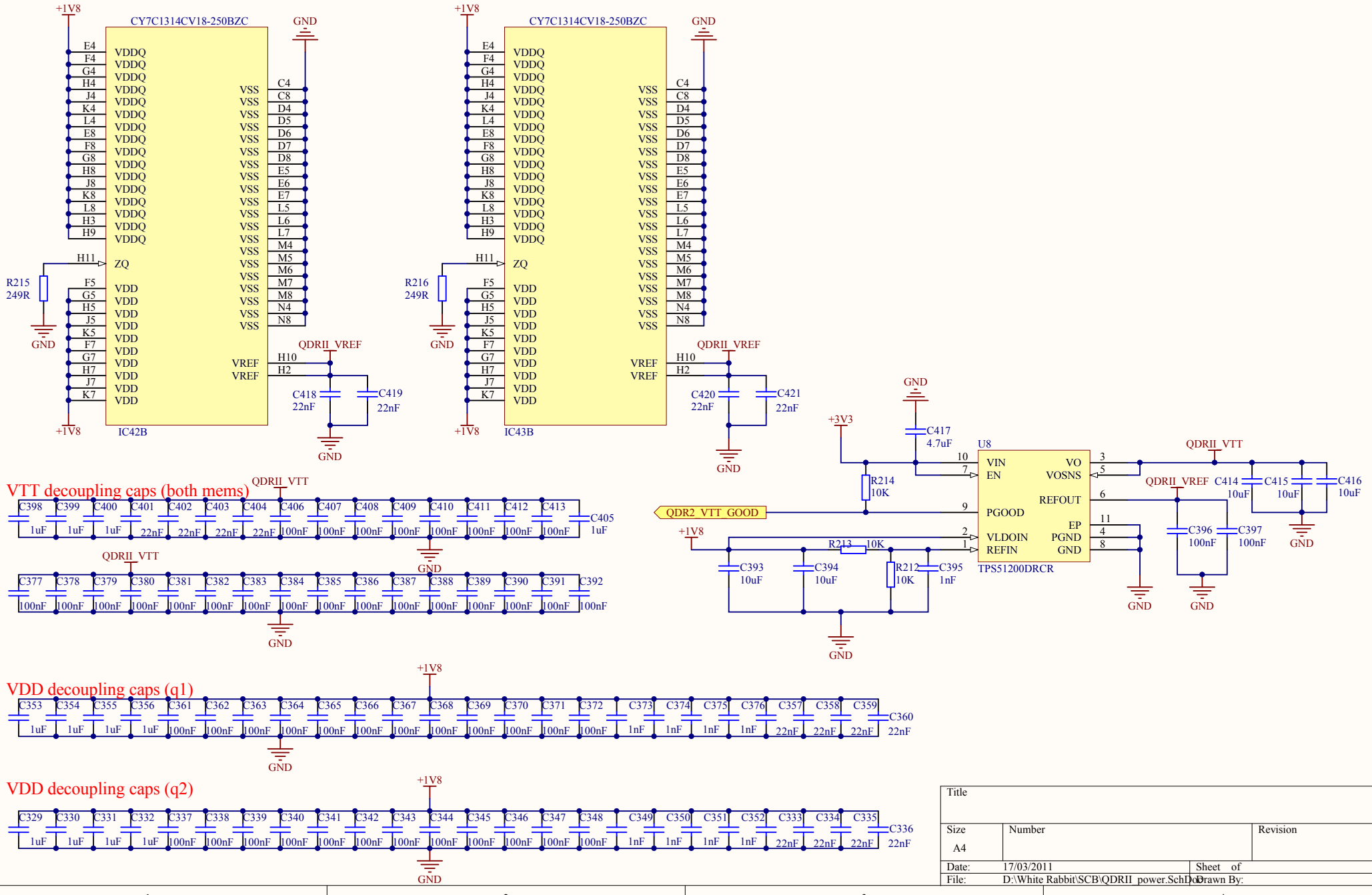

U4I
BANK 25
XC6VLX130T-1FF1156C
U4J
BANK 26
XC6VLX130T-1FF1156C
U4K
BANK 32
XC6VLX130T-1FF1156C
U4L
BANK 33
XC6VLX130T-1FF1156C
qdr2_2_bus
QDR2_2
qdr2_1_bus
QDR2_1
QDRII_VREF
VREFQDRII
SYST_MON_P[0..7]
SYST_MON_N[0..7]
U4O
BANK 36
XC6VLX130T-1FF1156C
U4N
BANK 35
XC6VLX130T-1FF1156C
U4G
BANK 23
XC6VLX130T-1FF1156C
U4F
BANK 22
XC6VLX130T-1FF1156C
+1V8
GND
Only 1.8V single-ended or differential clocks allowed.
Title
Size
A3
Number
Revision
Date: 17/03/2011
Sheet of
File: D:\White Rabbit\SCB\FPGA_QDRII.SchDoc
Drawn By:


GTX_DAC_OUT
R139 22K
R137 1K
SYST_MON_P0
C200 10nF
R134 4K7
R135 1K
SYST_MON_N0
R131 4K12
GND
DMTD_DAC_OUT
R127 22K
R125 1K
SYST_MON_P1
C198 10nF
R122 4K7
R123 1K
SYST_MON_N1
R119 4K12
+3V3_OSC
R116 22K
R114 1K
SYST_MON_P2
C195 10nF
R110 4K7
R112 1K
SYST_MON_N2
R108 4K12
+2V5_OSC
R106 22K
R104 1K
SYST_MON_P3
C189 10nF
R100 4K7
R101 1K
SYST_MON_N3
R98 4K12
+1V8
R138 10K
R136 1K
SYST_MON_P4
C199 10nF
R132 4K7
R133 1K
SYST_MON_N4
R130 4K12
Place all Anti-Alias Filters close to package pins
+1V0_GTX
R126 4K7
R124 1K
SYST_MON_P5
C197 10nF
R120 4K7
R121 1K
SYST_MON_N5
R118 4K12
+1V2_GTX
R117 4K7
R115 1K
SYST_MON_P6
C196 10nF
R111 4K7
R113 1K
SYST_MON_N6
R109 4K12
+1V2_cpu
R107 4K7
R105 1K
SYST_MON_P7
C190 10nF
R102 4K7
R103 1K
SYST_MON_N7
R99 4K12
SYST_MON_P[0..7]
SYST_MON_N[0..7]
+2V5
R129 10K
R128 10K
SCL_TMP
SDA_TMP
IC20
IC19
IC18
IC17
SCL
SDA
GND
A0
A1
VDD
TMP100
ADDR = 0x91
ADDR = 0x92
ADDR = 0x93
ADDR = 0x94
+3V3
C191 100nF
C192 100nF
C193 100nF
C194 100nF
Title
Size A4
Number
Revision
Date: 17/03/2011
Sheet of
File: D:\White Rabbit\..\FPGA_System_Monitor.SchDoc
Drawn By:


IC41
TPS54917RUVR
IC38
TPS54917RUVR
IC33
TPS54917RUVR
IC36
TPS54917RUVR
IC40
TPS61085PWR
IC39
AP7173-SPG-13
IC37
AP7173-SPG-13
IC34
AP7173-SPG-13
IC32
AP7173-SPG-13
IC35
AP7173-SPG-13
Q10
DMP2066LSN-7
Q7
NDS331N
D11
PMEG2010AEH
L13
3.3uH
L11
470nH
L10
470nH
L12
470nH
L9
470nH
+3V3_IN
+1V8
+2V5
+1V5
+1V0
+5V
+3V3
+1V0_GTX
+1V2_cpu
+1V2_GTX
+3V3_OSC
+2V5_OSC
GND
Power-Good
+1V5_PG
+1V0_PG
+1V0_GTX_PG
+3V3_OSC_PG
+2V5_OSC_PG
+1V2_GTX_PG
+2V5_PG
+1V8_PG
Power_Good
Title
Size
A3
Number
Revision
Date:
17/03/2011
Sheet of
File:
D:\White Rabbit\SCB\Power_Supply.SchDoc
Drawn By:



Title		
Size: A3	Number	Revision
Date: 17/03/2011	Sheet of	
File: D:\White Rabbit\SCB\QDRII_mem.SchDoc	Drawn By:	


CY7C1314CV18-250BZC
IC42B
IC43B
+1V8
GND
R215 249R
R216 249R
QDRII_VREF
C418 22nF
C419 22nF
C420 22nF
C421 22nF
VTT decoupling caps (both mems)
QDRII_VTT
C398 C399 C400 C401 C402 C403 C404 C406 C407 C408 C409 C410 C411 C412 C413 C405
1uF 1uF 1uF 22nF 22nF 22nF 22nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 1uF
C377 C378 C379 C380 C381 C382 C383 C384 C385 C386 C387 C388 C389 C390 C391 C392
100nF
+3V3
C417 4.7uF
U8
VIN
EN
PGOOD
VLDOIN
REFIN
VO
VOSNS
REFOUT
EP
PGND
GND
TPS51200DRCR
R214 10K
R213 10K
R212 10K
QDR2_VTT_GOOD
C393 10uF
C394 10uF
C395 1nF
C414 10uF
C415 10uF
C416 10uF
C396 100nF
C397 100nF
VDD decoupling caps (q1)
C353 C354 C355 C356 C361 C362 C363 C364 C365 C366 C367 C368 C369 C370 C371 C372 C373 C374 C375 C376 C357 C358 C359 C360
1uF 1uF 1uF 1uF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 1nF 1nF 1nF 1nF 22nF 22nF 22nF 22nF
VDD decoupling caps (q2)
C329 C330 C331 C332 C337 C338 C339 C340 C341 C342 C343 C344 C345 C346 C347 C348 C349 C350 C351 C352 C333 C334 C335 C336
1uF 1uF 1uF 1uF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 1nF 1nF 1nF 1nF 22nF 22nF 22nF 22nF
Title
Size A4
Number
Revision
Date: 17/03/2011
Sheet of
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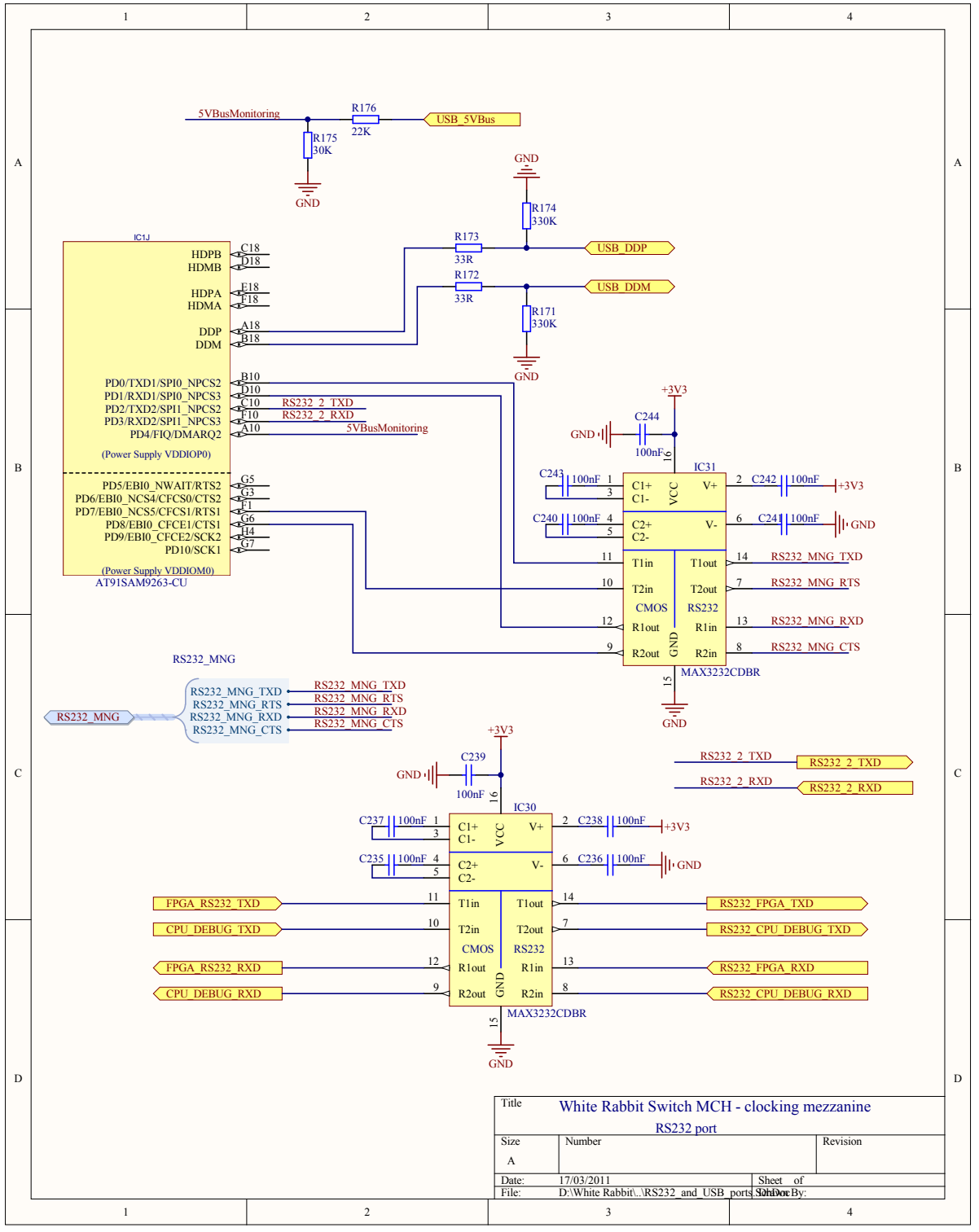
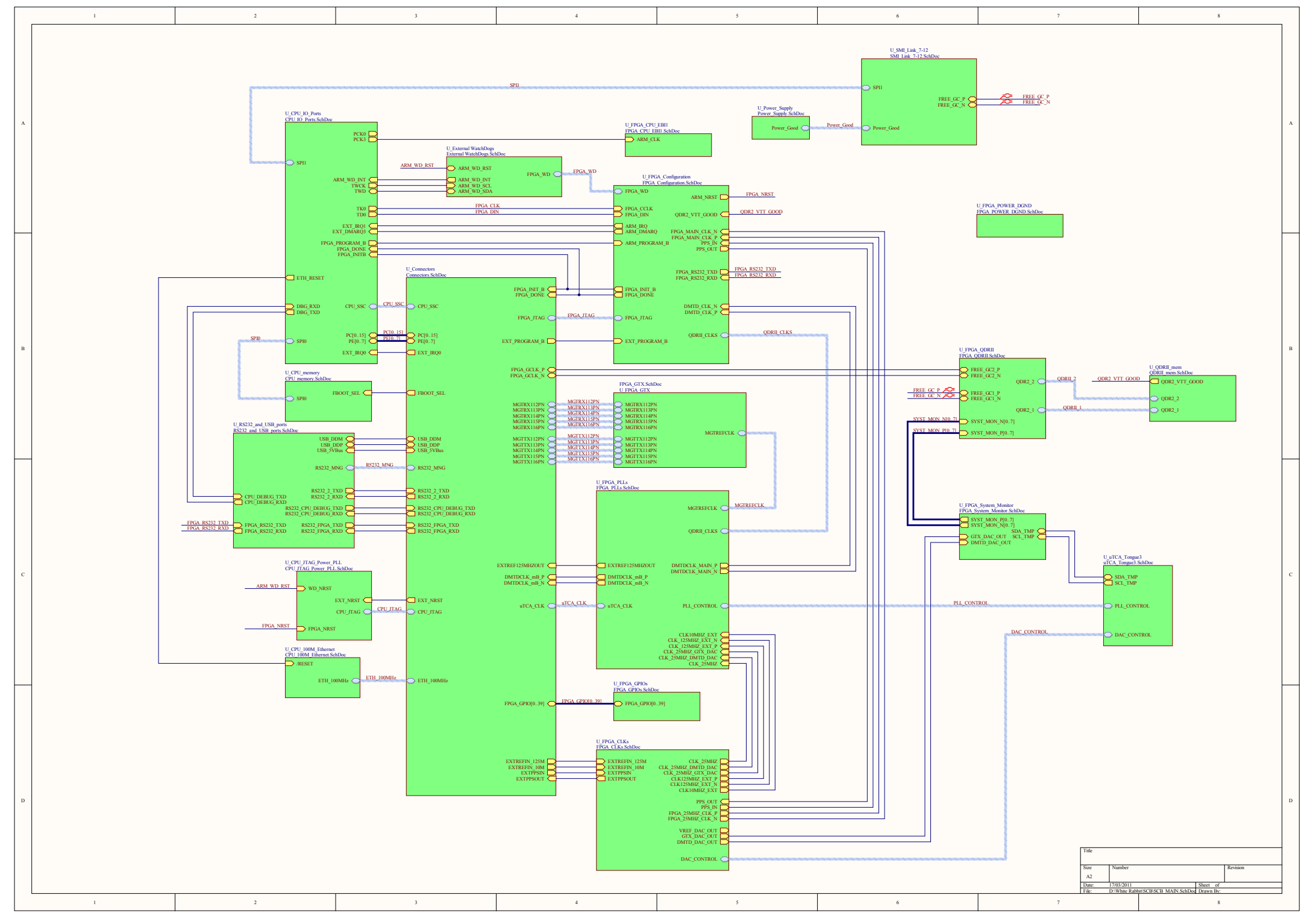
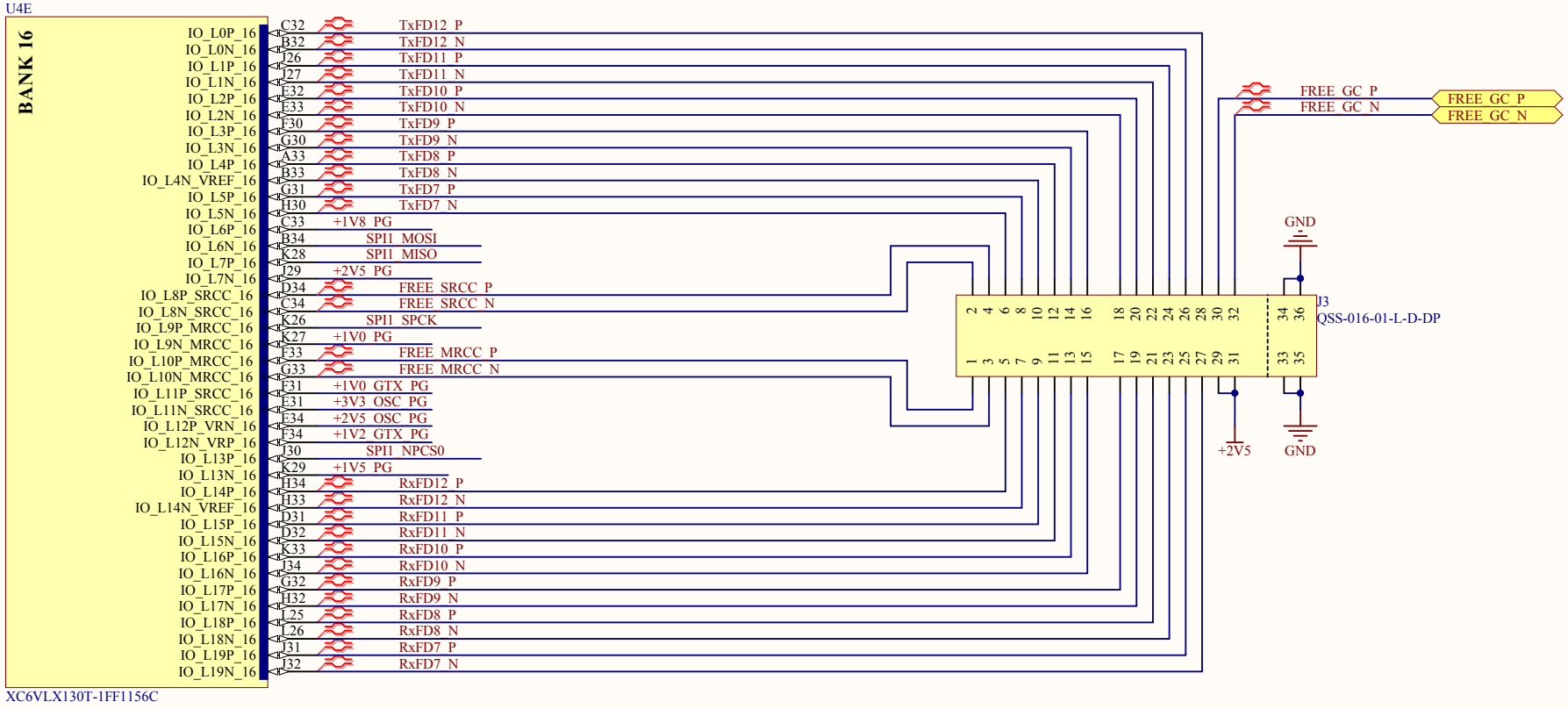
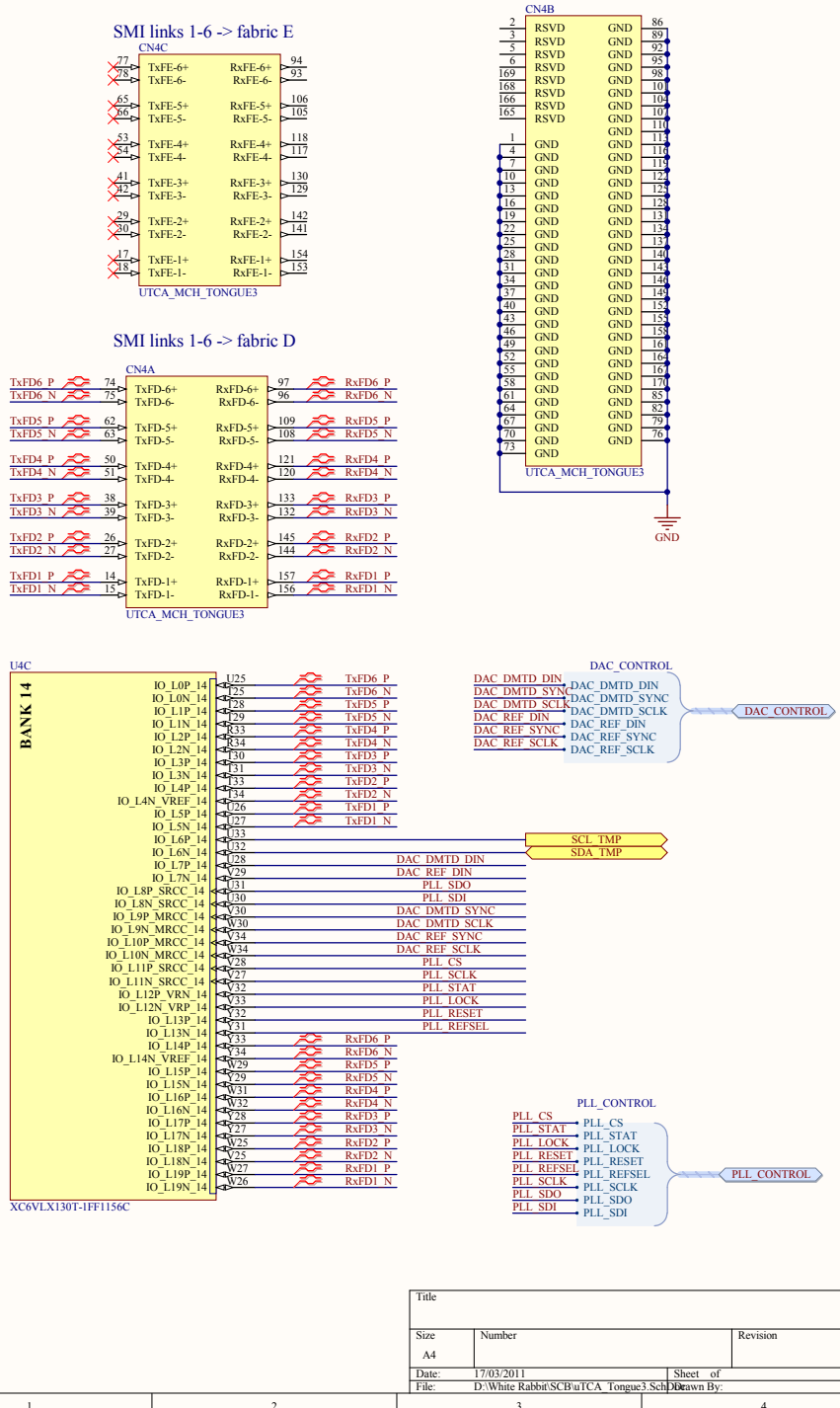


Title	White Rabbit Switch MCH - clocking mezzanine RS232 port	
Size: A	Number	Revision
Date: 17/03/2011	Sheet of	
File: D:\White Rabbit\..\RS232_and_USB_ports.SchDoc	Drawn By:	


U_SMI_Link_7-12
SMI_Link_7-12.SchDoc
SPI1
FREE_GC_P
FREE_GC_N
U_Power_Supply
Power_Supply.SchDoc
Power_Good
U_CPU_IO_Ports
CPU_IO_Ports.SchDoc
PCK0
PCK3
SPI1
ARM_WD_INT
TWCK
TWD
TK0
TD0
EXT_IRQ1
EXT_DMARQ3
FPGA_PROGRAM_B
FPGA_DONE
FPGA_INITB
ETH_RESET
DBG_RXD
DBG_TXD
CPU_SSC
PC[0..15]
PE[0..7]
SPI0
EXT_IRQ0
U_FPGA_CPU_EBI1
FPGA_CPU_EBI1.SchDoc
ARM_CLK
U_External WatchDogs
External WatchDogs.SchDoc
ARM_WD_RST
FPGA_WD
U_FPGA_Configuration
FPGA_Configuration.SchDoc
FPGA_CLK
FPGA_DIN
ARM_IRQ
ARM_DMARQ
ARM_PROGRAM_B
ARM_NRST
FPGA_NRST
QDR2_VTT_GOOD
FPGA_MAIN_CLK_N
FPGA_MAIN_CLK_P
PPS_IN
PPS_OUT
FPGA_RS232_TXD
FPGA_RS232_RXD
DMTD_CLK_N
DMTD_CLK_P
QDRII_CLKS
U_FPGA_POWER_DGND
FPGA_POWER_DGND.SchDoc
U_Connectors
Connectors.SchDoc
FPGA_INIT_B
FPGA_DONE
FPGA_JTAG
EXT_PROGRAM_B
U_CPU_memory
CPU_memory.SchDoc
FBOOT_SEL
U_FPGA_QDRII
FPGA_QDRII.SchDoc
FREE_GC2_P
FREE_GC2_N
FREE_GC1_P
FREE_GC1_N
QDR2_2
QDR2_1
SYST_MON_N[0..7]
SYST_MON_P[0..7]
U_QDRII_mem
QDRII_mem.SchDoc
QDR2_VTT_GOOD
QDR2_2
QDR2_1
QDRII_2
QDRII_1
FPGA_GTX.SchDoc
U_FPGA_GTX
MGTREFCLK
MGTRX112PN
MGTRX113PN
MGTRX114PN
MGTRX115PN
MGTRX116PN
MGTTX112PN
MGTTX113PN
MGTTX114PN
MGTTX115PN
MGTTX116PN
U_RS232_and_USB_ports
RS232_and_USB_ports.SchDoc
USB_DDM
USB_DDP
USB_5VBus
RS232_MNG
RS232_2_TXD
RS232_2_RXD
RS232_CPU_DEBUG_TXD
RS232_CPU_DEBUG_RXD
RS232_FPGA_TXD
RS232_FPGA_RXD
U_FPGA_PLLs
FPGA_PLLs.SchDoc
EXTREF125MHZOUT
DMTDCLK_mB_P
DMTDCLK_mB_N
uTCA_CLK
DMTDCLK_MAIN_P
DMTDCLK_MAIN_N
PLL_CONTROL
CLK10MHZ_EXT
CLK_125MHZ_EXT_N
CLK_125MHZ_EXT_P
CLK_25MHZ_GTX_DAC
CLK_25MHZ_DMTD_DAC
CLK_25MHZ
U_FPGA_System_Monitor
FPGA_System_Monitor.SchDoc
GTX_DAC_OUT
DMTD_DAC_OUT
SDA_TMP
SCL_TMP
U_uTCA_Tongue3
uTCA_Tongue3.SchDoc
DAC_CONTROL
U_CPU_JTAG_Power_PLL
CPU_JTAG_Power_PLL.SchDoc
WD_NRST
EXT_NRST
CPU_JTAG
U_CPU_100M_Ethernet
CPU_100M_Ethernet.SchDoc
/RESET
ETH_100MHz
U_FPGA_GPIOs
FPGA_GPIOs.SchDoc
FPGA_GPIO[0..39]
U_FPGA_CLKs
FPGA_CLKs.SchDoc
EXTREFIN_125M
EXTREFIN_10M
EXTPPSIN
EXTPPSOUT
VREF_DAC_OUT
FPGA_25MHZ_CLK_P
FPGA_25MHZ_CLK_N
Title
Size
A2
Number
Revision
Date: 17/03/2011
Sheet of
File: D:\White Rabbit\SCB\SCB_MAIN.SchDoc
Drawn By:



Title		
Size A4	Number	Revision
Date: 17/03/2011	Sheet of	
File: D:\White Rabbit\..\SMI_Link_7-12.SchDoc	Drawn By:	



Title		
Size: A4	Number	Revision
Date: 17/03/2011	Sheet of	
File: D:\White Rabbit\SCB\uTCA_Tongue3.SchDoc	Drawn By:	


Edge connector earthings