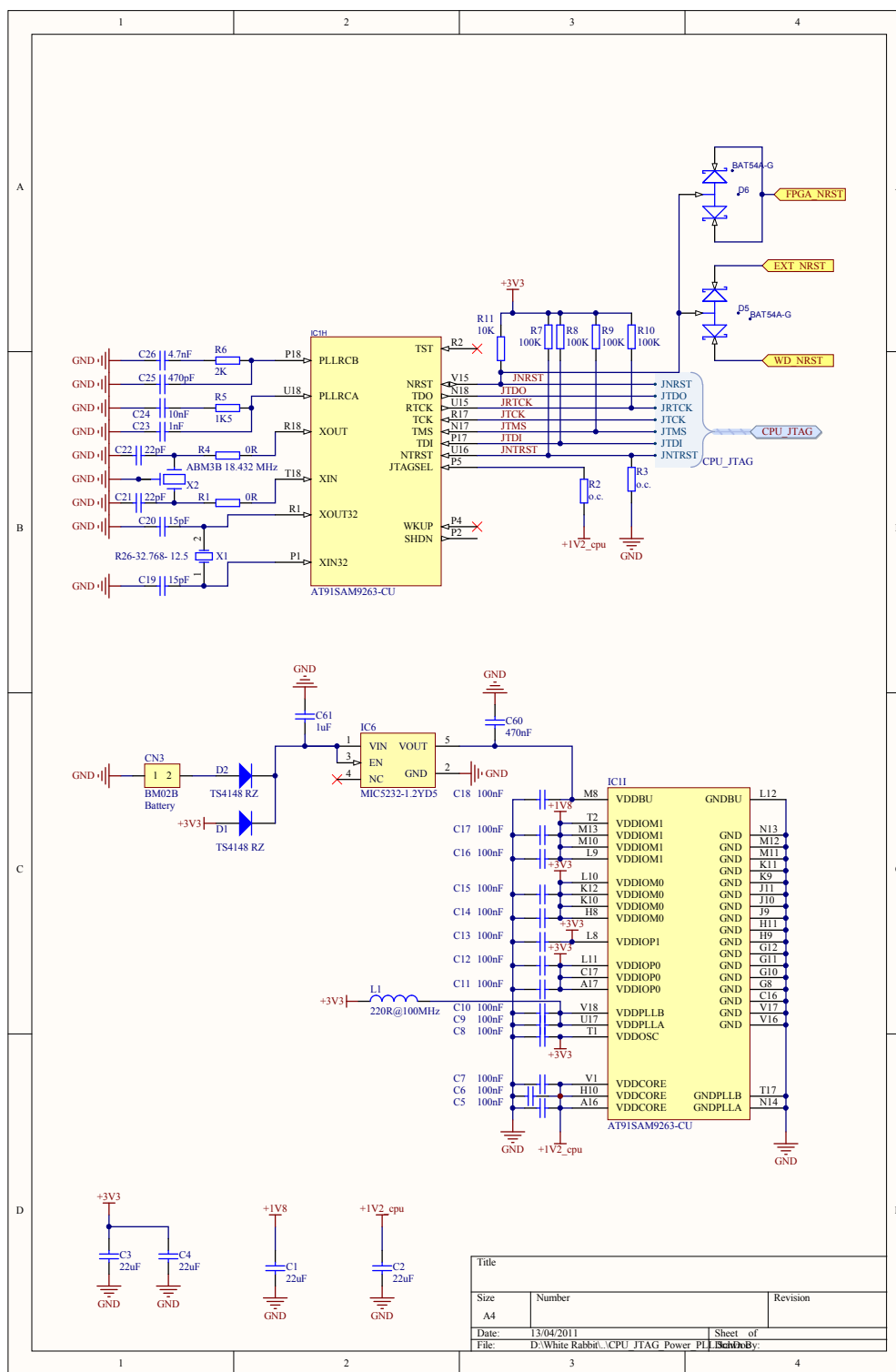
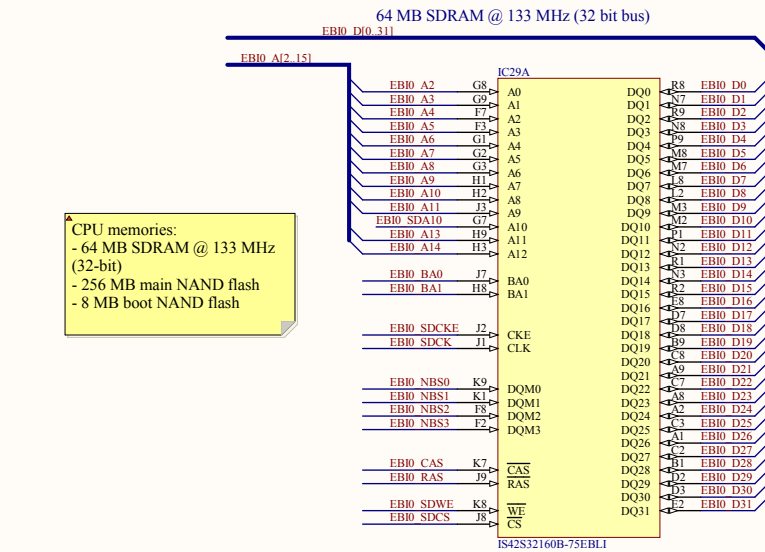
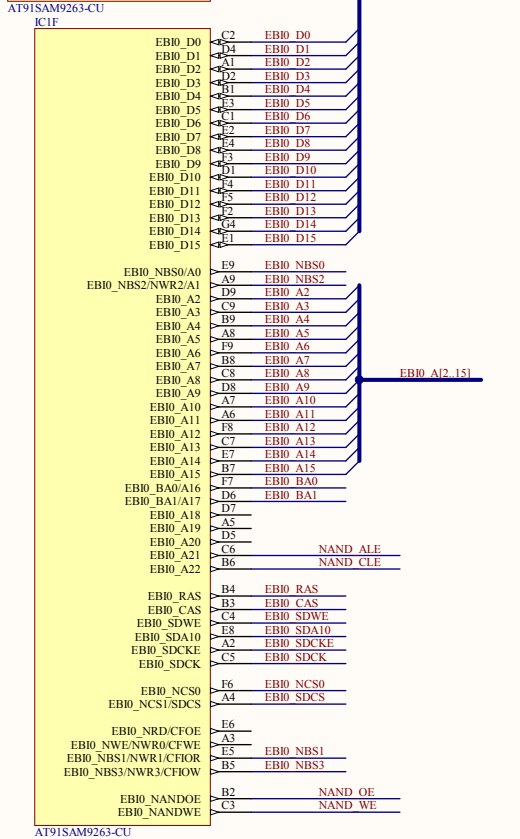
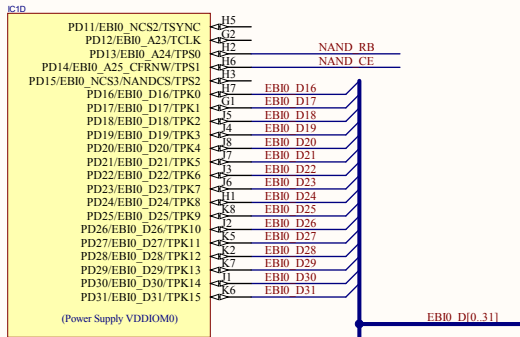


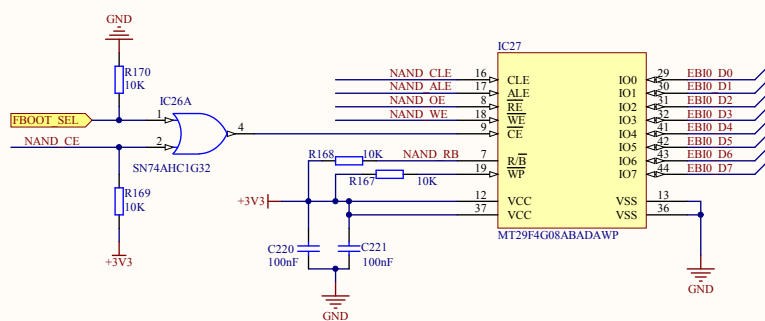
Project: White Rabbit Switch MCH - mainboard	
Sheet: ARM9 CPU I/O ports, busses and power	
Version: 1.1.0	Date: 2009/11/12
Author: Tomasz Wlostowski	License: Open Hardware License (OHL)
Company: CERN BE-CO-HT	

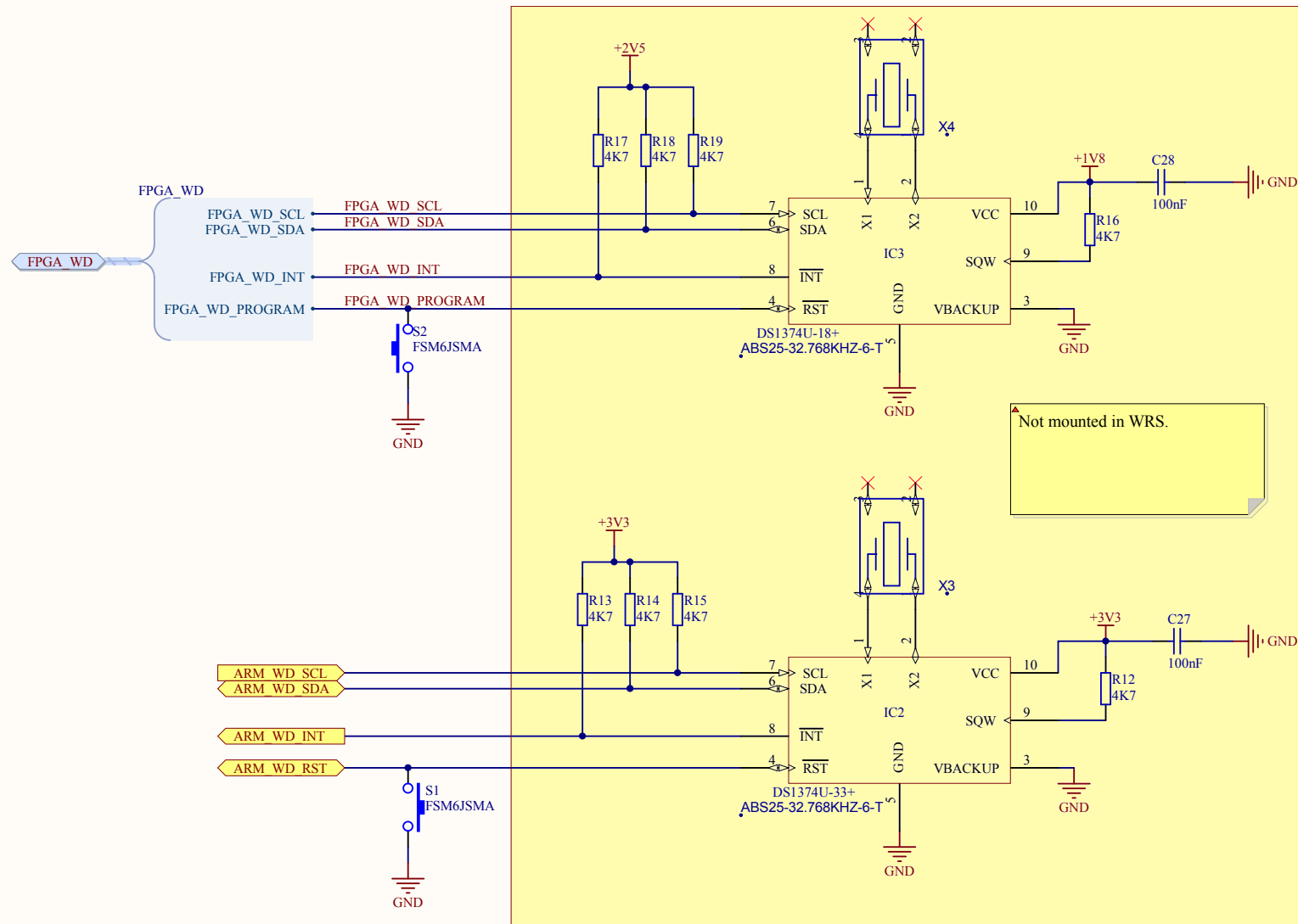


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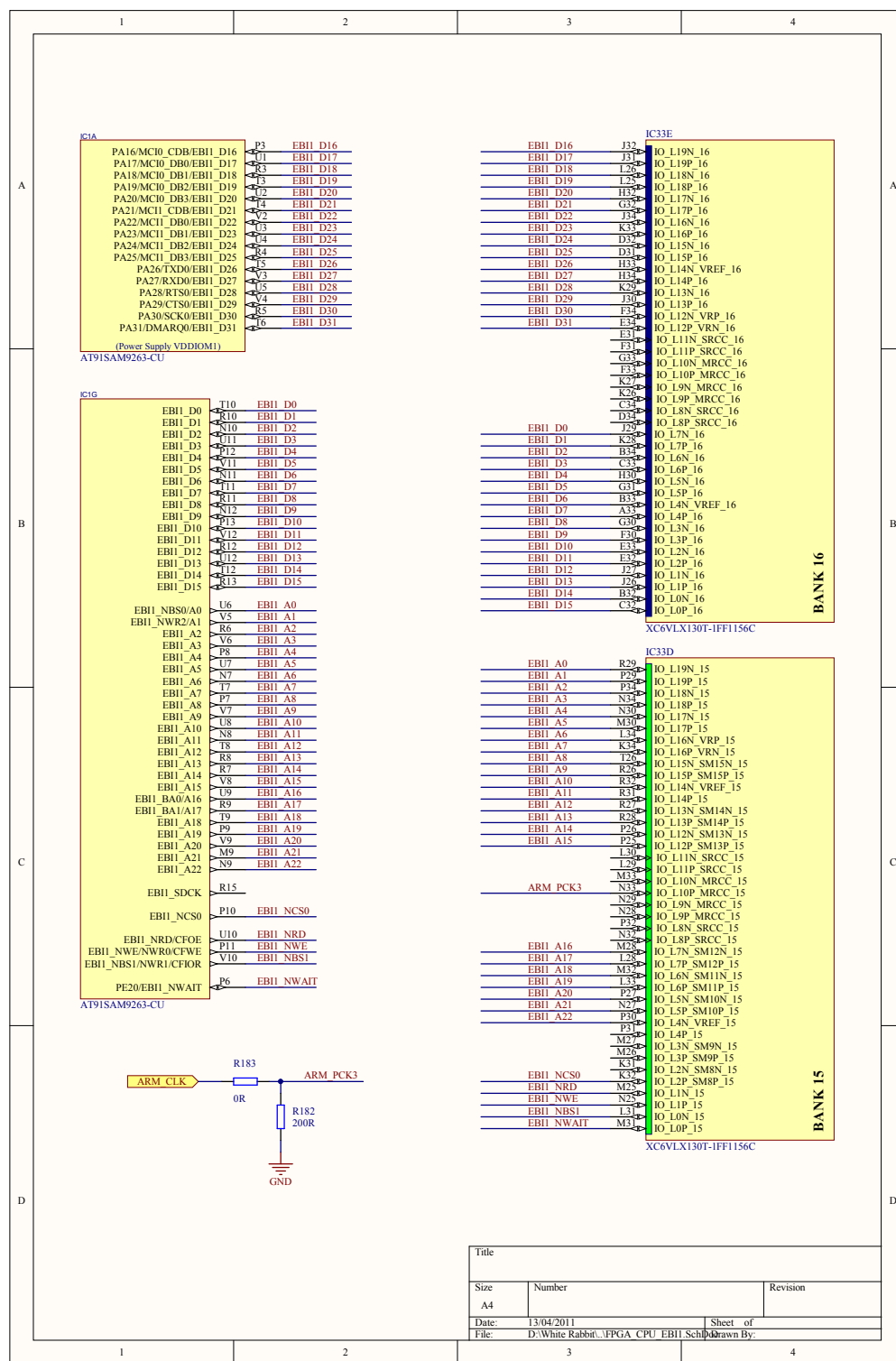


CPU memories:
- 64 MB SDRAM @ 133 MHz (32-bit)
- 256 MB main NAND flash
- 8 MB boot NAND flash



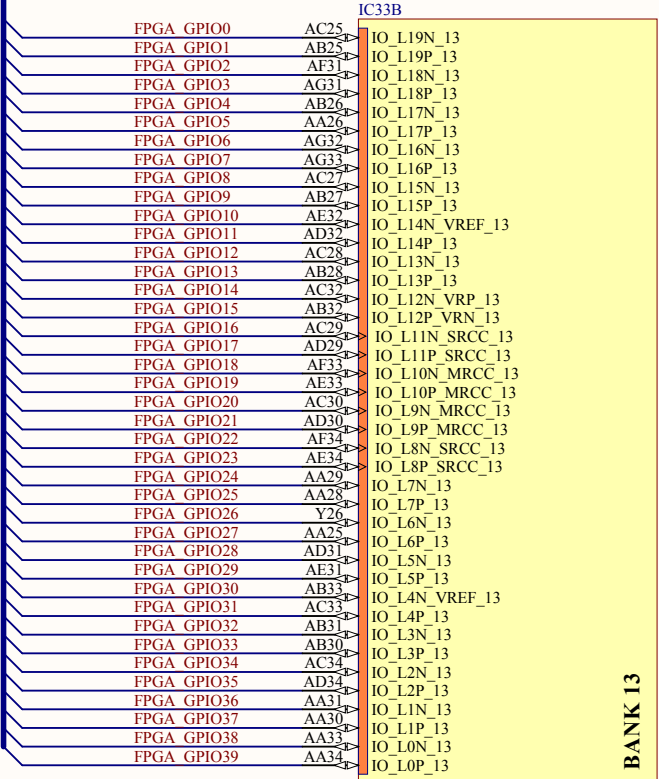


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FPGA_GPIO[0..39]

FPGA_GPIO[0..39]

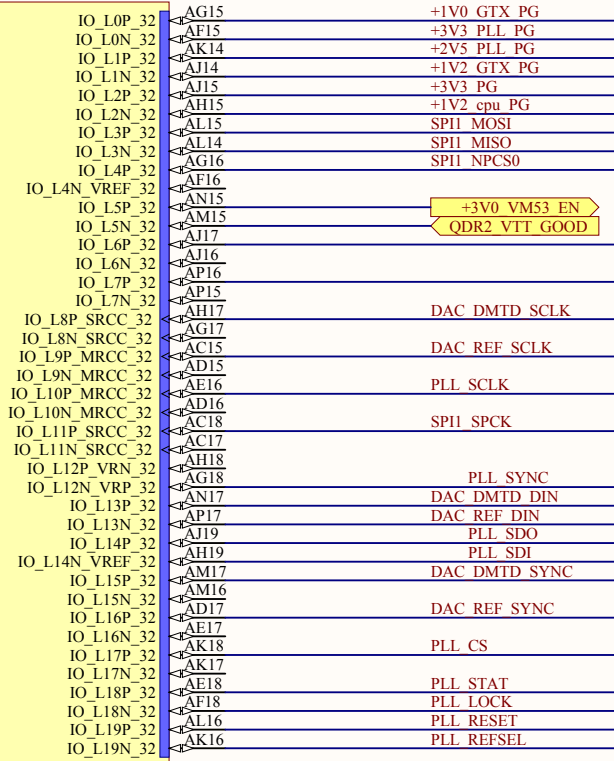


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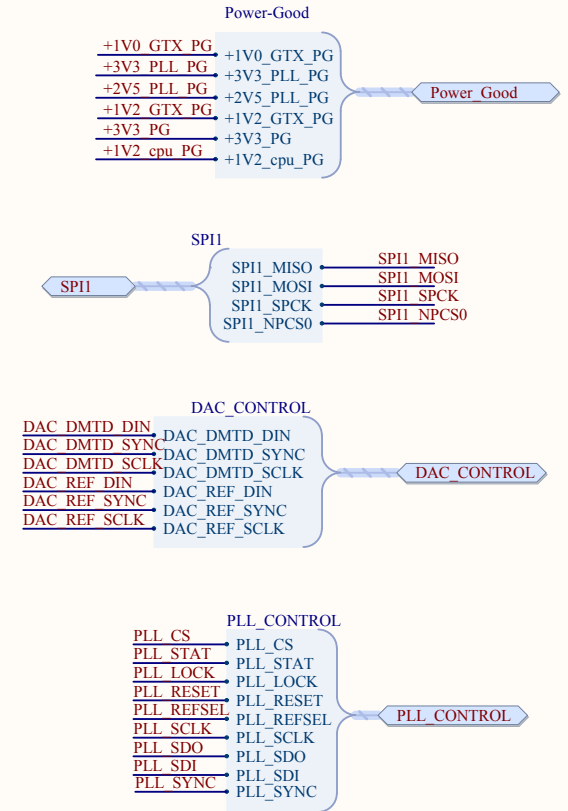
BANK 32



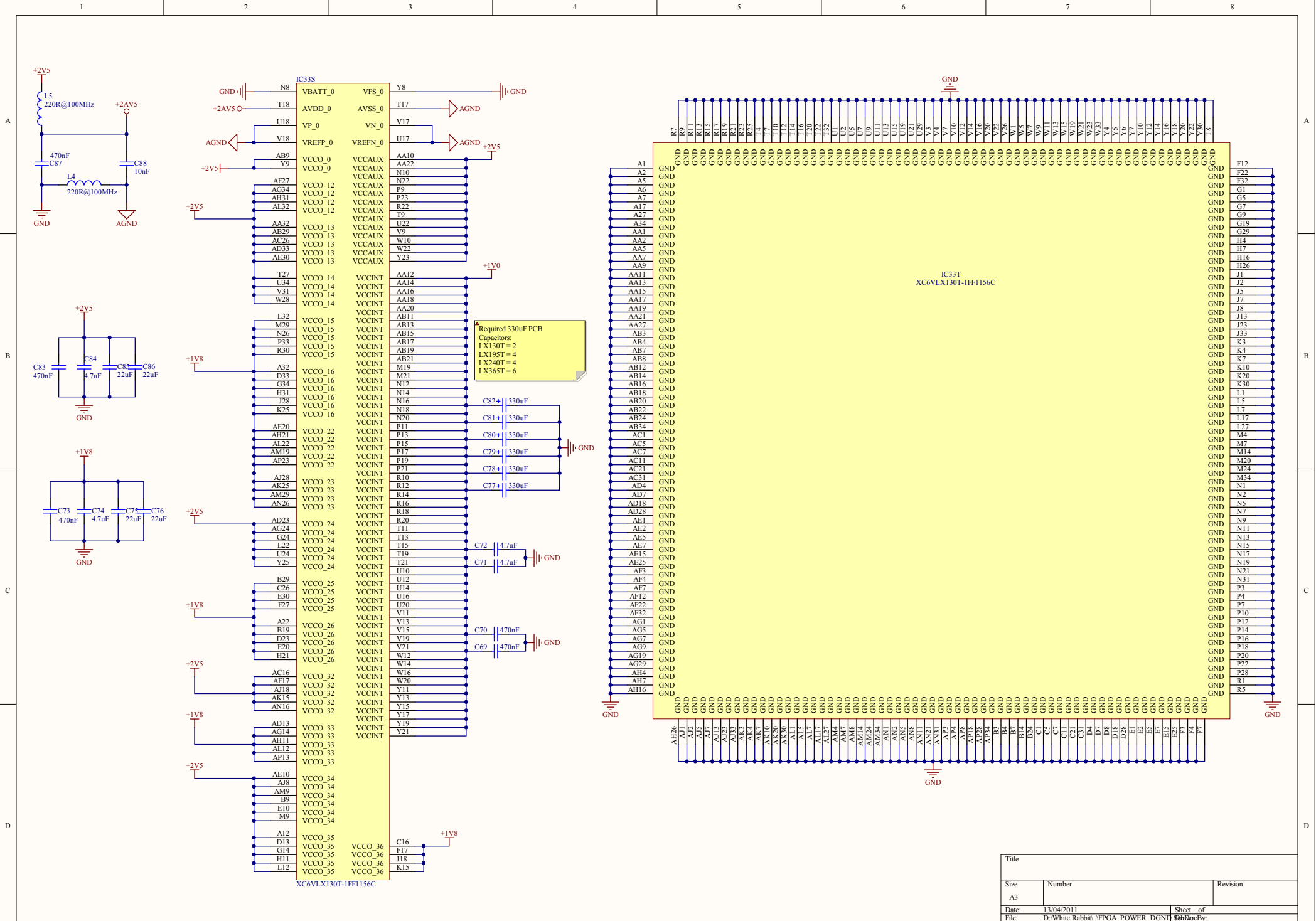
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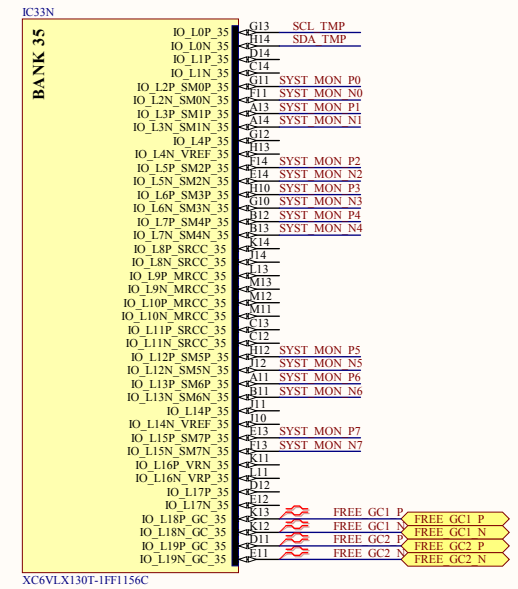
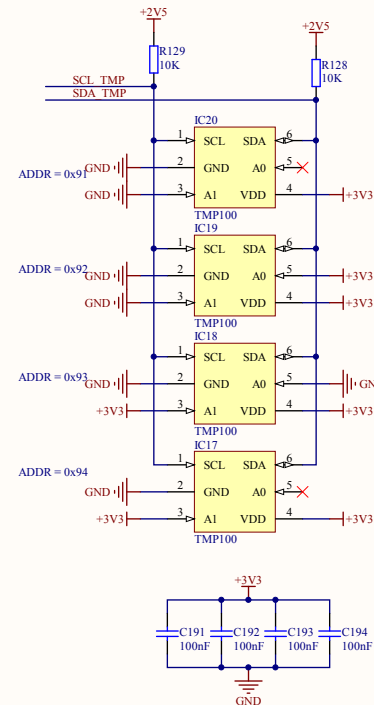
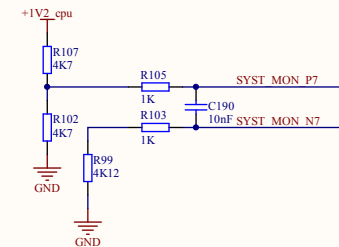
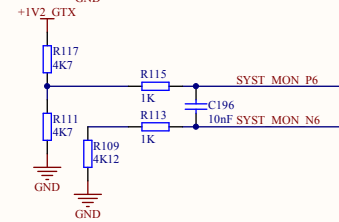
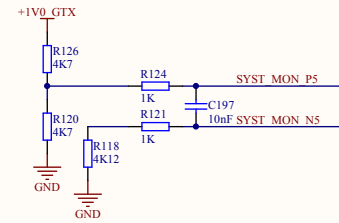
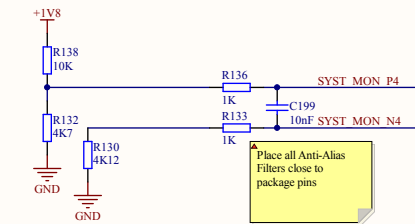
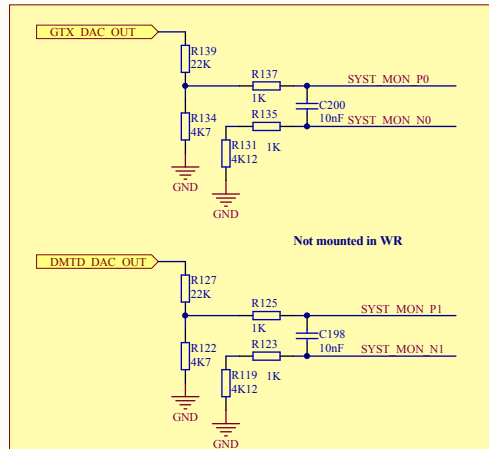
FPGA RS232 TXD
FPGA RS232 RXD



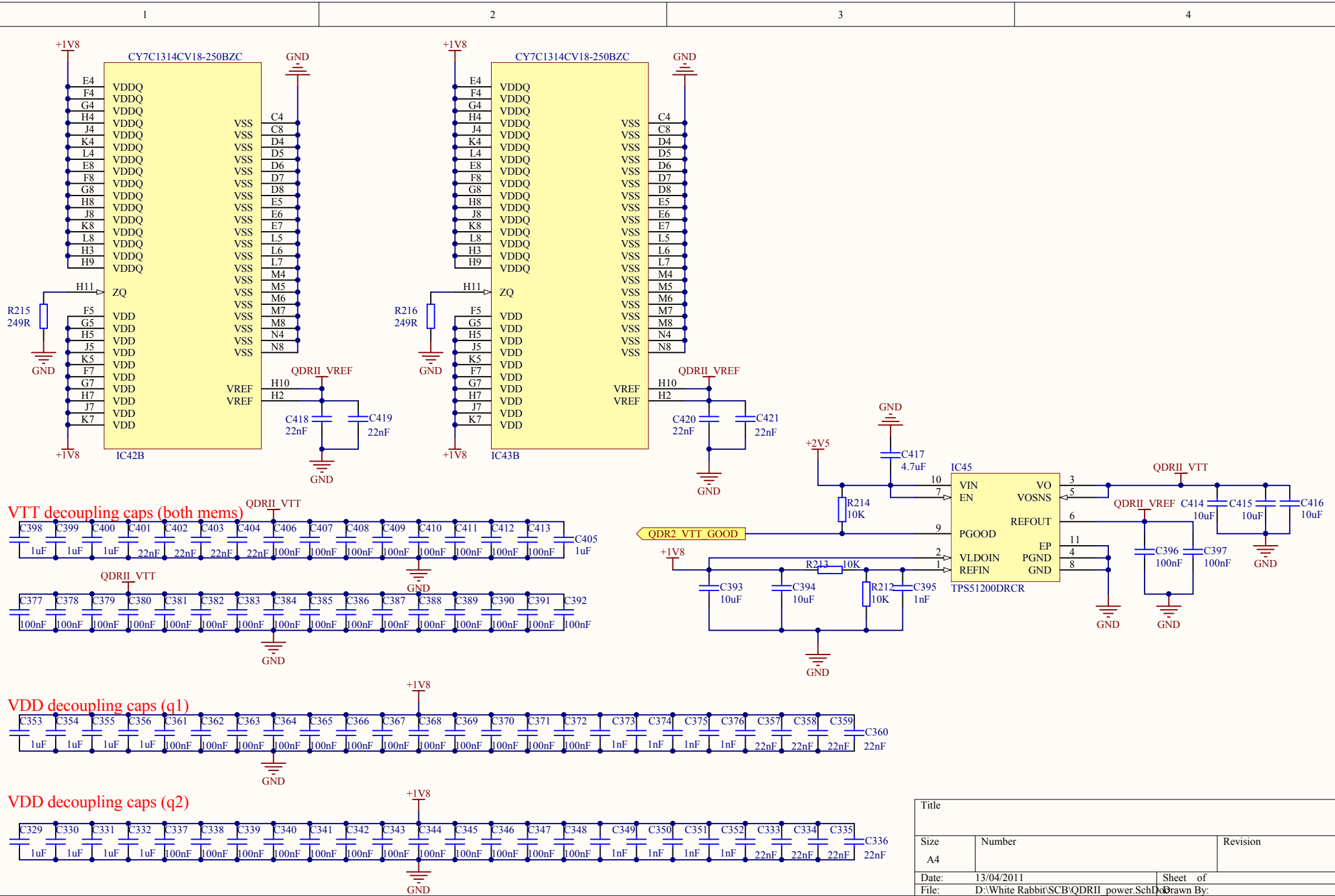
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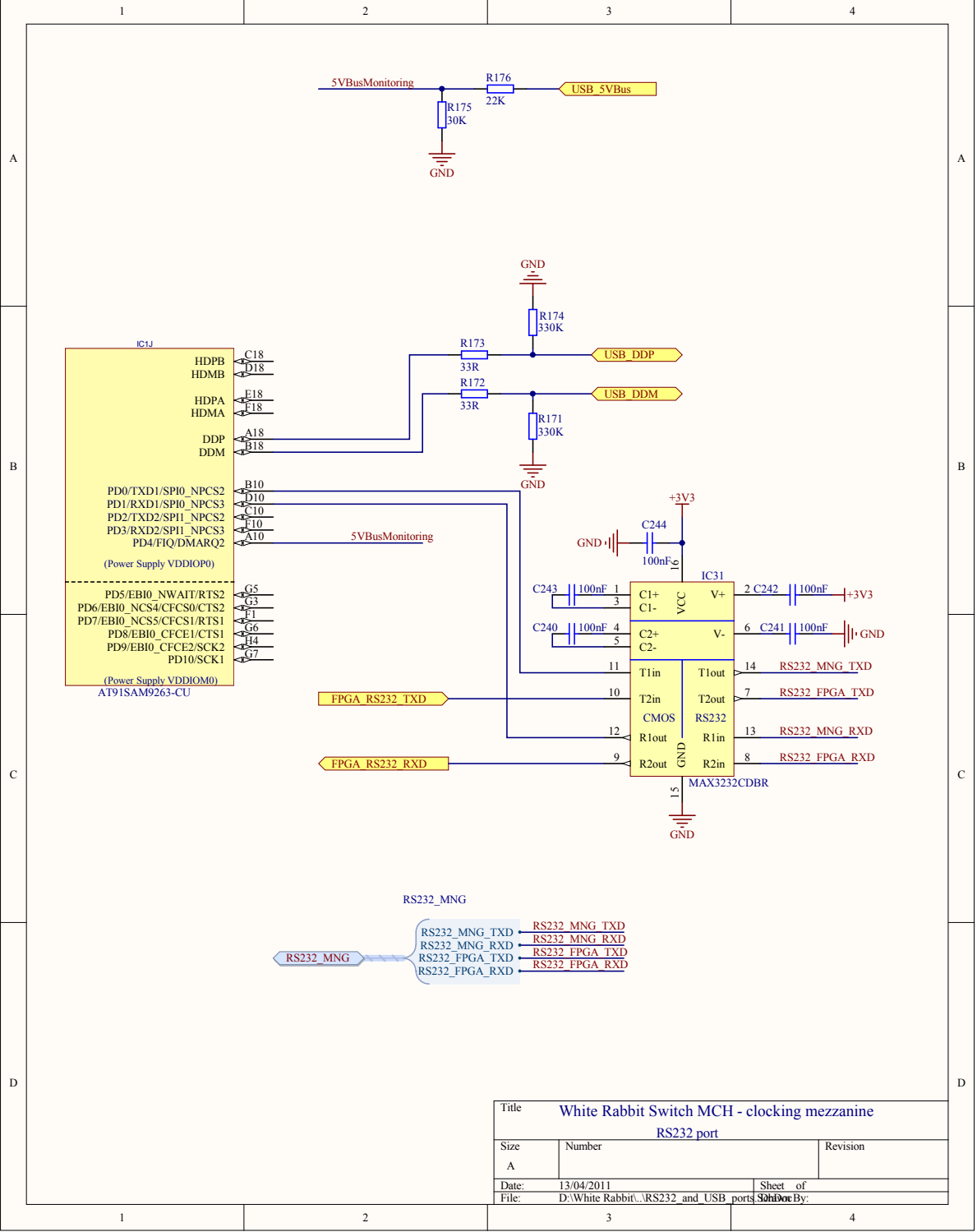
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Size	Number	Revision
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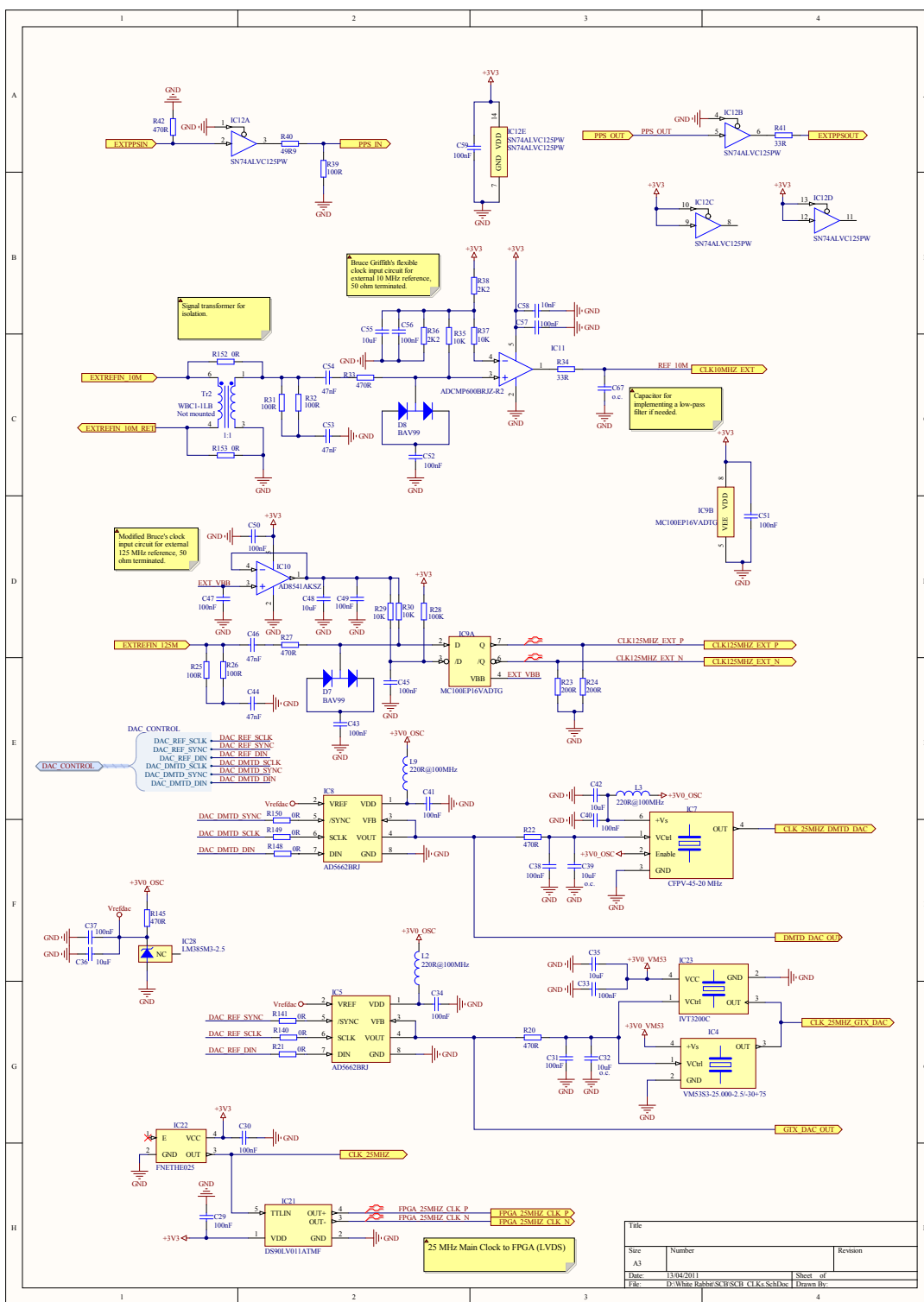
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Date: 13/04/2011	Sheet of	
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Size	Number	Revision
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Date:	13/04/2011	Sheet of
File:	D:\White Rabbit\SCB\QDRIL power.SchDoc	Drawn By:



Title		
White Rabbit Switch MCH - clocking mezzanine		
RS232 port		
Size	Number	Revision
A		
Date:	13/04/2011	Sheet of
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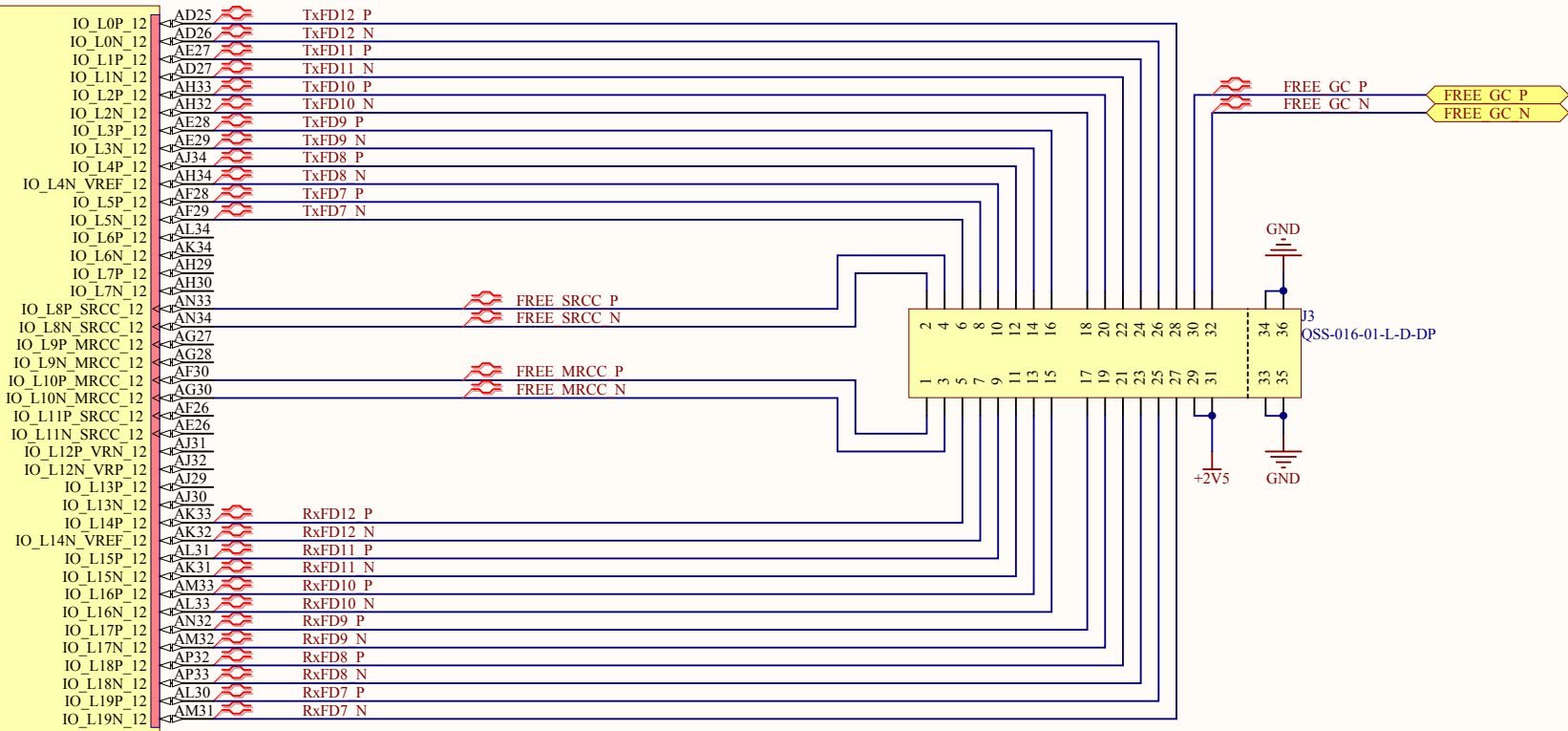


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BANK 12

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Title		
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Date:	13/04/2011	Sheet of
File:	D:\White Rabbit\SMI Link 7-12.SchDoc	Drawn By:

