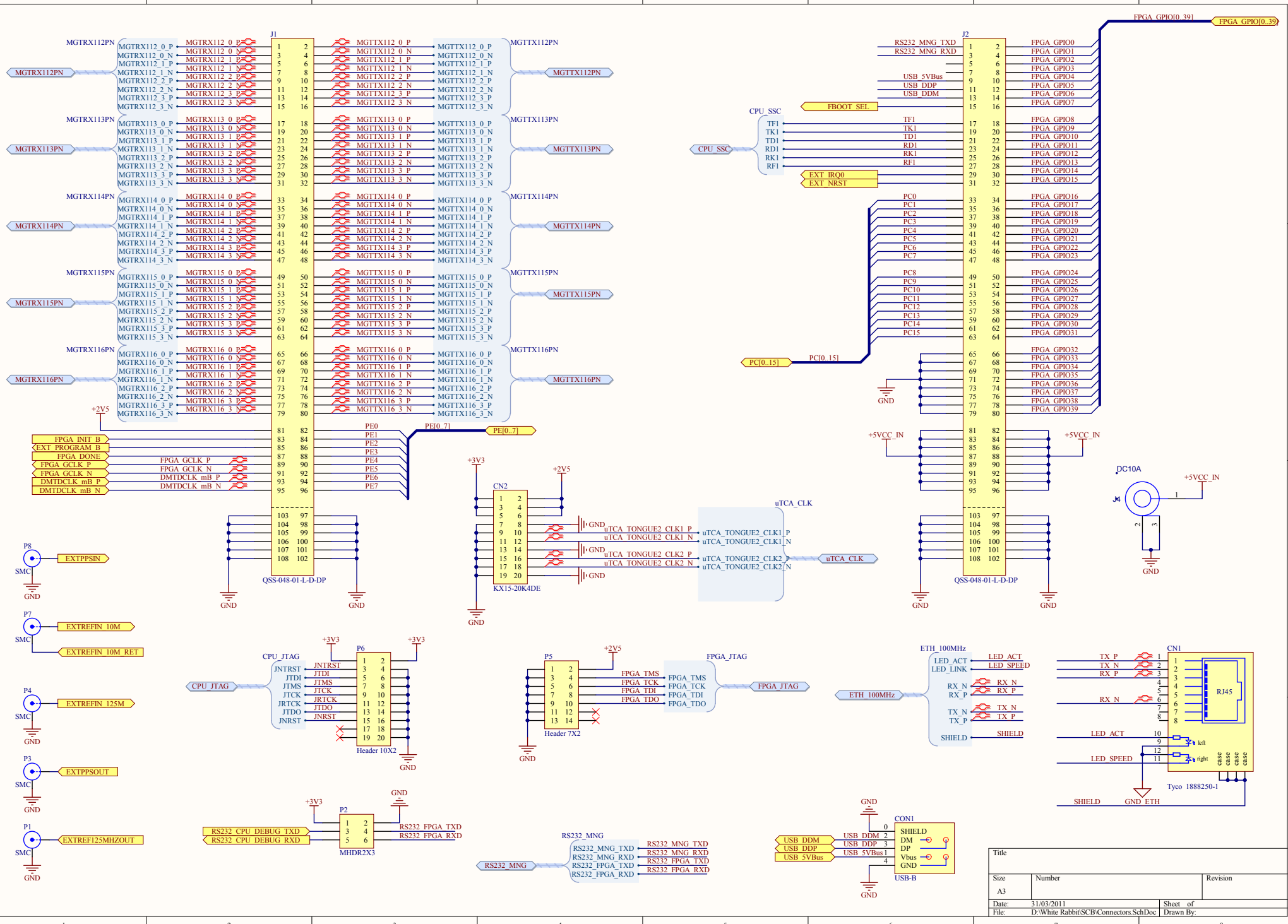
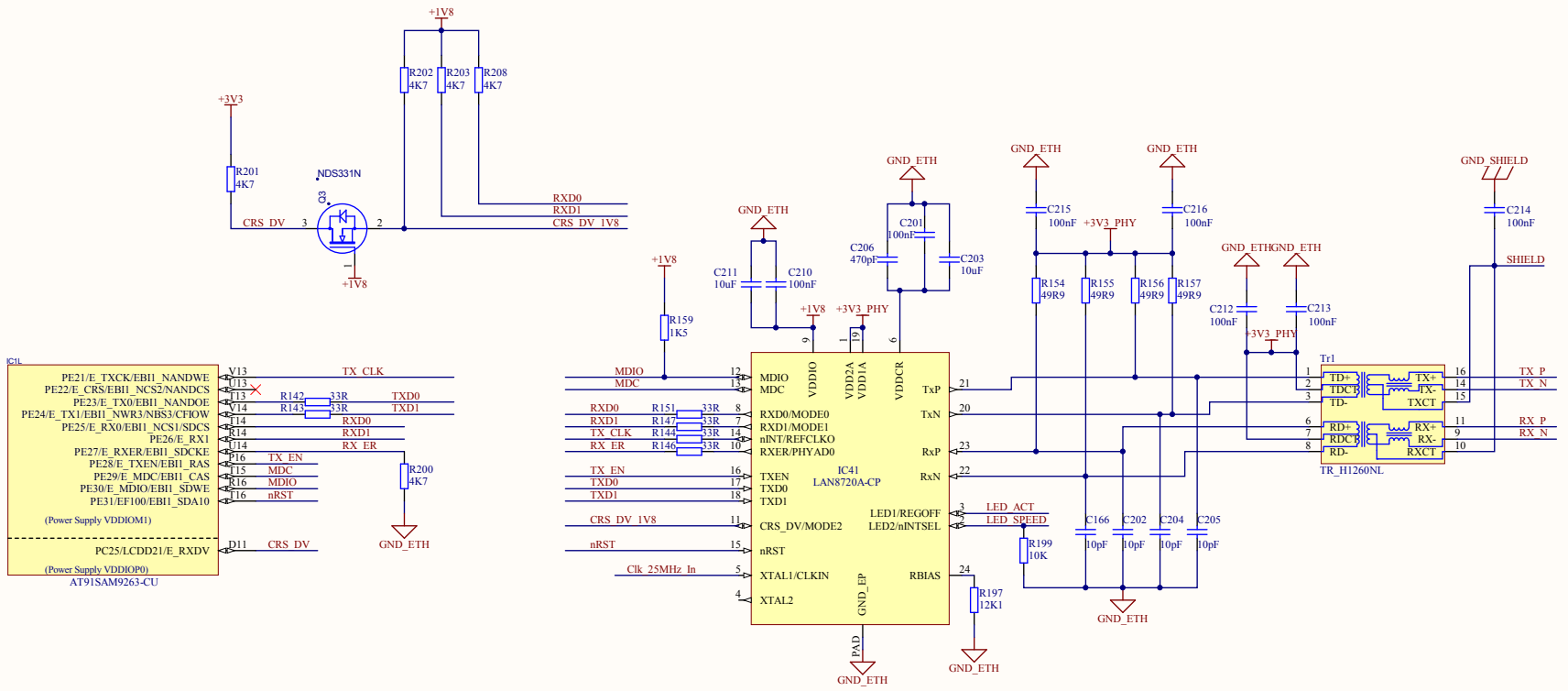
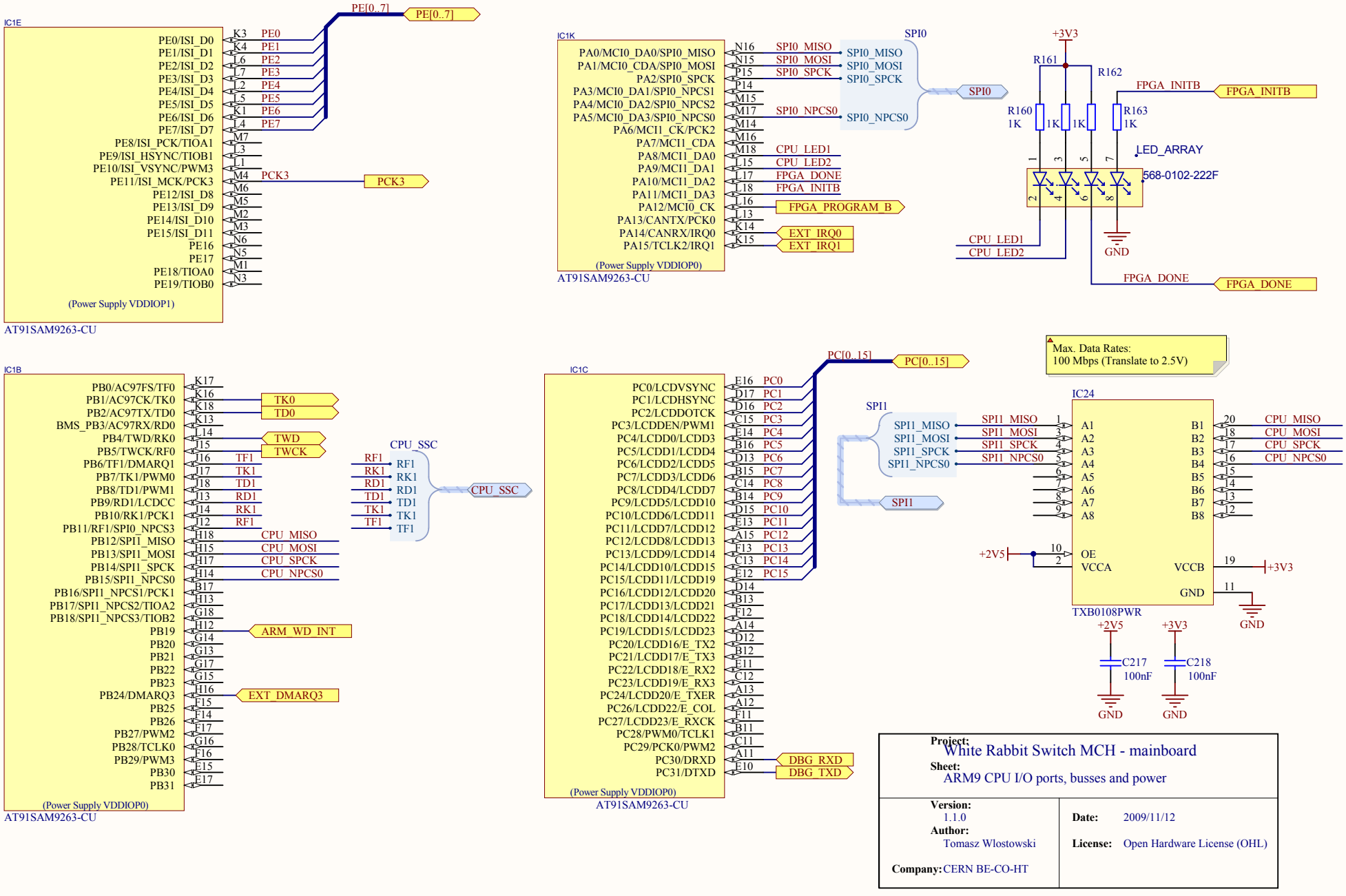
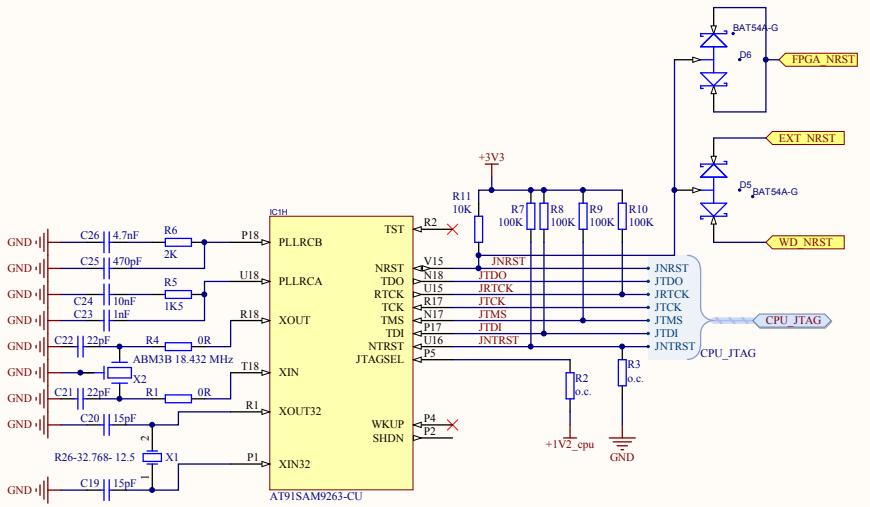
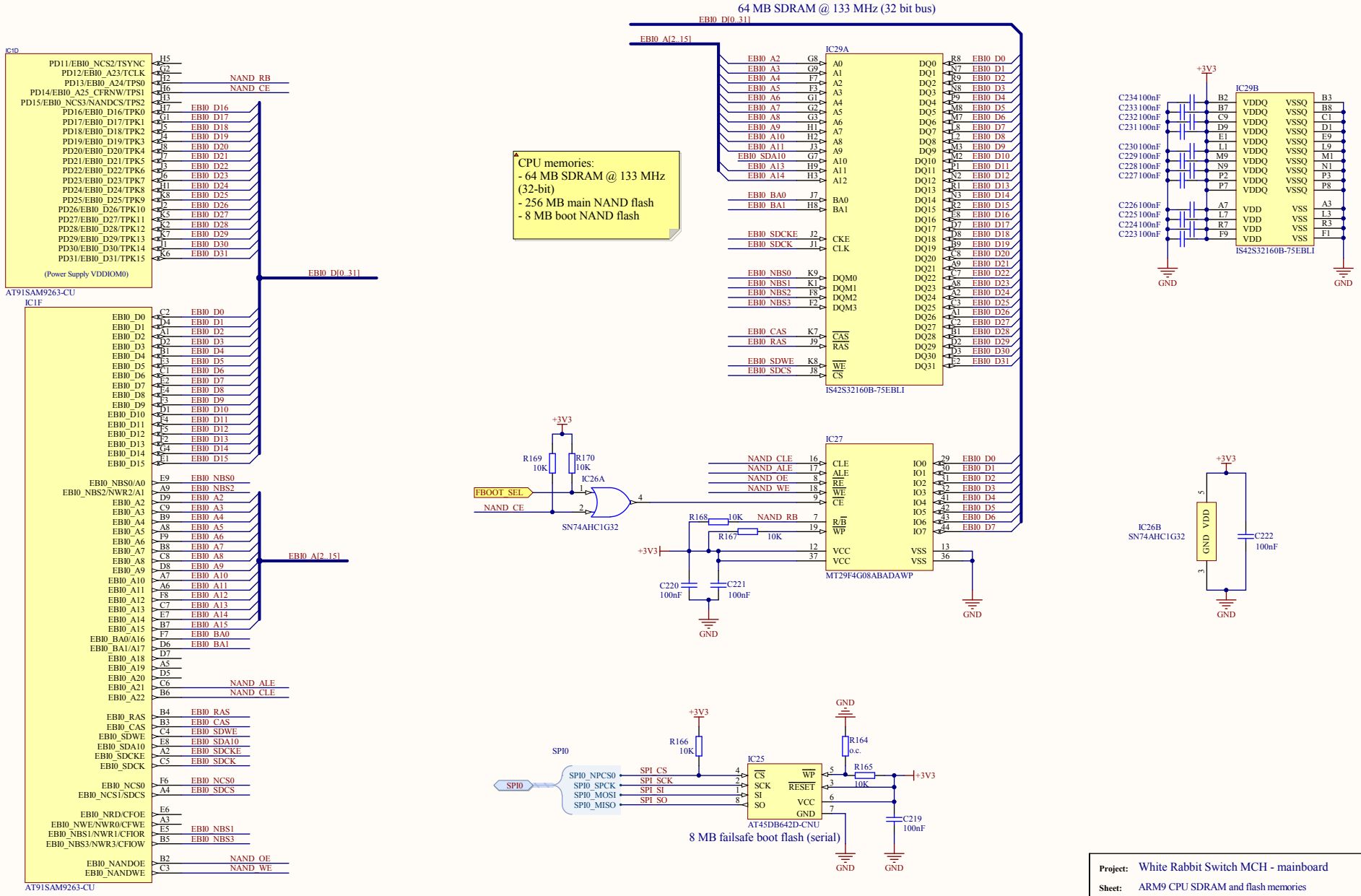

J1
J2
MGTRX112PN
MGTRX113PN
MGTRX114PN
MGTRX115PN
MGTRX116PN
MGTTX112PN
MGTTX113PN
MGTTX114PN
MGTTX115PN
MGTTX116PN
QSS-048-01-L-D-DP
FPGA_GPIO[0..39]
PC[0..15]
PE[0..7]
FPGA_INIT_B
EXT_PROGRAM_B
FPGA_DONE
FPGA_GCLK_P
FPGA_GCLK_N
DMTDCLK_mB_P
DMTDCLK_mB_N
+2V5
+3V5
+5VCC_IN
GND
CN2
KX15-20K4DE
uTCA_CLK
DC10A
P8
EXTPPSIN
P7
EXTREFIN_10M
EXTREFIN_10M_RET
P4
EXTREFIN_125M
P3
EXTPPSOUT
P1
EXTREF125MHZOUT
SMC
P6
CPU_JTAG
Header 10X2
P5
FPGA_JTAG
Header 7X2
ETH_100MHz
CN1
RJ45
Tyco 1888250-1
P2
MHDR2X3
RS232_MNG
CON1
USB-B
Title
Size
A3
Number
Revision
Date: 31/03/2011
Sheet of
File: D:\White Rabbit\SCB\Connectors.SchDoc
Drawn By:

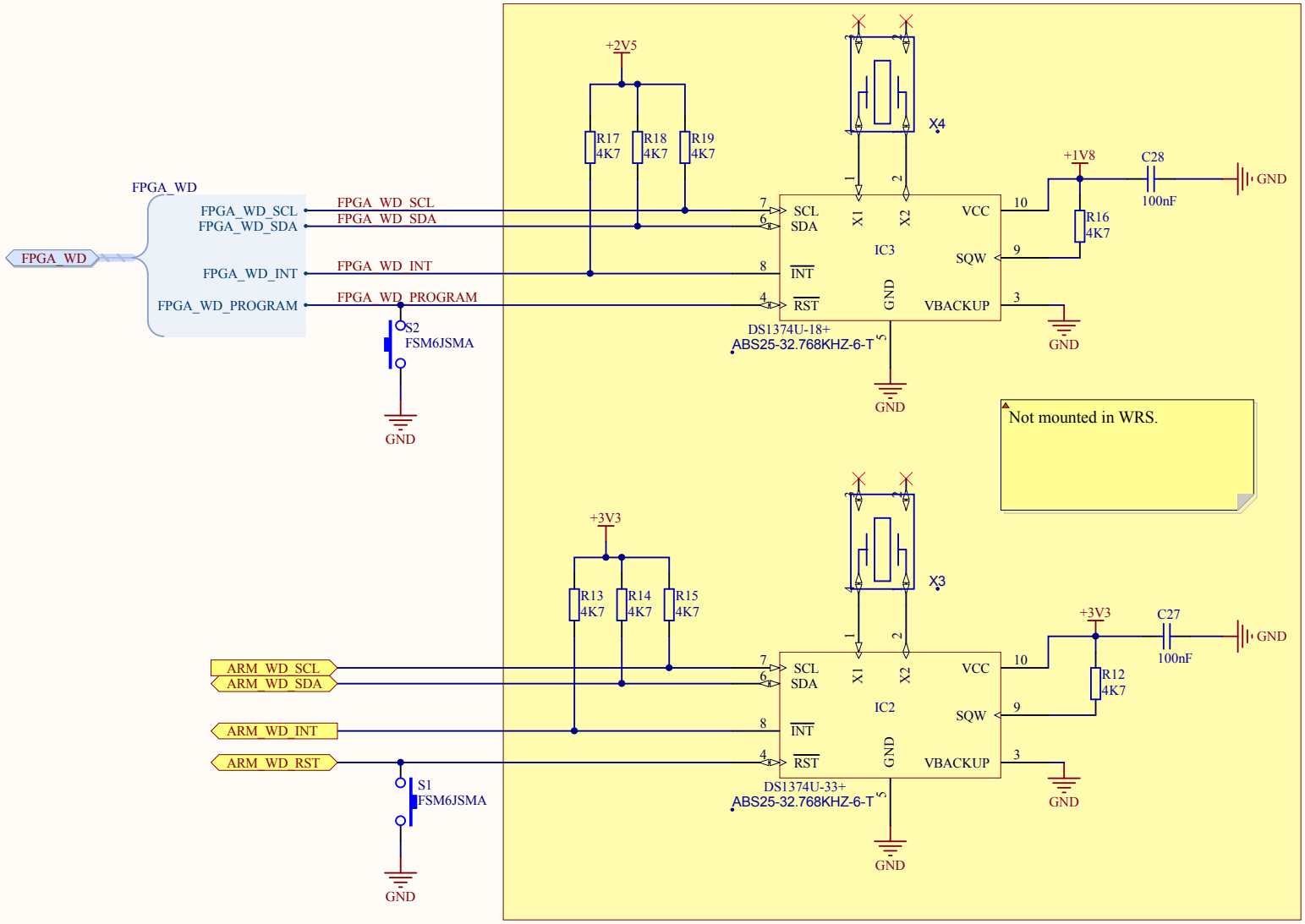


Project:	White Rabbit Switch MCH - mainboard
Sheet:	External 100Mbps Ethernet PHY & magnetics
Version:	1.1.0
Date:	2009/11/12
Author:	Tomasz Wlostowski
License:	Open Hardware License (OHL)
Company:	CERN BE-CO-HT

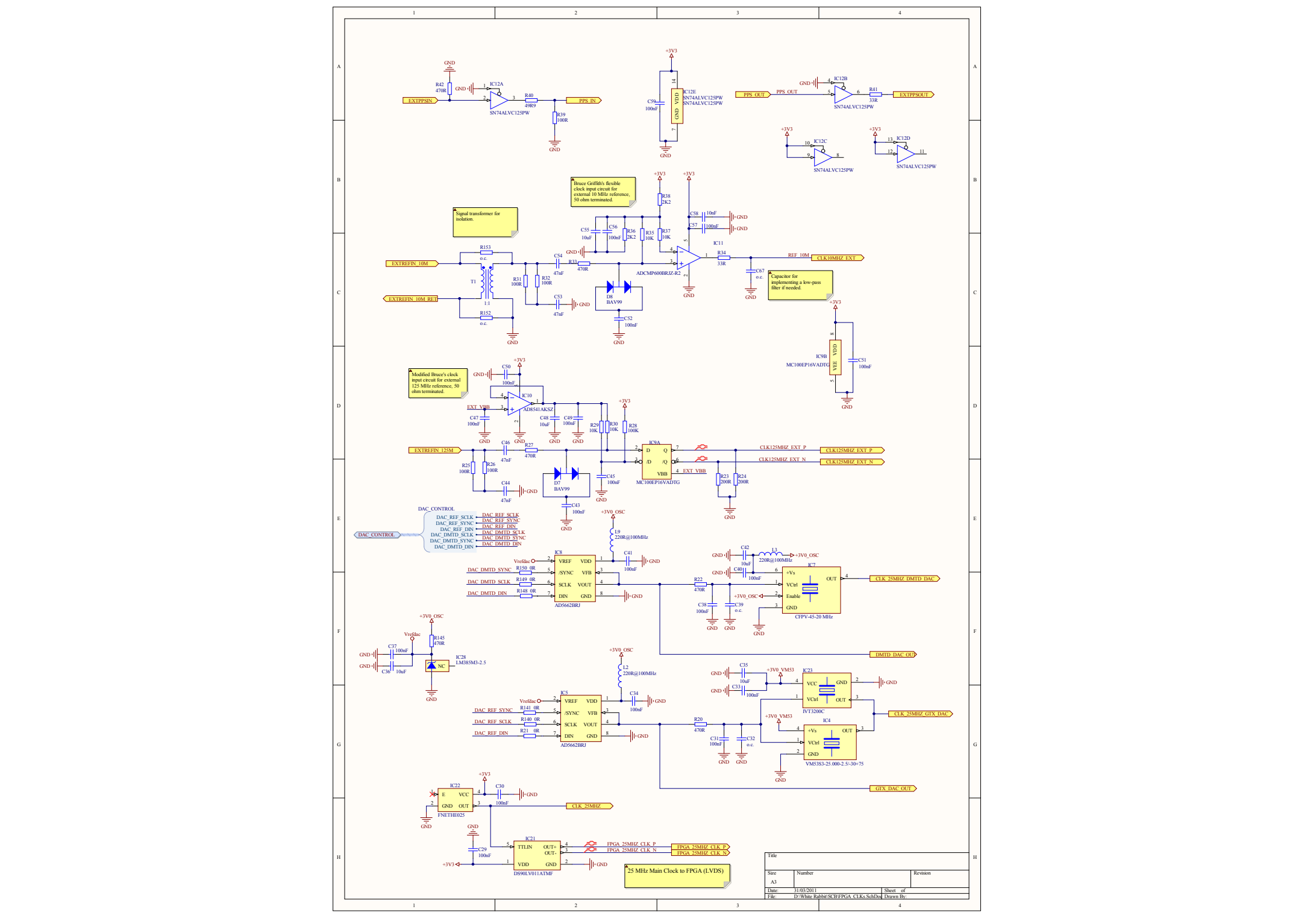

IC1E
PE0/ISI_D0
PE1/ISI_D1
PE2/ISI_D2
PE3/ISI_D3
PE4/ISI_D4
PE5/ISI_D5
PE6/ISI_D6
PE7/ISI_D7
PE8/ISI_PCK/TIOA1
PE9/ISI_HSYNC/TIOB1
PE10/ISI_VSYNC/PWM3
PE11/ISI_MCK/PCK3
PE12/ISI_D8
PE13/ISI_D9
PE14/ISI_D10
PE15/ISI_D11
PE16
PE17
PE18/TIOA0
PE19/TIOB0
(Power Supply VDDIOP1)
AT91SAM9263-CU
PE[0..7]
PCK3
IC1K
PA0/MCI0_DA0/SPI0_MISO
PA1/MCI0_CDA/SPI0_MOSI
PA2/SPI0_SPCK
PA3/MCI0_DA1/SPI0_NPCS1
PA4/MCI0_DA2/SPI0_NPCS2
PA5/MCI0_DA3/SPI0_NPCS0
PA6/MCI1_CK/PCK2
PA7/MCI1_CDA
PA8/MCI1_DA0
PA9/MCI1_DA1
PA10/MCI1_DA2
PA11/MCI1_DA3
PA12/MCI0_CK
PA13/CANTX/PCK0
PA14/CANRX/IRQ0
PA15/TCLK2/IRQ1
(Power Supply VDDIOP0)
AT91SAM9263-CU
SPI0_MISO
SPI0_MOSI
SPI0_SPCK
SPI0_NPCS0
SPI0
CPU_LED1
CPU_LED2
FPGA_DONE
FPGA_INITB
FPGA_PROGRAM_B
EXT_IRQ0
EXT_IRQ1
+3V3
R161
R162
R160
1K
R163
LED_ARRAY
568-0102-222F
GND
FPGA_INITB
FPGA_DONE
IC1B
PB0/AC97FS/TF0
PB1/AC97CK/TK0
PB2/AC97TX/TD0
BMS_PB3/AC97RX/RD0
PB4/TWD/RK0
PB5/TWCK/RF0
PB6/TF1/DMARQ1
PB7/TK1/PWM0
PB8/TD1/PWM1
PB9/RD1/LCDCC
PB10/RK1/PCK1
PB11/RF1/SPI0_NPCS3
PB12/SPI1_MISO
PB13/SPI1_MOSI
PB14/SPI1_SPCK
PB15/SPI1_NPCS0
PB16/SPI1_NPCS1/PCK1
PB17/SPI1_NPCS2/TIOA2
PB18/SPI1_NPCS3/TIOB2
PB19
PB20
PB21
PB22
PB23
PB24/DMARQ3
PB25
PB26
PB27/PWM2
PB28/TCLK0
PB29/PWM3
PB30
PB31
(Power Supply VDDIOP0)
AT91SAM9263-CU
TK0
TD0
TWD
TWCK
CPU_MISO
CPU_MOSI
CPU_SPCK
CPU_NPCS0
ARM_WD_INT
EXT_DMARQ3
CPU_SSC
RF1
RK1
RD1
TD1
TK1
TF1
IC1C
PC0/LCDVSYNC
PC1/LCDHSYNC
PC2/LCDDOTCK
PC3/LCDDEN/PWM1
PC4/LCDD0/LCDD3
PC5/LCDD1/LCDD4
PC6/LCDD2/LCDD5
PC7/LCDD3/LCDD6
PC8/LCDD4/LCDD7
PC9/LCDD5/LCDD10
PC10/LCDD6/LCDD11
PC11/LCDD7/LCDD12
PC12/LCDD8/LCDD13
PC13/LCDD9/LCDD14
PC14/LCDD10/LCDD15
PC15/LCDD11/LCDD19
PC16/LCDD12/LCDD20
PC17/LCDD13/LCDD21
PC18/LCDD14/LCDD22
PC19/LCDD15/LCDD23
PC20/LCDD16/E_TX2
PC21/LCDD17/E_TX3
PC22/LCDD18/E_RX2
PC23/LCDD19/E_RX3
PC24/LCDD20/E_TXER
PC26/LCDD22/E_COL
PC27/LCDD23/E_RXCK
PC28/PWM0/TCLK1
PC29/PCK0/PWM2
PC30/DRXD
PC31/DTXD
(Power Supply VDDIOP0)
AT91SAM9263-CU
PC[0..15]
DBG_RXD
DBG_TXD
SPI1
SPI1_MISO
SPI1_MOSI
SPI1_SPCK
SPI1_NPCS0
Max. Data Rates:
100 Mbps (Translate to 2.5V)
IC24
A1
A2
A3
A4
A5
A6
A7
A8
B1
B2
B3
B4
B5
B6
B7
B8
OE
VCCA
VCCB
GND
TXB0108PWR
+2V5
+3V3
C217
100nF
C218
100nF
Project:
White Rabbit Switch MCH - mainboard
Sheet:
ARM9 CPU I/O ports, busses and power
Version:
1.1.0
Author:
Tomasz Wlostowski
Company: CERN BE-CO-HT
Date: 2009/11/12
License: Open Hardware License (OHL)

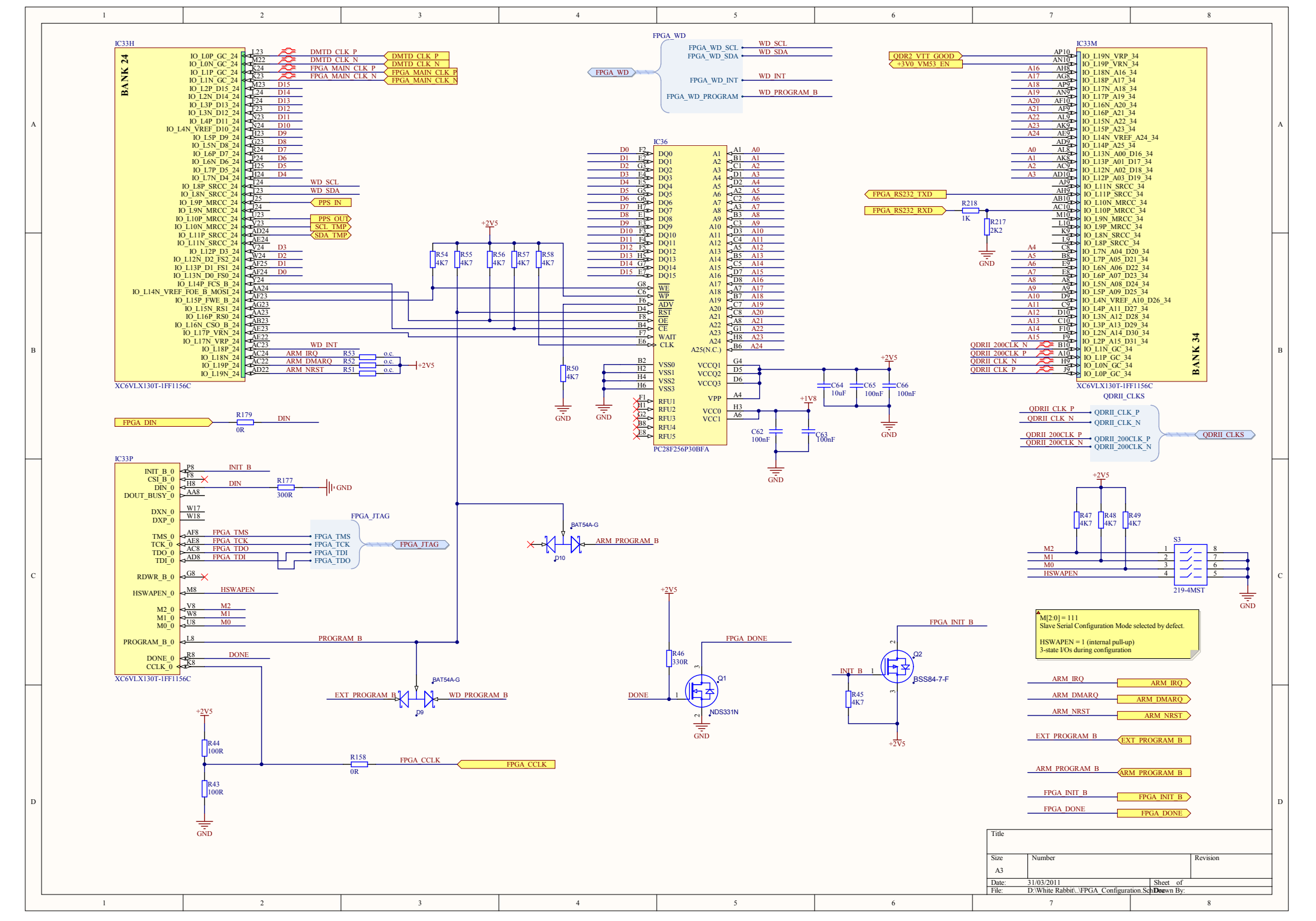

BAT54A-G
D6
FPGA_NRST
EXT_NRST
D5
BAT54A-G
WD_NRST
+3V3
R11 10K
R7 100K
R8 100K
R9 100K
R10 100K
IC1H
PLLRCB
PLLRCA
XOUT
XIN
XOUT32
XIN32
TST
NRST
TDO
RTCK
TCK
TMS
TDI
NTRST
JTAGSEL
WKUP
SHDN
JNRST
JTDO
JRTCK
JTCK
JTMS
JTDI
JNTRST
CPU_JTAG
C26 4.7nF
C25 470pF
C24 10nF
C23 1nF
C22 22pF
C21 22pF
C20 15pF
C19 15pF
R6 2K
R5 1K5
R4 0R
R1 0R
ABM3B 18.432 MHz
X2
R26-32.768- 12.5
X1
R2 o.c.
R3 o.c.
+1V2_cpu
GND
AT91SAM9263-CU
C61 1uF
C60 470nF
IC6
VIN
VOUT
EN
NC
GND
MIC5232-1.2YD5
CN3
BM02B
Battery
D2
TS4148 RZ
D1
TS4148 RZ
C18 100nF
IC1I
VDDBU
GNDBU
VDDIOM1
VDDIOM0
VDDIOP1
VDDIOP0
VDDPLLB
VDDPLLA
VDDOSC
VDDCORE
GNDPLLB
GNDPLLA
C17 100nF
C16 100nF
C15 100nF
C14 100nF
C13 100nF
C12 100nF
C11 100nF
C10 100nF
C9 100nF
C8 100nF
C7 100nF
C6 100nF
C5 100nF
L1
220R@100MHz
AT91SAM9263-CU
C3 22uF
C4 22uF
C1 22uF
C2 22uF
Title
Size
A4
Number
Revision
Date: 31/03/2011
File: D:\White Rabbit\...\CPU_JTAG_Power_PLL.SchDoc
Sheet of
Drawn By:

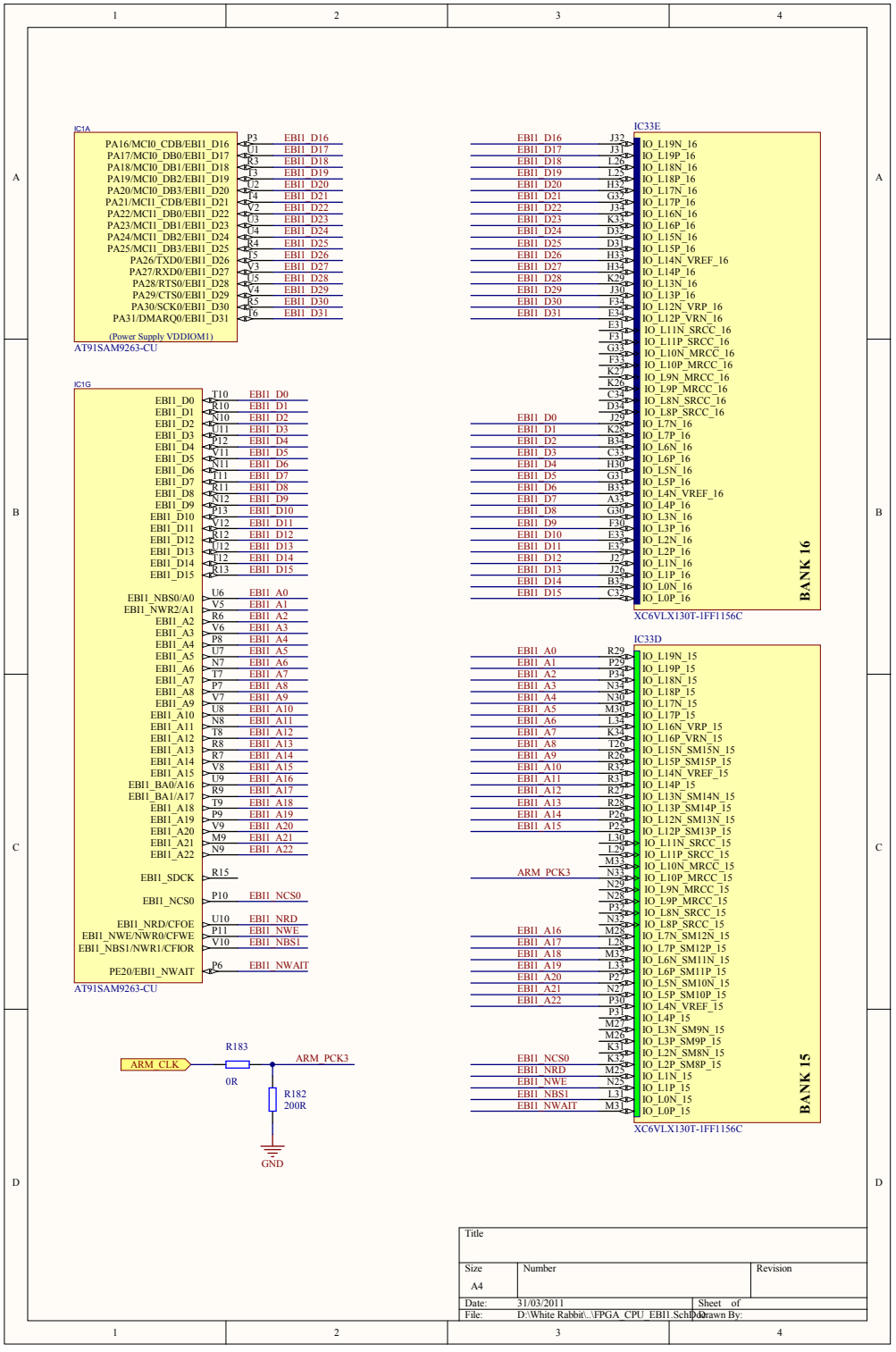

64 MB SDRAM @ 133 MHz (32 bit bus)
EBI0_D[0..31]
EBI0_A[2..15]
IC29A
IS42S32160B-75EBLI
IC29B
IS42S32160B-75EBLI
CPU memories:
- 64 MB SDRAM @ 133 MHz (32-bit)
- 256 MB main NAND flash
- 8 MB boot NAND flash
IC1D
AT91SAM9263-CU
(Power Supply VDDIOM0)
IC1F
AT91SAM9263-CU
IC27
MT29F4G08ABADAWP
IC26A
SN74AHC1G32
IC26B
SN74AHC1G32
IC25
AT45DB642D-CNU
8 MB failsafe boot flash (serial)
SPI0
FBOOT_SEL
NAND_CE
NAND_RB
NAND_ALE
NAND_CLE
NAND_OE
NAND_WE
+3V3
GND
Project: White Rabbit Switch MCH - mainboard
Sheet: ARM9 CPU SDRAM and flash memories
Version: 1.1.0
Date: 2009/11/12
Author: Tomasz Wlostowski
License: Open Hardware License (OHL)
Company: CERN BE-CO-HT

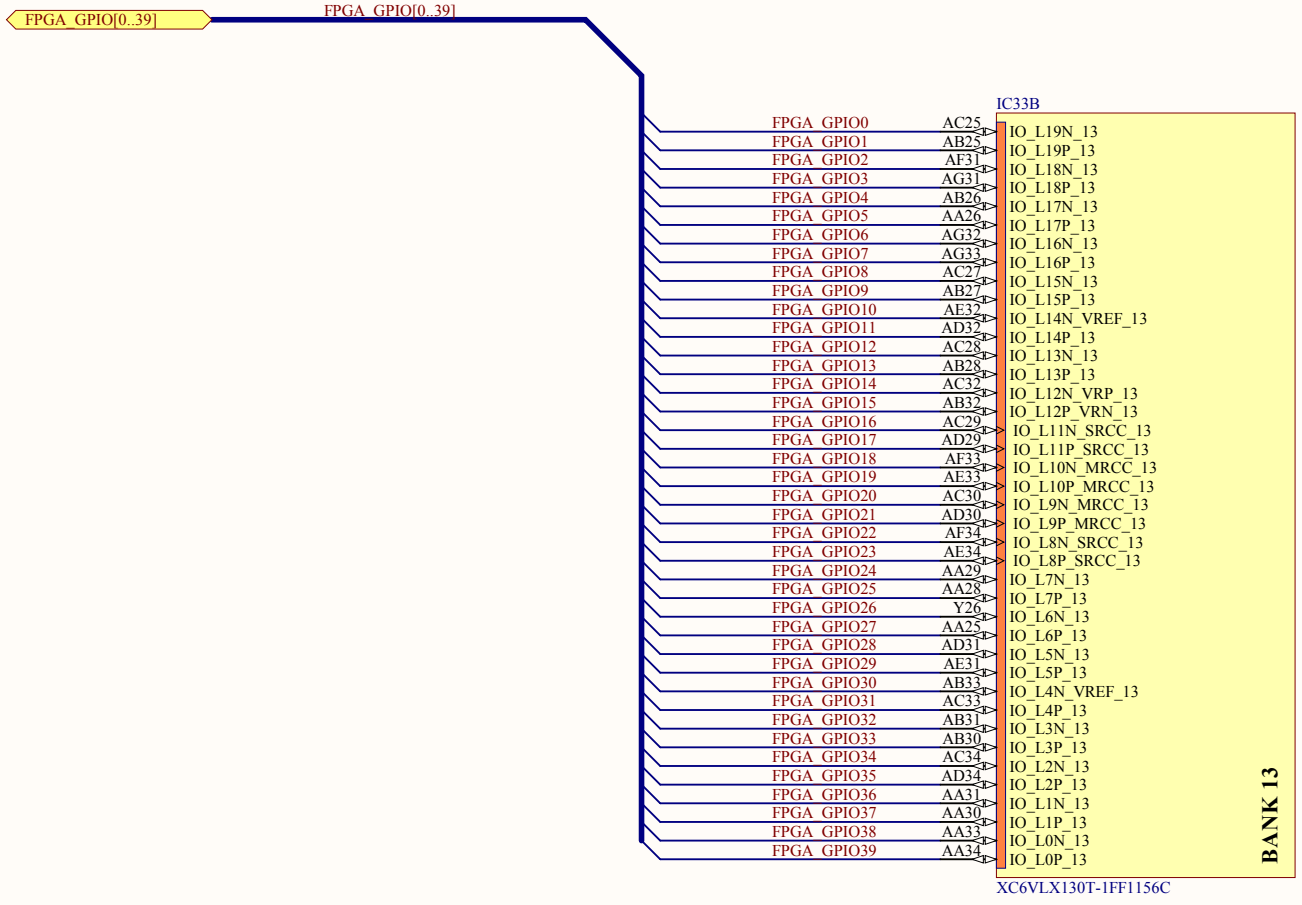


Title		
Size A4	Number	Revision
Date: 31/03/2011	Sheet of	
File: D:\White Rabbit\..\External WatchDogs.SchDoc	Drawn By:	

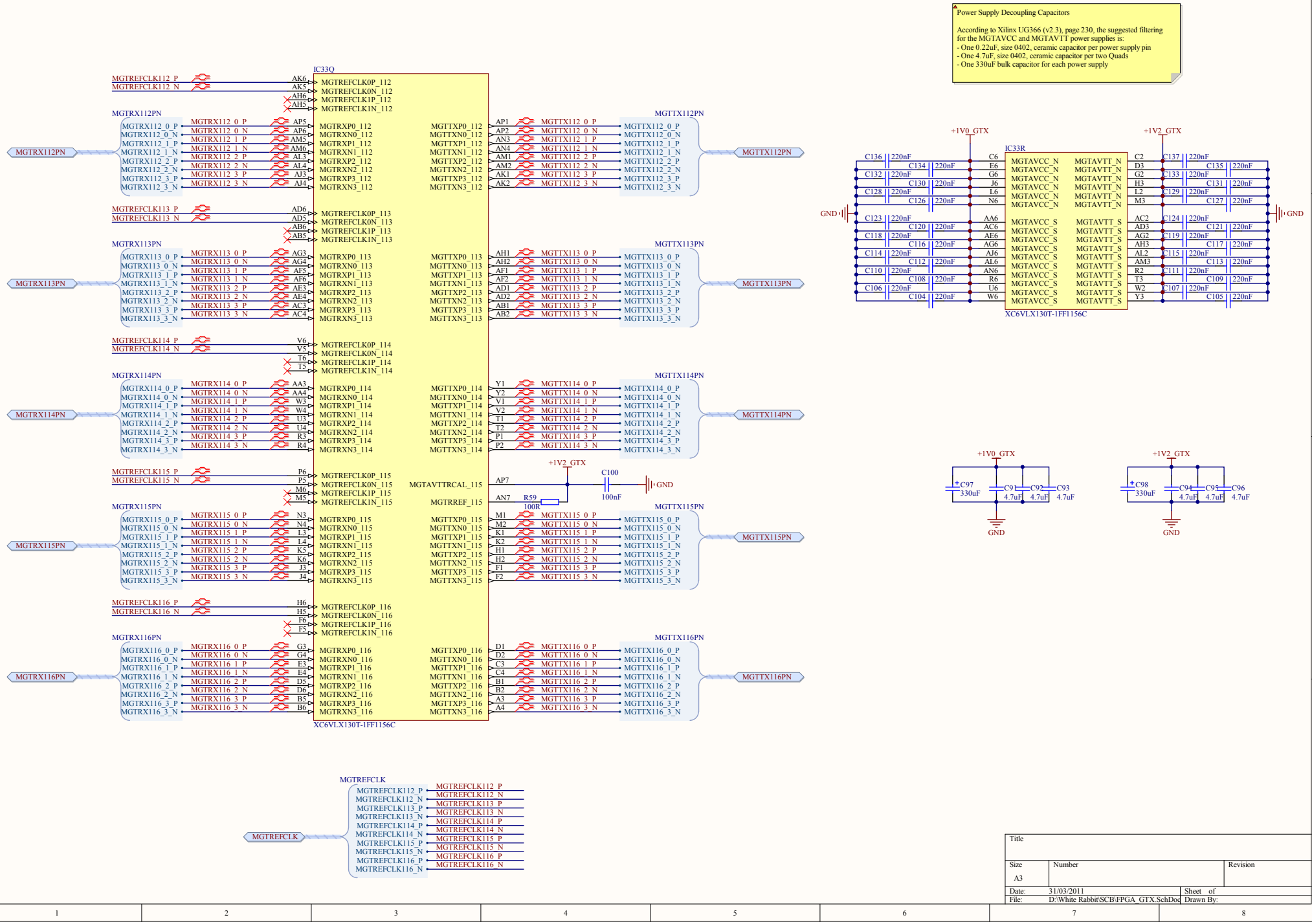

EXTPPSIN
PPS_IN
SN74ALVC125PW
PPS_OUT
EXTPPSOUT
Bruce Griffith's flexible clock input circuit for external 10 MHz reference, 50 ohm terminated.
Signal transformer for isolation.
EXTREFIN_10M
EXTREFIN_10M_RET
ADCMP600BRJZ-R2
REF_10M
CLK10MHZ_EXT
Capacitor for implementing a low-pass filter if needed.
MC100EP16VADTG
Modified Bruce's clock input circuit for external 125 MHz reference, 50 ohm terminated.
AD8541AKSZ
EXTREFIN_125M
CLK125MHZ_EXT_P
CLK125MHZ_EXT_N
DAC_CONTROL
DAC_REF_SCLK
DAC_REF_SYNC
DAC_REF_DIN
DAC_DMTD_SCLK
DAC_DMTD_SYNC
DAC_DMTD_DIN
AD5662BRJ
CFPV-45-20 MHz
CLK_25MHZ_DMTD_DAC
DMTD_DAC_OUT
IVT3200C
CLK_25MHZ_GTX_DAC
VM53S3-25.000-2.5/-30+75
GTX_DAC_OUT
LM385M3-2.5
FNETHE025
CLK_25MHZ
DS90LV011ATMF
FPGA_25MHZ_CLK_P
FPGA_25MHZ_CLK_N
25 MHz Main Clock to FPGA (LVDS)
Title
Size
A3
Number
Revision
Date: 31/03/2011
Sheet of
File: D:\White Rabbit\SCB\FPGA_CLKs.SchDoc
Drawn By:


IC33H
BANK 24
XC6VLX130T-1FF1156C
DMTD_CLK_P
DMTD_CLK_N
FPGA_MAIN_CLK_P
FPGA_MAIN_CLK_N
WD_SCL
WD_SDA
PPS_IN
PPS_OUT
SCL_TMP
SDA_TMP
WD_INT
ARM_IRQ
ARM_DMARQ
ARM_NRST
FPGA_WD
FPGA_WD_SCL
FPGA_WD_SDA
FPGA_WD_INT
FPGA_WD_PROGRAM
IC36
PC28F256P30BFA
IC33M
BANK 34
XC6VLX130T-1FF1156C
QDR2_VTT_GOOD
+3V0_VM53_EN
FPGA_RS232_TXD
FPGA_RS232_RXD
QDRII_200CLK_N
QDRII_200CLK_P
QDRII_CLK_N
QDRII_CLK_P
IC33P
XC6VLX130T-1FF1156C
FPGA_DIN
DIN
INIT_B
FPGA_JTAG
FPGA_TMS
FPGA_TCK
FPGA_TDO
FPGA_TDI
HSWAPEN
PROGRAM_B
DONE
FPGA_CCLK
EXT_PROGRAM_B
ARM_PROGRAM_B
FPGA_DONE
FPGA_INIT_B
QDRII_CLKS
219-4MST
BSS84-7-F
NDS331N
BAT54A-G
+2V5
+1V8
GND
M[2:0] = 111
Slave Serial Configuration Mode selected by defect.
HSWAPEN = 1 (internal pull-up)
3-state I/Os during configuration
Title
Size
A3
Number
Revision
Date: 31/03/2011
Sheet of
File: D:\White Rabbit\..\FPGA_Configuration.SchDoc
Drawn By:

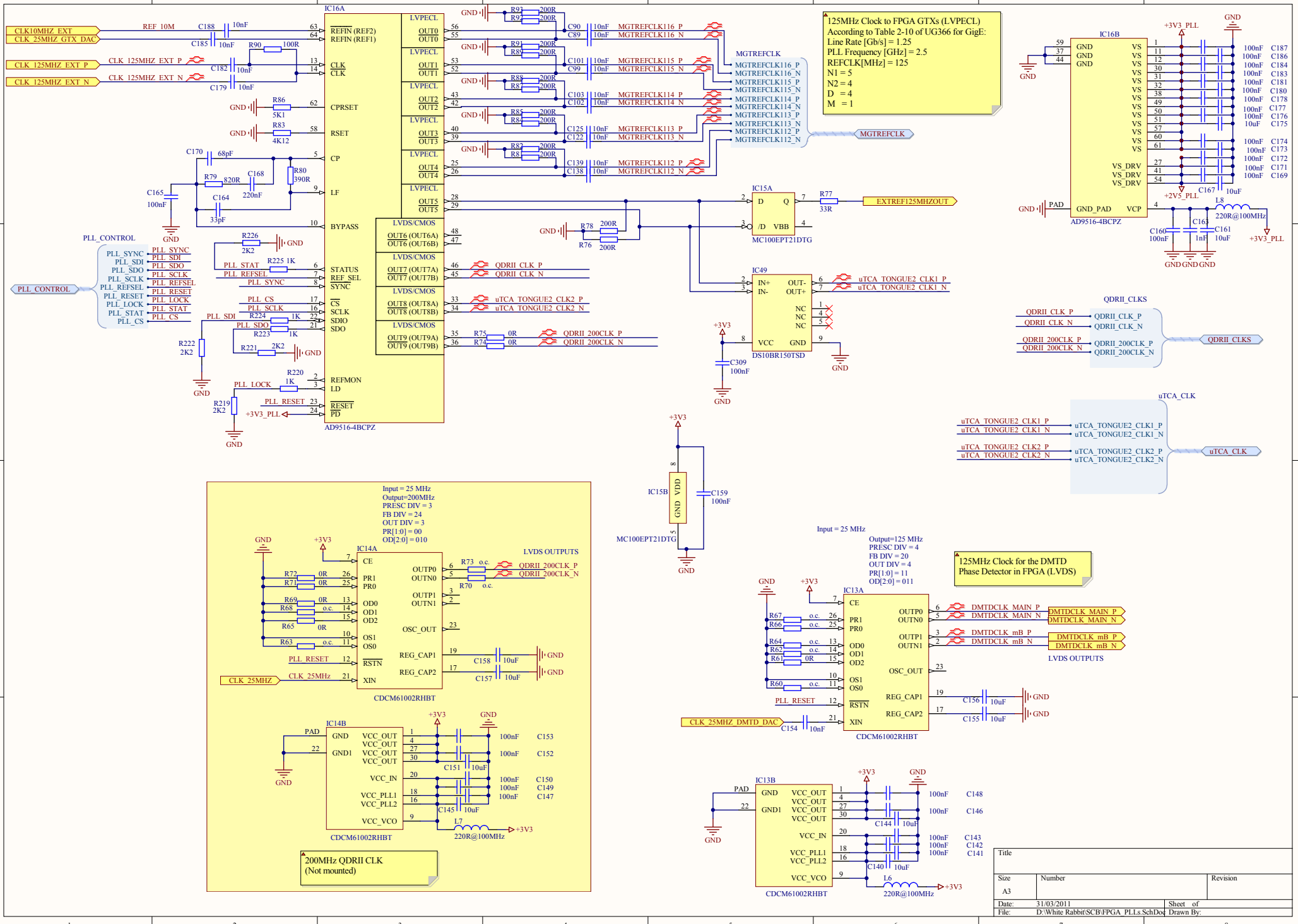

IC1A
PA16/MCI0_CDB/EBI1_D16
PA17/MCI0_DB0/EBI1_D17
PA18/MCI0_DB1/EBI1_D18
PA19/MCI0_DB2/EBI1_D19
PA20/MCI0_DB3/EBI1_D20
PA21/MCI1_CDB/EBI1_D21
PA22/MCI1_DB0/EBI1_D22
PA23/MCI1_DB1/EBI1_D23
PA24/MCI1_DB2/EBI1_D24
PA25/MCI1_DB3/EBI1_D25
PA26/TXD0/EBI1_D26
PA27/RXD0/EBI1_D27
PA28/RTS0/EBI1_D28
PA29/CTS0/EBI1_D29
PA30/SCK0/EBI1_D30
PA31/DMARQ0/EBI1_D31
(Power Supply VDDIOM1)
AT91SAM9263-CU
IC1G
EBI1_D0
EBI1_D1
EBI1_D2
EBI1_D3
EBI1_D4
EBI1_D5
EBI1_D6
EBI1_D7
EBI1_D8
EBI1_D9
EBI1_D10
EBI1_D11
EBI1_D12
EBI1_D13
EBI1_D14
EBI1_D15
EBI1_NBS0/A0
EBI1_NWR2/A1
EBI1_A2
EBI1_A3
EBI1_A4
EBI1_A5
EBI1_A6
EBI1_A7
EBI1_A8
EBI1_A9
EBI1_A10
EBI1_A11
EBI1_A12
EBI1_A13
EBI1_A14
EBI1_A15
EBI1_BA0/A16
EBI1_BA1/A17
EBI1_A18
EBI1_A19
EBI1_A20
EBI1_A21
EBI1_A22
EBI1_SDCK
EBI1_NCS0
EBI1_NRD/CFOE
EBI1_NWE/NWR0/CFWE
EBI1_NBS1/NWR1/CFIOR
PE20/EBI1_NWAIT
AT91SAM9263-CU
R183
ARM_CLK
ARM_PCK3
0R
R182
200R
GND
IC33E
EBI1_D16
EBI1_D17
EBI1_D18
EBI1_D19
EBI1_D20
EBI1_D21
EBI1_D22
EBI1_D23
EBI1_D24
EBI1_D25
EBI1_D26
EBI1_D27
EBI1_D28
EBI1_D29
EBI1_D30
EBI1_D31
IO_L19N_16
IO_L19P_16
IO_L18N_16
IO_L18P_16
IO_L17N_16
IO_L17P_16
IO_L16N_16
IO_L16P_16
IO_L15N_16
IO_L15P_16
IO_L14N_VREF_16
IO_L14P_16
IO_L13N_16
IO_L13P_16
IO_L12N_VRP_16
IO_L12P_VRN_16
IO_L11N_SRCC_16
IO_L11P_SRCC_16
IO_L10N_MRCC_16
IO_L10P_MRCC_16
IO_L9N_MRCC_16
IO_L9P_MRCC_16
IO_L8N_SRCC_16
IO_L8P_SRCC_16
IO_L7N_16
IO_L7P_16
IO_L6N_16
IO_L6P_16
IO_L5N_16
IO_L5P_16
IO_L4N_VREF_16
IO_L4P_16
IO_L3N_16
IO_L3P_16
IO_L2N_16
IO_L2P_16
IO_L1N_16
IO_L1P_16
IO_L0N_16
IO_L0P_16
BANK 16
XC6VLX130T-1FF1156C
IC33D
EBI1_A0
EBI1_A1
EBI1_A2
EBI1_A3
EBI1_A4
EBI1_A5
EBI1_A6
EBI1_A7
EBI1_A8
EBI1_A9
EBI1_A10
EBI1_A11
EBI1_A12
EBI1_A13
EBI1_A14
EBI1_A15
ARM_PCK3
EBI1_A16
EBI1_A17
EBI1_A18
EBI1_A19
EBI1_A20
EBI1_A21
EBI1_A22
EBI1_NCS0
EBI1_NRD
EBI1_NWE
EBI1_NBS1
EBI1_NWAIT
IO_L19N_15
IO_L19P_15
IO_L18N_15
IO_L18P_15
IO_L17N_15
IO_L17P_15
IO_L16N_VRP_15
IO_L16P_VRN_15
IO_L15N_SM15N_15
IO_L15P_SM15P_15
IO_L14N_VREF_15
IO_L14P_15
IO_L13N_SM14N_15
IO_L13P_SM14P_15
IO_L12N_SM13N_15
IO_L12P_SM13P_15
IO_L11N_SRCC_15
IO_L11P_SRCC_15
IO_L10N_MRCC_15
IO_L10P_MRCC_15
IO_L9N_MRCC_15
IO_L9P_MRCC_15
IO_L8N_SRCC_15
IO_L8P_SRCC_15
IO_L7N_SM12N_15
IO_L7P_SM12P_15
IO_L6N_SM11N_15
IO_L6P_SM11P_15
IO_L5N_SM10N_15
IO_L5P_SM10P_15
IO_L4N_VREF_15
IO_L4P_15
IO_L3N_SM9N_15
IO_L3P_SM9P_15
IO_L2N_SM8N_15
IO_L2P_SM8P_15
IO_L1N_15
IO_L1P_15
IO_L0N_15
IO_L0P_15
BANK 15
XC6VLX130T-1FF1156C
Title
Size
A4
Number
Revision
Date: 31/03/2011
Sheet of
File: D:\White Rabbit\..\FPGA_CPU_EBI1.SchDoc
Drawn By:

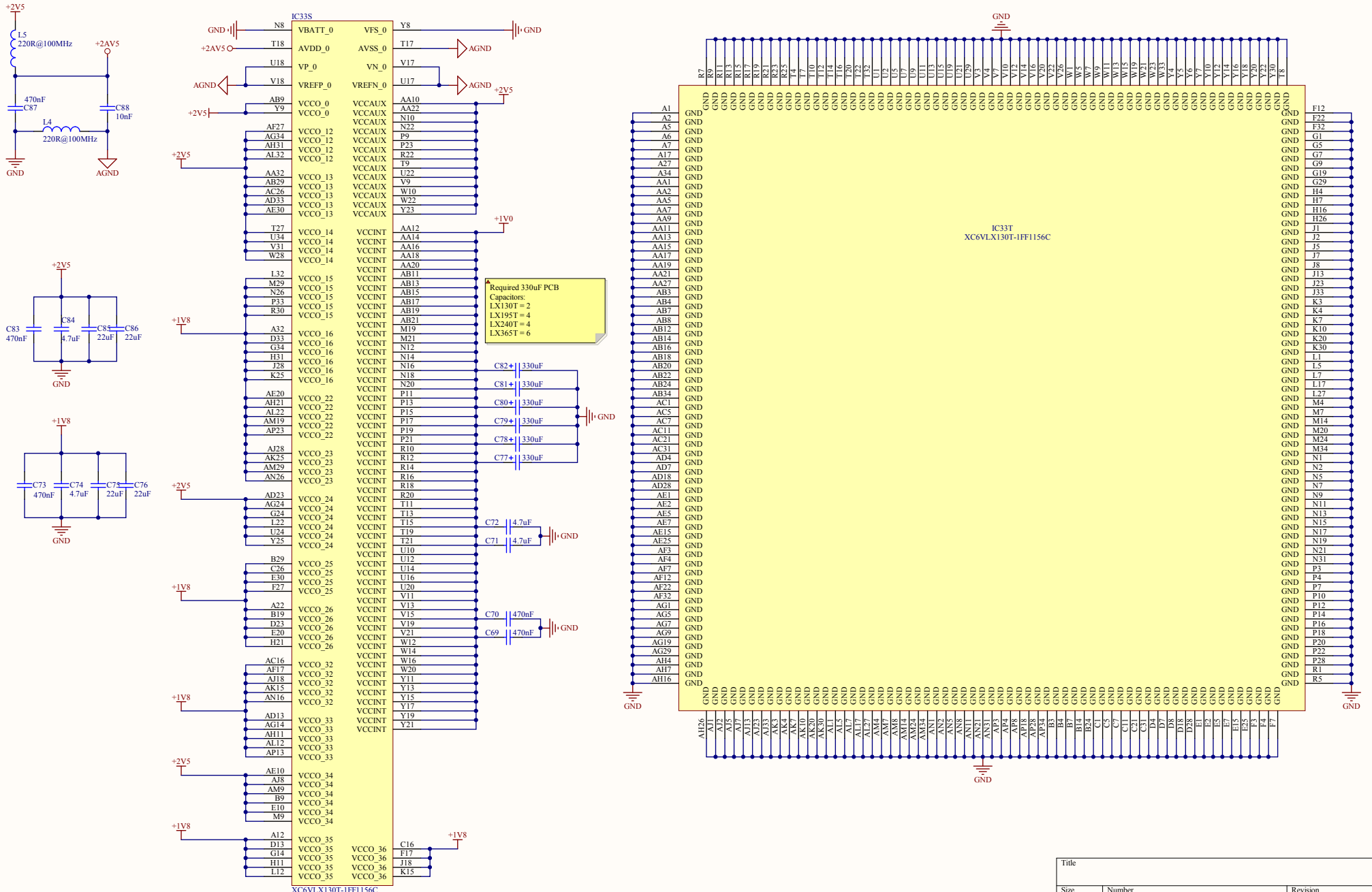


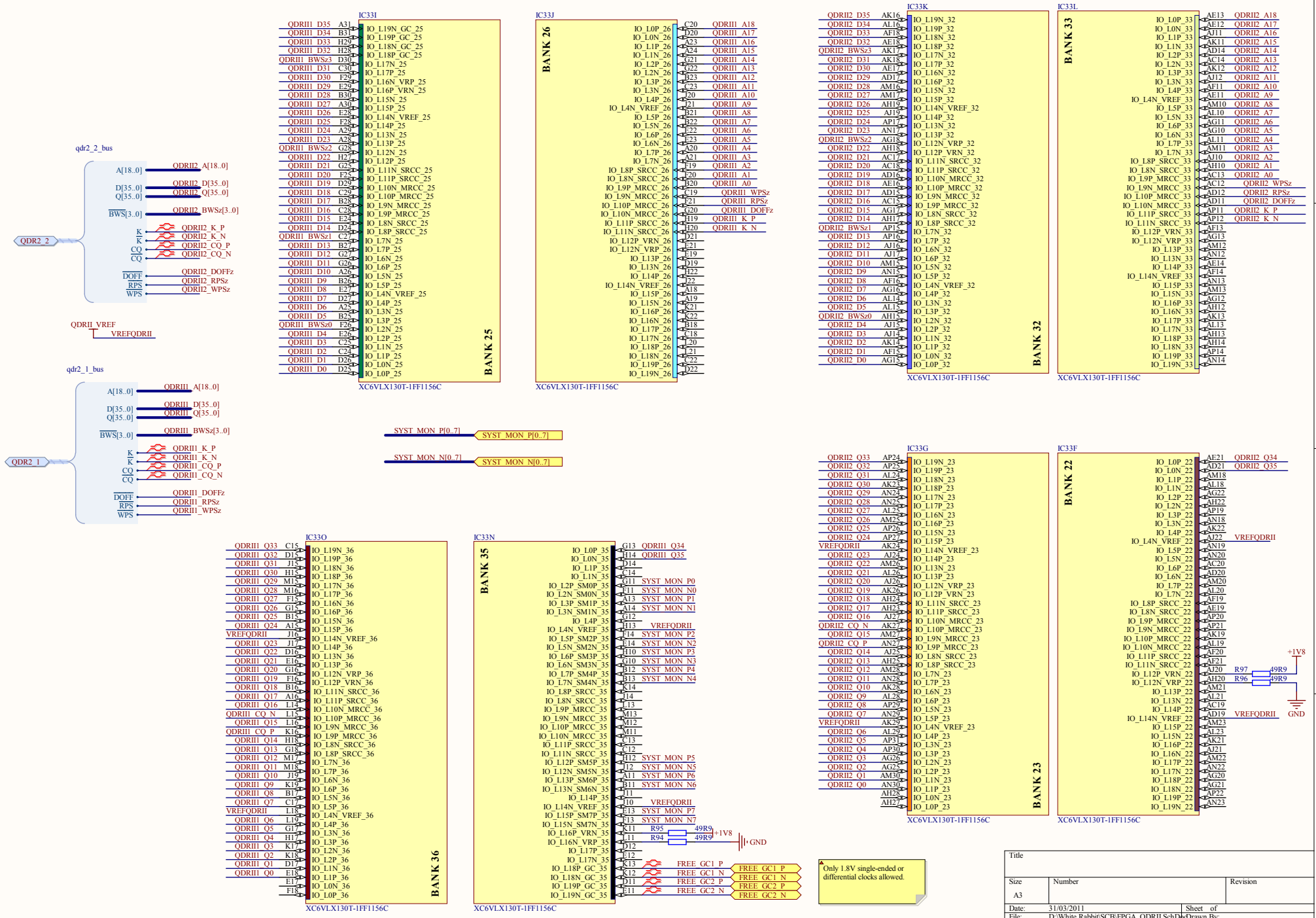
Title		
Size A4	Number	Revision
Date: 31/03/2011	Sheet of	
File: D:\White Rabbit\SCB\FPGA_GPIOs.SchDoc	Drawn By:	

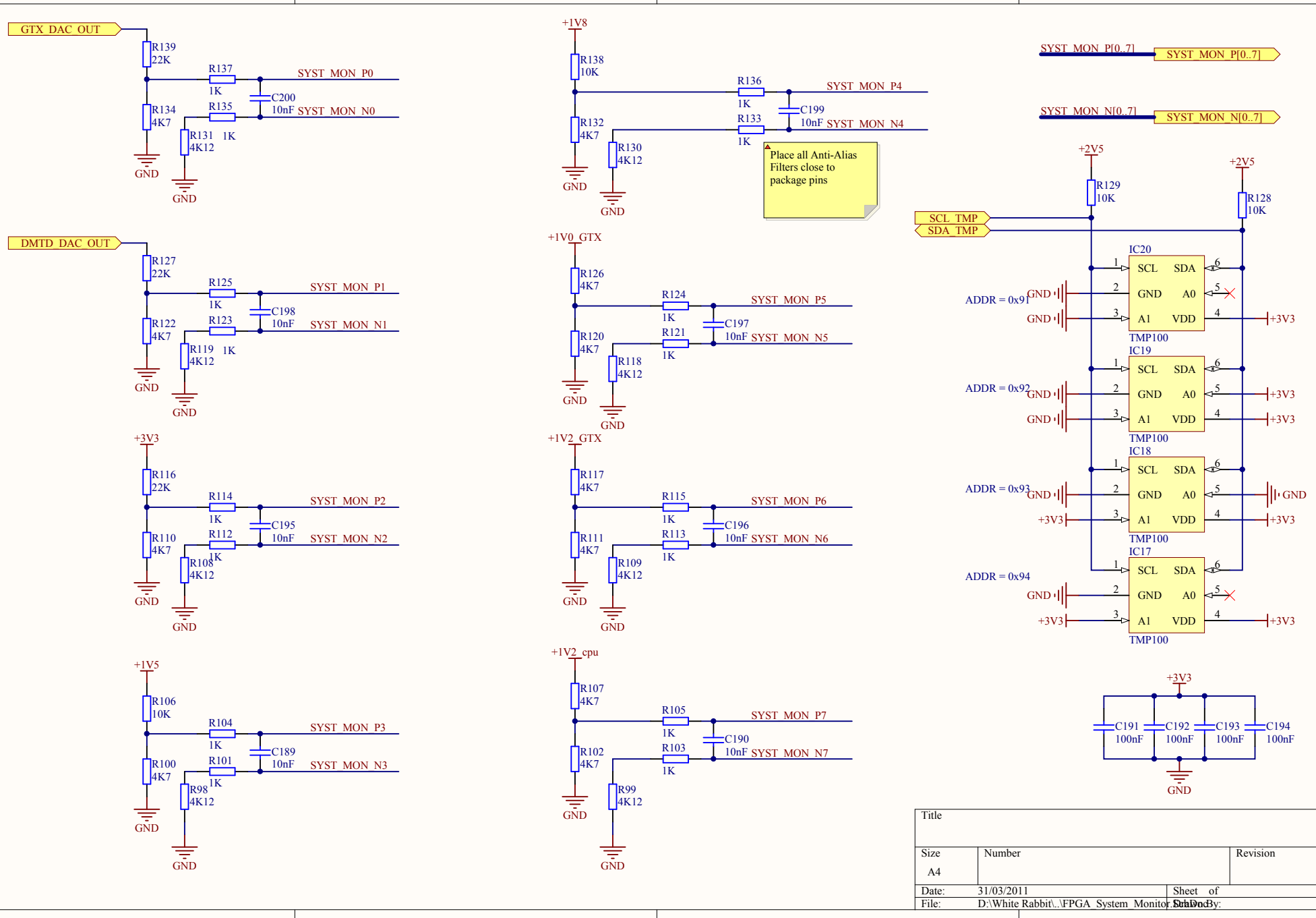


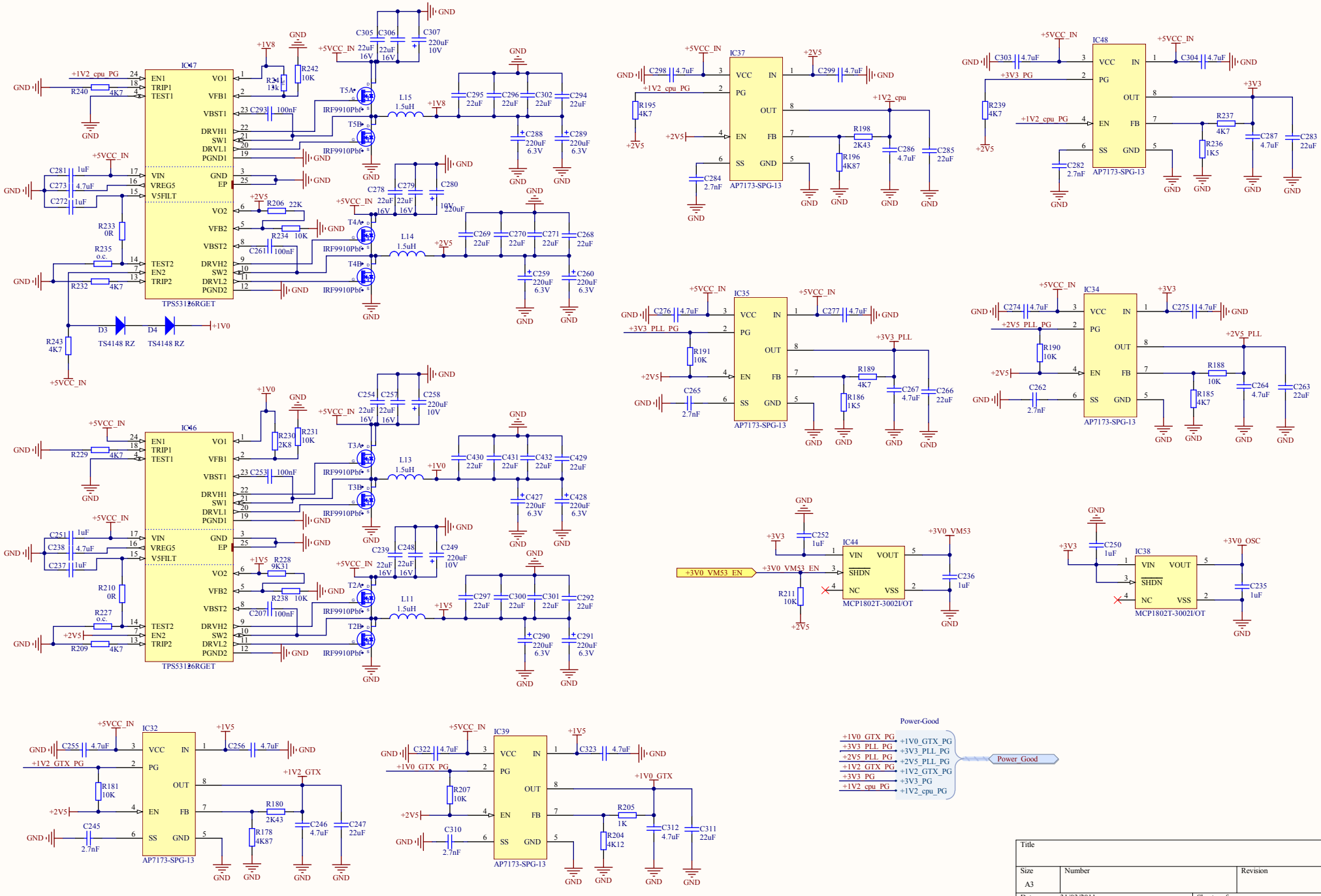
Title		
Size: A3	Number	Revision
Date: 31/03/2011		Sheet of
File: D:\White Rabbit\SCB\FPGA_GTX.SchDoc		Drawn By:

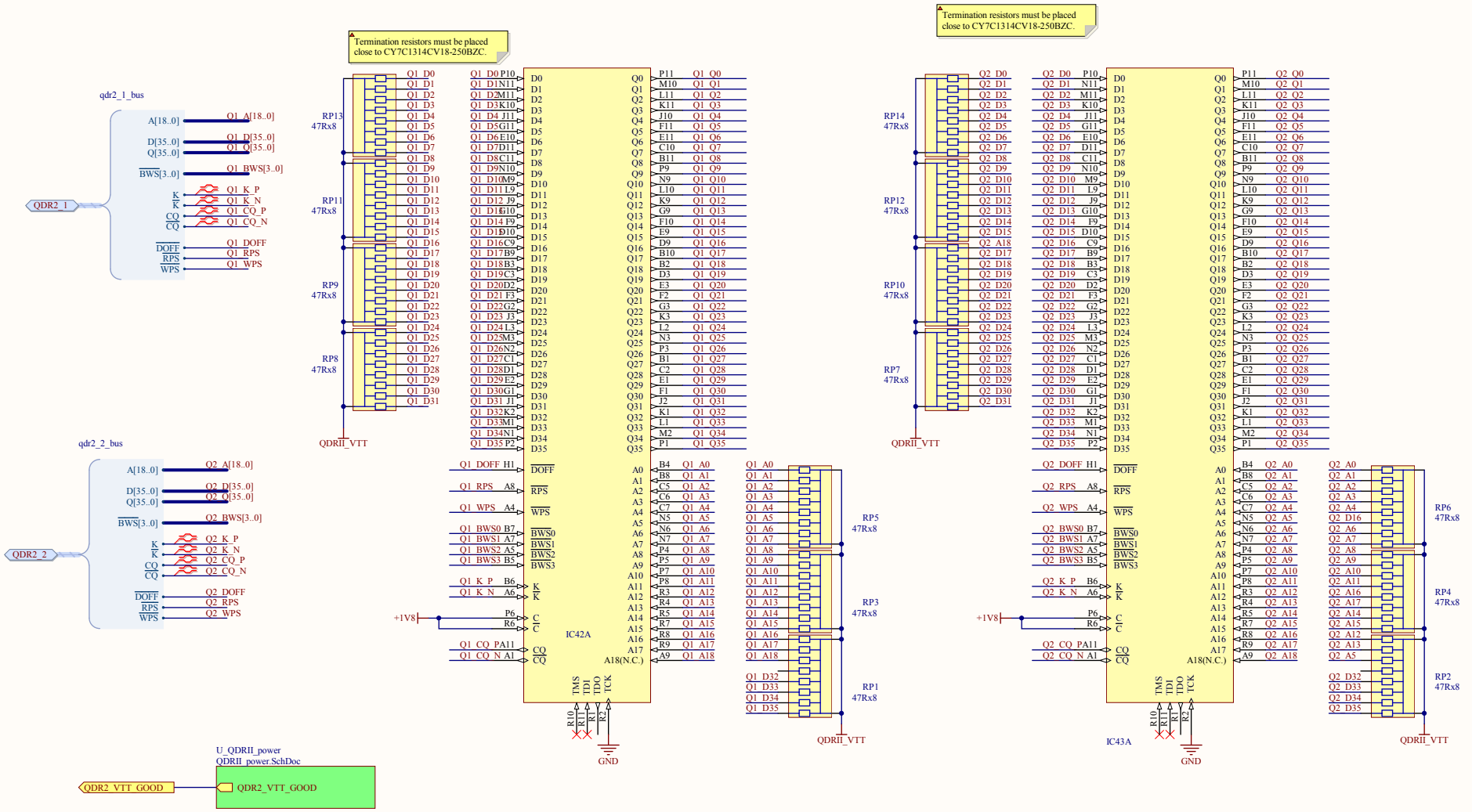

IC16A
AD9516-4BCPZ
125MHz Clock to FPGA GTXs (LVPECL)
According to Table 2-10 of UG366 for GigE:
Line Rate [Gb/s] = 1.25
PLL Frequency [GHz] = 2.5
REFCLK[MHz] = 125
N1 = 5
N2 = 4
D = 4
M = 1
IC16B
AD9516-4BCPZ
IC15A
MC100EPT21DTG
IC49
DS10BR150TSD
IC15B
MC100EPT21DTG
Input = 25 MHz
Output=200MHz
PRESC DIV = 3
FB DIV = 24
OUT DIV = 3
PR[1:0] = 00
OD[2:0] = 010
IC14A
CDCM61002RHBT
IC14B
CDCM61002RHBT
200MHz QDRII CLK
(Not mounted)
Input = 25 MHz
Output=125 MHz
PRESC DIV = 4
FB DIV = 20
OUT DIV = 4
PR[1:0] = 11
OD[2:0] = 011
IC13A
CDCM61002RHBT
125MHz Clock for the DMTD
Phase Detector in FPGA (LVDS)
IC13B
CDCM61002RHBT
Title
Size A3
Number
Revision
Date: 31/03/2011
Sheet of
File: D:\White Rabbit\SCB\FPGA_PLLs.SchDoc
Drawn By:


+2V5
L5
220R@100MHz
+2AV5
470nF
C87
C88
10nF
L4
220R@100MHz
GND
AGND
+1V8
C83
470nF
C84
4.7uF
C85
22uF
C86
22uF
C73
470nF
C74
4.7uF
C75
22uF
C76
22uF
IC33S
XC6VLX130T-1FF1156C
Required 330uF PCB
Capacitors:
LX130T = 2
LX195T = 4
LX240T = 4
LX365T = 6
C82 330uF
C81 330uF
C80 330uF
C79 330uF
C78 330uF
C77 330uF
C72 4.7uF
C71 4.7uF
C70 470nF
C69 470nF
C16
+1V0
IC33T
XC6VLX130T-1FF1156C
Title
Size
A3
Number
Revision
Date:
31/03/2011
Sheet of
File:
D:\White Rabbit\..\FPGA_POWER_DGND.SchDoc
Drawn By:

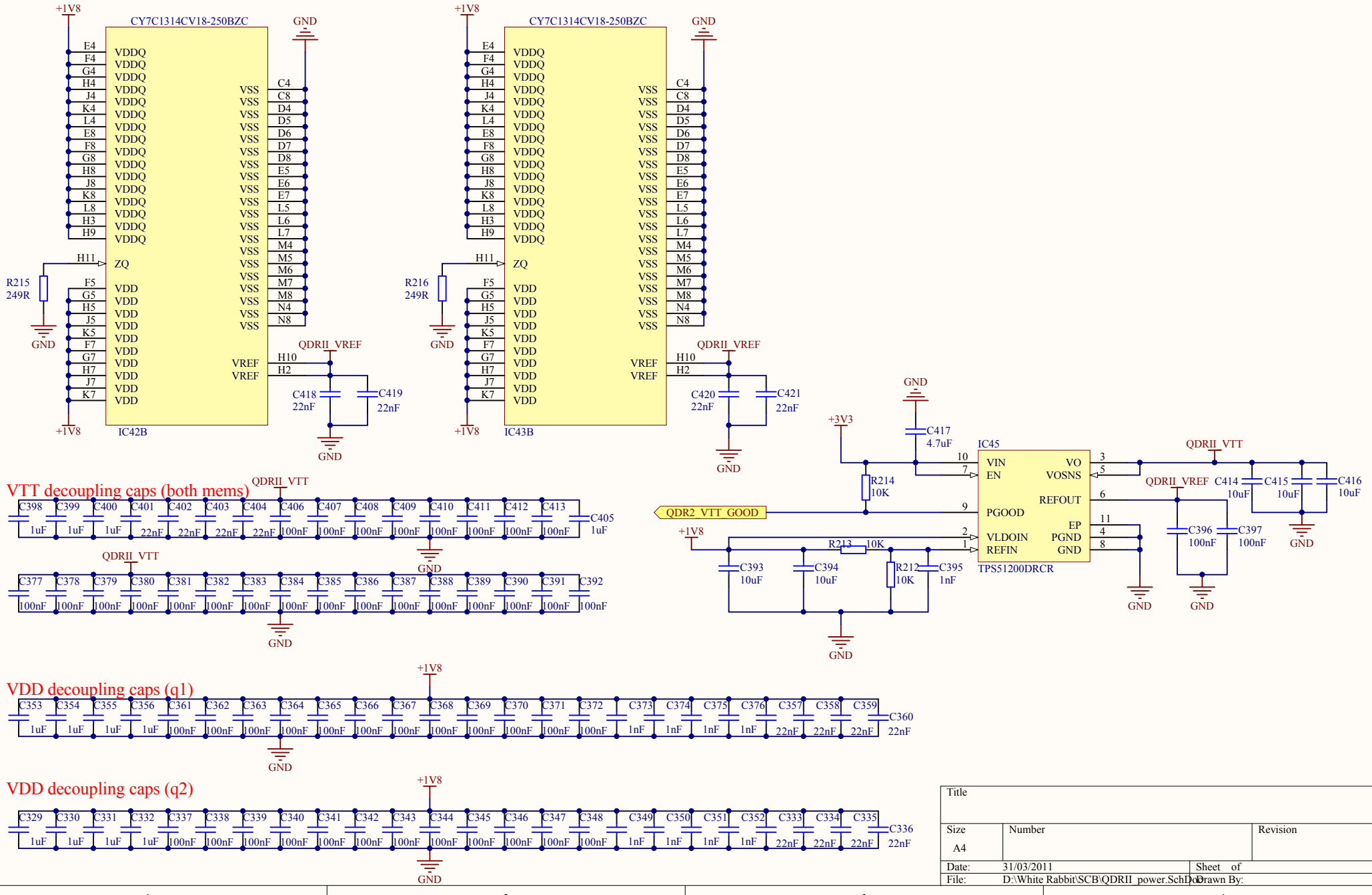

IC33I
IC33J
IC33K
IC33L
IC33O
IC33N
IC33G
IC33F
BANK 25
BANK 26
BANK 32
BANK 33
BANK 36
BANK 35
BANK 23
BANK 22
XC6VLX130T-1FF1156C
qdr2_2_bus
qdr2_1_bus
QDR2_2
QDR2_1
QDRII_VREF
VREFQDRII
SYST_MON_P[0..7]
SYST_MON_N[0..7]
+1V8
GND
R95
R94
R97
R96
49R9
Only 1.8V single-ended or differential clocks allowed.
Title
Size
A3
Number
Revision
Date: 31/03/2011
Sheet of
File: D:\White Rabbit\SCB\FPGA_QDRII.SchDoc
Drawn By:

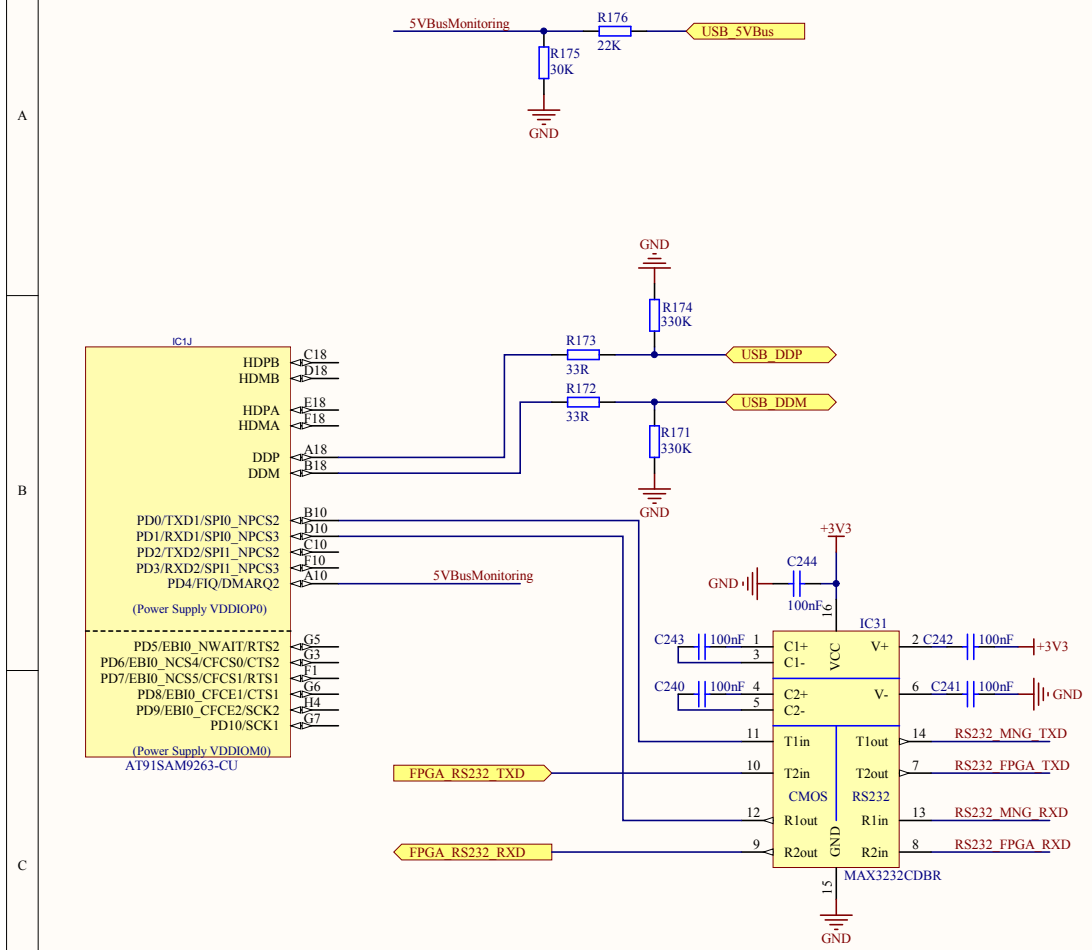

GTX_DAC_OUT
R139 22K
R137 1K
SYST_MON_P0
C200 10nF
R134 4K7
R135 1K
SYST_MON_N0
R131 4K12
GND
DMTD_DAC_OUT
R127 22K
R125 1K
SYST_MON_P1
C198 10nF
R122 4K7
R123 1K
SYST_MON_N1
R119 4K12
+3V3
R116 22K
R114 1K
SYST_MON_P2
C195 10nF
R110 4K7
R112 1K
SYST_MON_N2
R108 4K12
+1V5
R106 10K
R104 1K
SYST_MON_P3
C189 10nF
R100 4K7
R101 1K
SYST_MON_N3
R98 4K12
+1V8
R138 10K
R136 1K
SYST_MON_P4
C199 10nF
R132 4K7
R133 1K
SYST_MON_N4
R130 4K12
Place all Anti-Alias Filters close to package pins
+1V0_GTX
R126 4K7
R124 1K
SYST_MON_P5
C197 10nF
R120 4K7
R121 1K
SYST_MON_N5
R118 4K12
+1V2_GTX
R117 4K7
R115 1K
SYST_MON_P6
C196 10nF
R111 4K7
R113 1K
SYST_MON_N6
R109 4K12
+1V2_cpu
R107 4K7
R105 1K
SYST_MON_P7
C190 10nF
R102 4K7
R103 1K
SYST_MON_N7
R99 4K12
SYST_MON_P[0..7]
SYST_MON_N[0..7]
+2V5
R129 10K
R128 10K
SCL_TMP
SDA_TMP
IC20
IC19
IC18
IC17
SCL
SDA
GND
A0
A1
VDD
TMP100
ADDR = 0x91
ADDR = 0x92
ADDR = 0x93
ADDR = 0x94
+3V3
C191 100nF
C192 100nF
C193 100nF
C194 100nF
Title
Size A4
Number
Revision
Date: 31/03/2011
Sheet of
File: D:\White Rabbit\..\FPGA_System_Monitor.SchDoc
Drawn By:


IC47
TPS53126RGET
IC46
TPS53126RGET
IC37
AP7173-SPG-13
IC48
AP7173-SPG-13
IC35
AP7173-SPG-13
IC34
AP7173-SPG-13
IC44
MCP1802T-3002I/OT
IC38
MCP1802T-3002I/OT
IC32
AP7173-SPG-13
IC39
AP7173-SPG-13
D3
TS4148 RZ
D4
TS4148 RZ
Power-Good
Power_Good
Title
Size
A3
Number
Revision
Date:
31/03/2011
Sheet of
File:
D:\White Rabbit\SCB\Power_Supply.SchDoc
Drawn By:

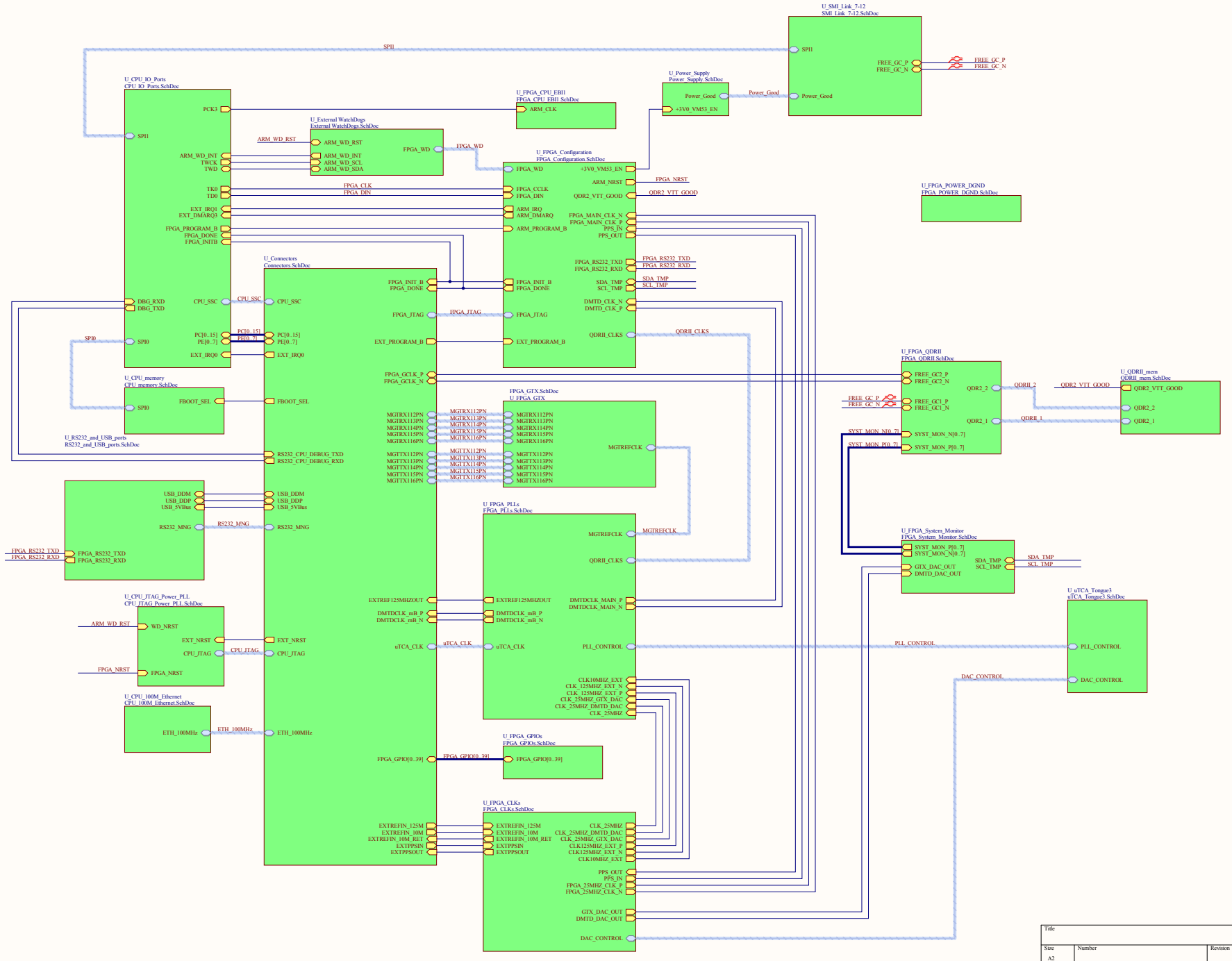


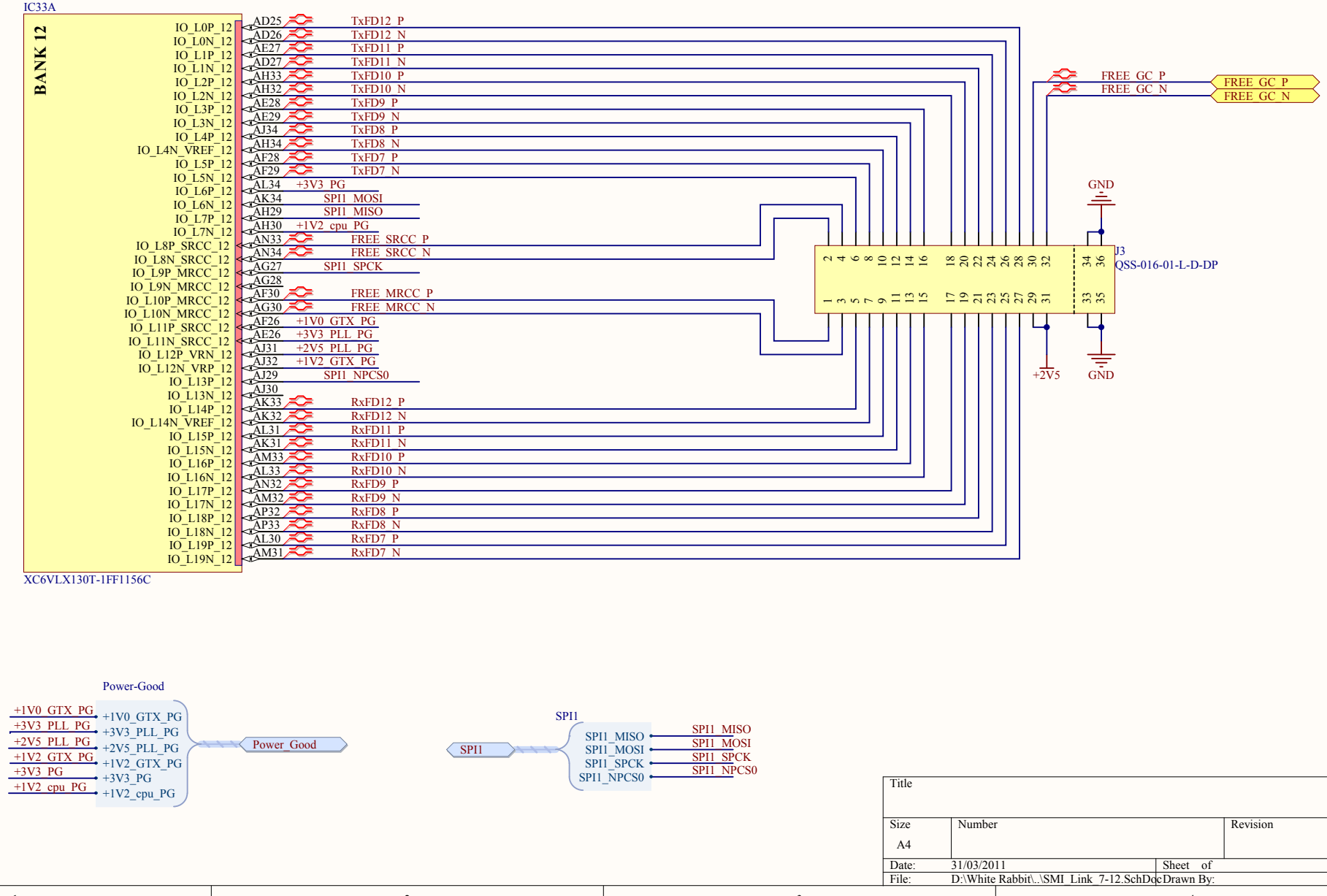
Title		
Size: A3	Number	Revision
Date: 31/03/2011	Sheet of	
File: D:\White Rabbit\SCB\QDRII_mem.SchDoc	Drawn By:	

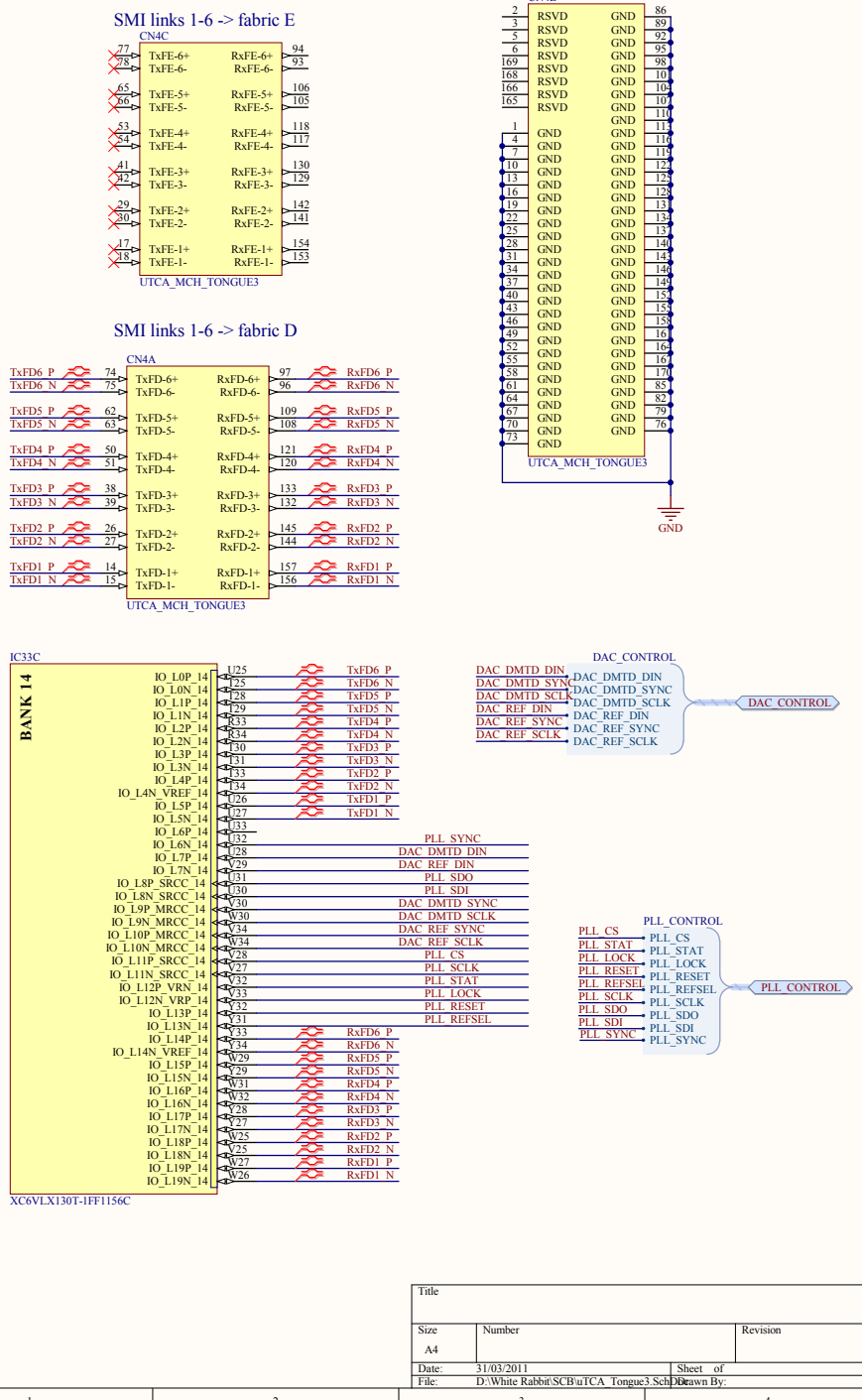

CY7C1314CV18-250BZC
IC42B
IC43B
+1V8
GND
R215 249R
R216 249R
QDRII_VREF
C418 22nF
C419 22nF
C420 22nF
C421 22nF
VTT decoupling caps (both mems)
QDRII_VTT
C398 C399 C400 C401 C402 C403 C404 C406 C407 C408 C409 C410 C411 C412 C413 C405
1uF 1uF 1uF 22nF 22nF 22nF 22nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 1uF
C377 C378 C379 C380 C381 C382 C383 C384 C385 C386 C387 C388 C389 C390 C391 C392
100nF
IC45
TPS51200DRCR
VIN
EN
PGOOD
VLDOIN
REFIN
VO
VOSNS
REFOUT
EP
PGND
GND
+3V3
C417 4.7uF
R214 10K
R213 10K
R212 10K
C393 10uF
C394 10uF
C395 1nF
QDR2_VTT_GOOD
C414 10uF
C415 10uF
C416 10uF
C396 100nF
C397 100nF
VDD decoupling caps (q1)
C353 C354 C355 C356 C361 C362 C363 C364 C365 C366 C367 C368 C369 C370 C371 C372 C373 C374 C375 C376 C357 C358 C359 C360
1uF 1uF 1uF 1uF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 1nF 1nF 1nF 1nF 22nF 22nF 22nF 22nF
VDD decoupling caps (q2)
C329 C330 C331 C332 C337 C338 C339 C340 C341 C342 C343 C344 C345 C346 C347 C348 C349 C350 C351 C352 C333 C334 C335 C336
1uF 1uF 1uF 1uF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 1nF 1nF 1nF 1nF 22nF 22nF 22nF 22nF
Title
Size A4
Number
Revision
Date: 31/03/2011
Sheet of
File: D:\White Rabbit\SCB\QDRII_power.SchDoc
Drawn By:



Title	White Rabbit Switch MCH - clocking mezzanine RS232 port	
Size A	Number	Revision
Date: 31/03/2011	Sheet of	
File: D:\White Rabbit\..\RS232_and_USB_ports.SchDoc	Drawn By:	


U_SMI_Link_7-12
SMI_Link_7-12.SchDoc
SPI1
FREE_GC_P
FREE_GC_N
U_CPU_IO_Ports
CPU_IO_Ports.SchDoc
PCK3
SPI1
ARM_WD_INT
TWCK
TWD
TK0
TD0
EXT_IRQ1
EXT_DMARQ3
FPGA_PROGRAM_B
FPGA_DONE
FPGA_INITB
DBG_RXD
DBG_TXD
CPU_SSC
PC[0..15]
PE[0..7]
EXT_IRQ0
U_FPGA_CPU_EBI1
FPGA_CPU_EBI1.SchDoc
ARM_CLK
U_Power_Supply
Power_Supply.SchDoc
Power_Good
+3V0_VM53_EN
U_External WatchDogs
External WatchDogs.SchDoc
ARM_WD_RST
ARM_WD_INT
ARM_WD_SCL
ARM_WD_SDA
FPGA_WD
FPGA_CLK
FPGA_DIN
U_FPGA_Configuration
FPGA_Configuration.SchDoc
+3V0_VM53_EN
ARM_NRST
FPGA_NRST
QDR2_VTT_GOOD
FPGA_CCLK
ARM_IRQ
ARM_DMARQ
ARM_PROGRAM_B
FPGA_MAIN_CLK_N
FPGA_MAIN_CLK_P
PPS_IN
PPS_OUT
U_FPGA_POWER_DGND
FPGA_POWER_DGND.SchDoc
U_Connectors
Connectors.SchDoc
FPGA_INIT_B
FPGA_DONE
FPGA_JTAG
EXT_PROGRAM_B
FPGA_RS232_TXD
FPGA_RS232_RXD
SDA_TMP
SCL_TMP
DMTD_CLK_N
DMTD_CLK_P
QDRII_CLKS
SPI0
U_CPU_memory
CPU_memory.SchDoc
FBOOT_SEL
U_RS232_and_USB_ports
RS232_and_USB_ports.SchDoc
RS232_CPU_DEBUG_TXD
RS232_CPU_DEBUG_RXD
FPGA_GCLK_P
FPGA_GCLK_N
U_FPGA_QDRII
FPGA_QDRII.SchDoc
FREE_GC2_P
FREE_GC2_N
FREE_GC1_P
FREE_GC1_N
QDR2_2
QDR2_1
SYST_MON_N[0..7]
SYST_MON_P[0..7]
U_QDRII_mem
QDRII_mem.SchDoc
QDRII_2
QDRII_1
FPGA_GTX.SchDoc
U_FPGA_GTX
MGTREFCLK
MGTRX112PN
MGTRX113PN
MGTRX114PN
MGTRX115PN
MGTRX116PN
MGTTX112PN
MGTTX113PN
MGTTX114PN
MGTTX115PN
MGTTX116PN
USB_DDM
USB_DDP
USB_5VBus
RS232_MNG
FPGA_RS232_TXD
FPGA_RS232_RXD
U_FPGA_PLLs
FPGA_PLLs.SchDoc
QDRII_CLKS
EXTREF125MHZOUT
DMTDCLK_mB_P
DMTDCLK_mB_N
DMTDCLK_MAIN_P
DMTDCLK_MAIN_N
uTCA_CLK
PLL_CONTROL
CLK10MHZ_EXT
CLK_125MHZ_EXT_N
CLK_125MHZ_EXT_P
CLK_25MHZ_GTX_DAC
CLK_25MHZ_DMTD_DAC
CLK_25MHZ
U_FPGA_System_Monitor
FPGA_System_Monitor.SchDoc
GTX_DAC_OUT
DMTD_DAC_OUT
U_uTCA_Tongue3
uTCA_Tongue3.SchDoc
DAC_CONTROL
U_CPU_JTAG_Power_PLL
CPU_JTAG_Power_PLL.SchDoc
ARM_WD_RST
WD_NRST
EXT_NRST
CPU_JTAG
U_CPU_100M_Ethernet
CPU_100M_Ethernet.SchDoc
ETH_100MHz
U_FPGA_GPIOs
FPGA_GPIOs.SchDoc
FPGA_GPIO[0..39]
U_FPGA_CLKs
FPGA_CLKs.SchDoc
EXTREFIN_125M
EXTREFIN_10M
EXTREFIN_10M_RET
EXTPPSIN
EXTPPSOUT
FPGA_25MHZ_CLK_P
FPGA_25MHZ_CLK_N
Title
Size
A2
Number
Revision
Date: 31/03/2011
Sheet of
File: D:\White Rabbit\SCB\SCB_MAIN.SchDoc
Drawn By:


IC33A
BANK 12
IO_L0P_12
IO_L0N_12
IO_L1P_12
IO_L1N_12
IO_L2P_12
IO_L2N_12
IO_L3P_12
IO_L3N_12
IO_L4P_12
IO_L4N_VREF_12
IO_L5P_12
IO_L5N_12
IO_L6P_12
IO_L6N_12
IO_L7P_12
IO_L7N_12
IO_L8P_SRCC_12
IO_L8N_SRCC_12
IO_L9P_MRCC_12
IO_L9N_MRCC_12
IO_L10P_MRCC_12
IO_L10N_MRCC_12
IO_L11P_SRCC_12
IO_L11N_SRCC_12
IO_L12P_VRN_12
IO_L12N_VRP_12
IO_L13P_12
IO_L13N_12
IO_L14P_12
IO_L14N_VREF_12
IO_L15P_12
IO_L15N_12
IO_L16P_12
IO_L16N_12
IO_L17P_12
IO_L17N_12
IO_L18P_12
IO_L18N_12
IO_L19P_12
IO_L19N_12
AD25 TxFD12_P
AD26 TxFD12_N
AE27 TxFD11_P
AD27 TxFD11_N
AH33 TxFD10_P
AH32 TxFD10_N
AE28 TxFD9_P
AE29 TxFD9_N
AJ34 TxFD8_P
AH34 TxFD8_N
AF28 TxFD7_P
AF29 TxFD7_N
AL34 +3V3_PG
AK34 SPI1_MOSI
AH29 SPI1_MISO
AH30 +1V2_cpu_PG
AN33 FREE_SRCC_P
AN34 FREE_SRCC_N
AG27 SPI1_SPCK
AG28
AF30 FREE_MRCC_P
AG30 FREE_MRCC_N
AF26 +1V0_GTX_PG
AE26 +3V3_PLL_PG
AJ31 +2V5_PLL_PG
AJ32 +1V2_GTX_PG
AJ29 SPI1_NPCS0
AJ30
AK33 RxFD12_P
AK32 RxFD12_N
AL31 RxFD11_P
AK31 RxFD11_N
AM33 RxFD10_P
AL33 RxFD10_N
AN32 RxFD9_P
AM32 RxFD9_N
AP32 RxFD8_P
AP33 RxFD8_N
AL30 RxFD7_P
AM31 RxFD7_N
XC6VLX130T-1FF1156C
FREE_GC_P
FREE_GC_N
FREE_GC_P
FREE_GC_N
GND
J3
QSS-016-01-L-D-DP
+2V5
GND
Power-Good
+1V0_GTX_PG
+3V3_PLL_PG
+2V5_PLL_PG
+1V2_GTX_PG
+3V3_PG
+1V2_cpu_PG
Power_Good
SPI1
SPI1_MISO
SPI1_MOSI
SPI1_SPCK
SPI1_NPCS0
SPI1_MISO
SPI1_MOSI
SPI1_SPCK
SPI1_NPCS0
Title
Size
A4
Number
Revision
Date: 31/03/2011
Sheet of
File: D:\White Rabbit\..\SMI_Link_7-12.SchDoc
Drawn By:


SMI links 1-6 -> fabric E
CN4C
TxFE-6+ TxFE-6- RxFE-6+ RxFE-6-
TxFE-5+ TxFE-5- RxFE-5+ RxFE-5-
TxFE-4+ TxFE-4- RxFE-4+ RxFE-4-
TxFE-3+ TxFE-3- RxFE-3+ RxFE-3-
TxFE-2+ TxFE-2- RxFE-2+ RxFE-2-
TxFE-1+ TxFE-1- RxFE-1+ RxFE-1-
UTCA_MCH_TONGUE3
SMI links 1-6 -> fabric D
CN4A
TxFD6_P TxFD6_N RxFD6_P RxFD6_N
TxFD5_P TxFD5_N RxFD5_P RxFD5_N
TxFD4_P TxFD4_N RxFD4_P RxFD4_N
TxFD3_P TxFD3_N RxFD3_P RxFD3_N
TxFD2_P TxFD2_N RxFD2_P RxFD2_N
TxFD1_P TxFD1_N RxFD1_P RxFD1_N
TxFD-6+ TxFD-6- RxFD-6+ RxFD-6-
TxFD-5+ TxFD-5- RxFD-5+ RxFD-5-
TxFD-4+ TxFD-4- RxFD-4+ RxFD-4-
TxFD-3+ TxFD-3- RxFD-3+ RxFD-3-
TxFD-2+ TxFD-2- RxFD-2+ RxFD-2-
TxFD-1+ TxFD-1- RxFD-1+ RxFD-1-
UTCA_MCH_TONGUE3
CN4B
RSVD GND
GND
UTCA_MCH_TONGUE3
GND
IC33C
BANK 14
IO_L0P_14 IO_L0N_14 IO_L1P_14 IO_L1N_14 IO_L2P_14 IO_L2N_14 IO_L3P_14 IO_L3N_14 IO_L4P_14 IO_L4N_VREF_14 IO_L5P_14 IO_L5N_14 IO_L6P_14 IO_L6N_14 IO_L7P_14 IO_L7N_14 IO_L8P_SRCC_14 IO_L8N_SRCC_14 IO_L9P_MRCC_14 IO_L9N_MRCC_14 IO_L10P_MRCC_14 IO_L10N_MRCC_14 IO_L11P_SRCC_14 IO_L11N_SRCC_14 IO_L12P_VRN_14 IO_L12N_VRP_14 IO_L13P_14 IO_L13N_14 IO_L14P_14 IO_L14N_VREF_14 IO_L15P_14 IO_L15N_14 IO_L16P_14 IO_L16N_14 IO_L17P_14 IO_L17N_14 IO_L18P_14 IO_L18N_14 IO_L19P_14 IO_L19N_14
TxFD6_P TxFD6_N TxFD5_P TxFD5_N TxFD4_P TxFD4_N TxFD3_P TxFD3_N TxFD2_P TxFD2_N TxFD1_P TxFD1_N
PLL_SYNC DAC_DMTD_DIN DAC_REF_DIN PLL_SDO PLL_SDI DAC_DMTD_SYNC DAC_DMTD_SCLK DAC_REF_SYNC DAC_REF_SCLK PLL_CS PLL_SCLK PLL_STAT PLL_LOCK PLL_RESET PLL_REFSEL
RxFD6_P RxFD6_N RxFD5_P RxFD5_N RxFD4_P RxFD4_N RxFD3_P RxFD3_N RxFD2_P RxFD2_N RxFD1_P RxFD1_N
XC6VLX130T-1FF1156C
DAC_CONTROL
DAC_DMTD_DIN DAC_DMTD_SYNC DAC_DMTD_SCLK DAC_REF_DIN DAC_REF_SYNC DAC_REF_SCLK
DAC_CONTROL
PLL_CONTROL
PLL_CS PLL_STAT PLL_LOCK PLL_RESET PLL_REFSEL PLL_SCLK PLL_SDO PLL_SDI PLL_SYNC
PLL_CONTROL
Title
Size A4
Number
Revision
Date: 31/03/2011
Sheet of
File: D:\White Rabbit\SCB\uTCA_Tongue3.SchDoc
Drawn By: