EEE 3208

Communication Theory Lab

Experiment No: 05

Experiment Name: Study of Time Division Multiplexing System

Submitted by,

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Year : 3rd
Semester: 2nd
Section: C2

Objective: The target of this experiment is to be familiar with the concept of Time division multiplexing and Observe the waveforms of multiplexed and demultiplexed signals in a 4-Ch TDM system to learn the significance of synchronization in TDM systems.

Answer-1:

Time Frames (or Frames)

- In Time Division Multiplexing, the available channel bandwidth is used by multiple signals in different time slots.
- A **time frame** consists of one complete cycle of time slots allocated to each channel in the system. For example, if there are N channels, a single frame has N distinct time slots—one for each channel.
- After one frame is finished (i.e., each channel has “spoken” once), the process repeats with the next frame.

Synchronization

- Synchronization ensures that the receiver (demultiplexer) knows which time slot corresponds to which channel.
- A **synchronizing (sync) pulse** or special synchronization pattern is often inserted into the time-multiplexed signal so that the receiver can lock onto the start of each frame.
- If the transmitter and receiver clocks drift out of alignment, the demultiplexer might assign the wrong samples to the wrong channels, causing signal distortion. Hence, a **synchronization mechanism** (like a PLL or a frame-sync signal) is crucial.

Answer-2:

Modulation Technique

- In many introductory TDM experiments, **Pulse Amplitude Modulation (PAM)** is used. Each channel’s analog signal is sampled in rapid succession, creating a series of amplitude pulses—one set for each channel—within a frame.

Is the Signal Purely Digitized?

- **PAM** alone is not fully digitized because it involves sampling analog waveforms and transmitting them as pulses of varying amplitude.
- To be fully digitized (like PCM), you would need to add **quantization** and **binary encoding** after sampling.
- Therefore, basic TDM with PAM is not a pure digital signal. It is discrete in time (pulses) but still analog in amplitude.

Answer-3:

A typical TDM system has these blocks:

1. Input Channels: Multiple analog inputs (e.g., CH-0, CH-1, etc.).
2. PAM Sampler / Multiplexer (MUX):
    - Samples each channel in a round-robin fashion, assigning each channel a time slot.
    - A clock or counter determines when each channel is sampled.
3. Summer / Amplifier (optional depending on design):
    - Combines the time-multiplexed pulses into one composite signal.
    - Adjusts amplitude if needed for transmission.
4. Transmitter:
    - Sends the multiplexed pulse train over the communication medium.
    - May include drivers or filters as required.
5. Synchronization Block:
    - Generates the frame-sync signals or special sync pulses.
    - Ensures the receiver knows when each frame starts.
6. Receiver:
    - Receives the composite time-multiplexed signal.
    - Often includes a clock recovery circuit or uses an external clock input.
7. Demultiplexer (DMUX):
    - Routes each sampled pulse back to its respective channel by “opening” the correct output gate at the correct time slot.
8. Low Pass Filters (LPF):
    - Smooth out the pulses to recover the original analog waveforms.
    - Remove high-frequency sampling components.

The necessity of each block is straightforward:

- MUX/DMUX handle channel separation in the time domain.
- Synchronization/clock ensures correct time slot alignment.
- Filters reconstruct the original analog signals.

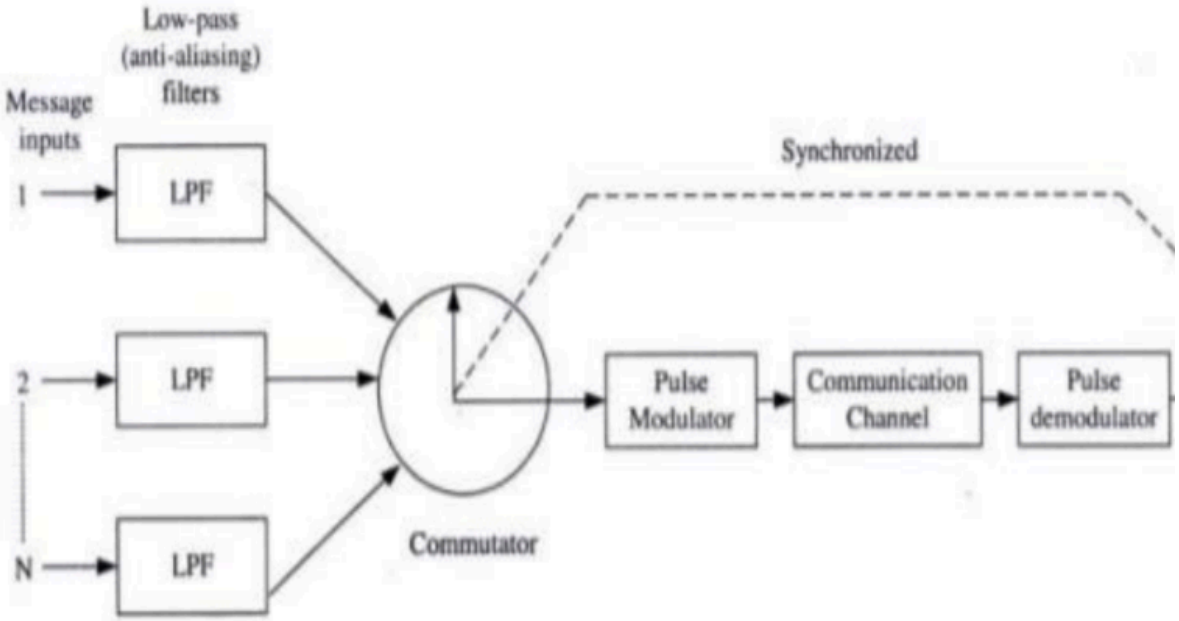


Fig. Block Diagram of TDM Transmitter

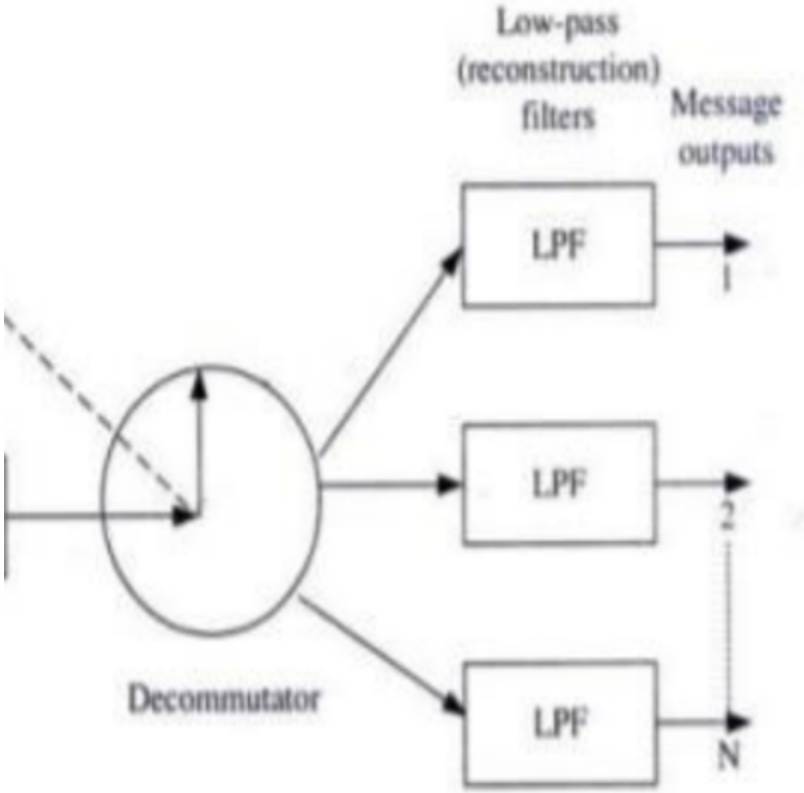


Fig. Block Diagram of TDM Reciever

Answer-4:

In many TDM setups, you have two key frequencies:

- : The main clock frequency that drives the sampling/multiplexing.
- (sometimes labeled channel frequency or “channel clock”): The effective rate at which each channel is sampled.

We know, $T2 = 4T1$. so, $F2 = F1 / 4$

Depending on notation, $f_{clk} = 4f_{cho}$ or, $T_{clk} = T_{cho} / 4$

- Interpretation: If the clock is running at 4 times the channel sampling rate, then for every single “channel sample,” the system might have 4 smaller subdivisions, which can be used for other channels or for synchronization overhead.
- The exact factor “4” depends on how many channels and whether there is a dedicated sync pulse slot, etc.

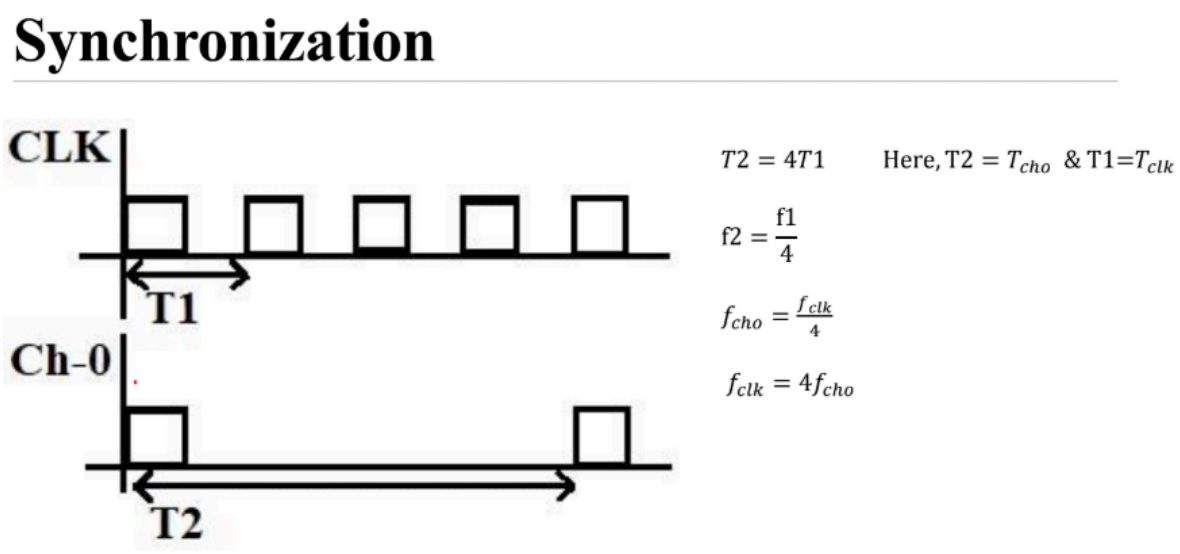


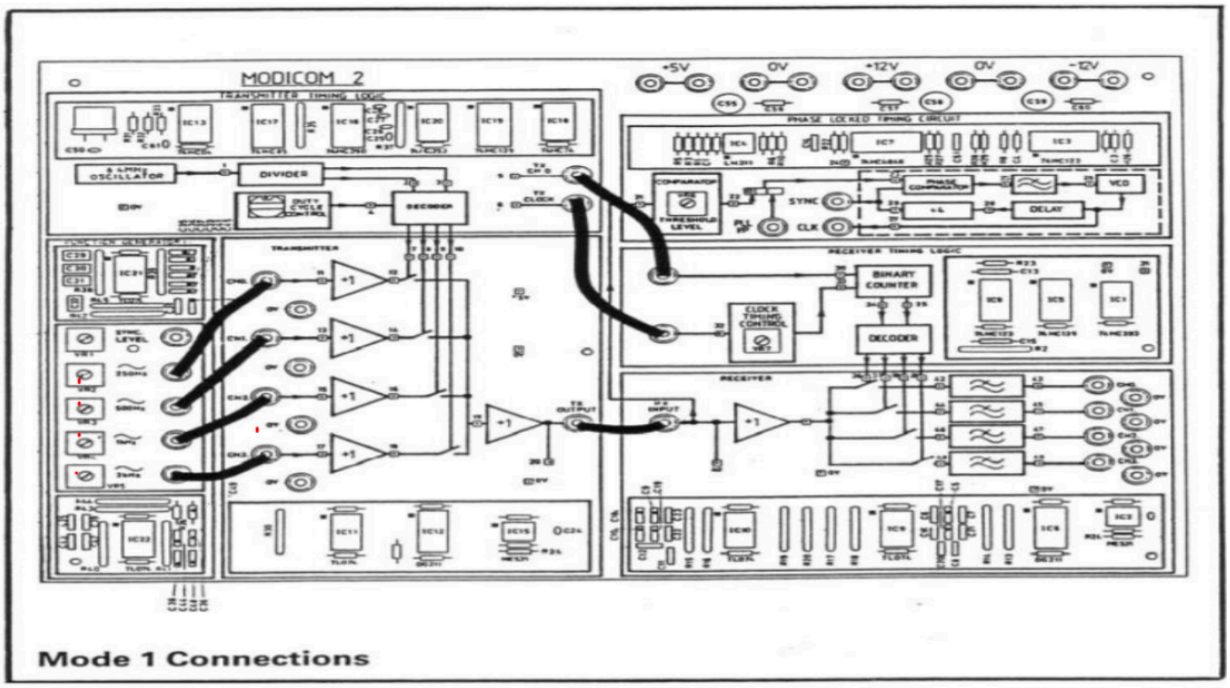
FIG: timing diagram showing how the higher-frequency clock ticks multiple times for each channel sample slot, ensuring each channel can be sampled in turn.

Answer-5:

According to the typical experimental setup:

- **Connections**:
  - TX CH-0 → RX CH-0
  - TX CLOCK → RX CLOCK
  - TX OUTPUT → RX OUTPUT
- **Principle**:
  - Only one channel (CH-0) is connected directly from the transmitter to the receiver.
  - The clock from the transmitter is also fed directly to the receiver, ensuring both ends run at the same sampling rate.
  - The output of the TDM multiplexer (though it might only be carrying one channel) is connected to the receiver's demultiplexer input.
  - Because there is only one channel, the demultiplexer essentially routes the single time slot back out to CH-0 with minimal complexity.
- **Outcome**:
  - You observe that the single channel's signal is transmitted and recovered with the correct timing.
  - This mode demonstrates the most basic TDM functionality and verifies that the clock and sampling system are working.

Mode-1 Connection



Mode 1 Connections

Answer-6:

Additional Connection:

- TX CH-0 → PLL Input
- TX OUTPUT → RX OUTPUT (the multiplexed signal line remains the same)

Role of the PLL (Phase-Locked Loop):

1. The PLL is used to **recover or regenerate** a clean clock signal from the incoming TDM signal (or from a channel reference).
2. A PLL locks onto the frequency/phase of an input reference (e.g., a portion of the TDM signal or a dedicated pilot tone).
3. Once locked, the PLL output is a stable clock used for synchronization at the receiver end.

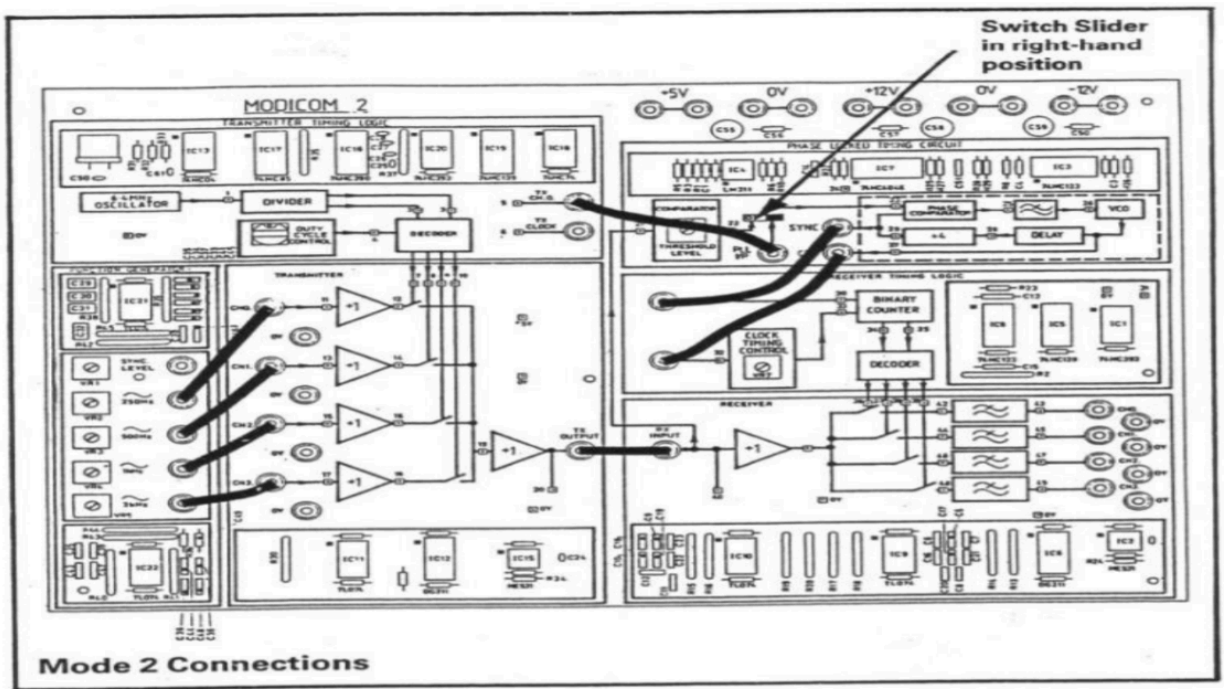
Principle:

- The system checks how well the PLL can track the frequency/phase of the input signal.
- The PLL's output then drives the demultiplexer timing or further synchronization blocks to ensure correct gating of the time slots.

Detailed Description of PLL Block:

- A PLL typically has a **phase detector**, a **low-pass filter**, and a **voltage-controlled oscillator (VCO)**.
- The phase detector compares the input reference signal with the VCO output, generating an error voltage proportional to their phase difference.
- The low-pass filter smooths the error voltage, which in turn adjusts the VCO to match the input frequency/phase.
- This process continues until the VCO output is locked to the reference input.

Mode-2 Connection



Answer-7:

Additional Connection:

- The comparator is introduced between the TX output and the receiver or sometimes as part of a sync detection circuit.

Role of the Comparator:

1. A comparator is often used to transform an analog or noisy pulse into a clean digital-like signal (0 V or 5 V, for instance).

2. If the TDM signal or the sync pulses vary in amplitude, the comparator “squares” them off for more reliable detection.

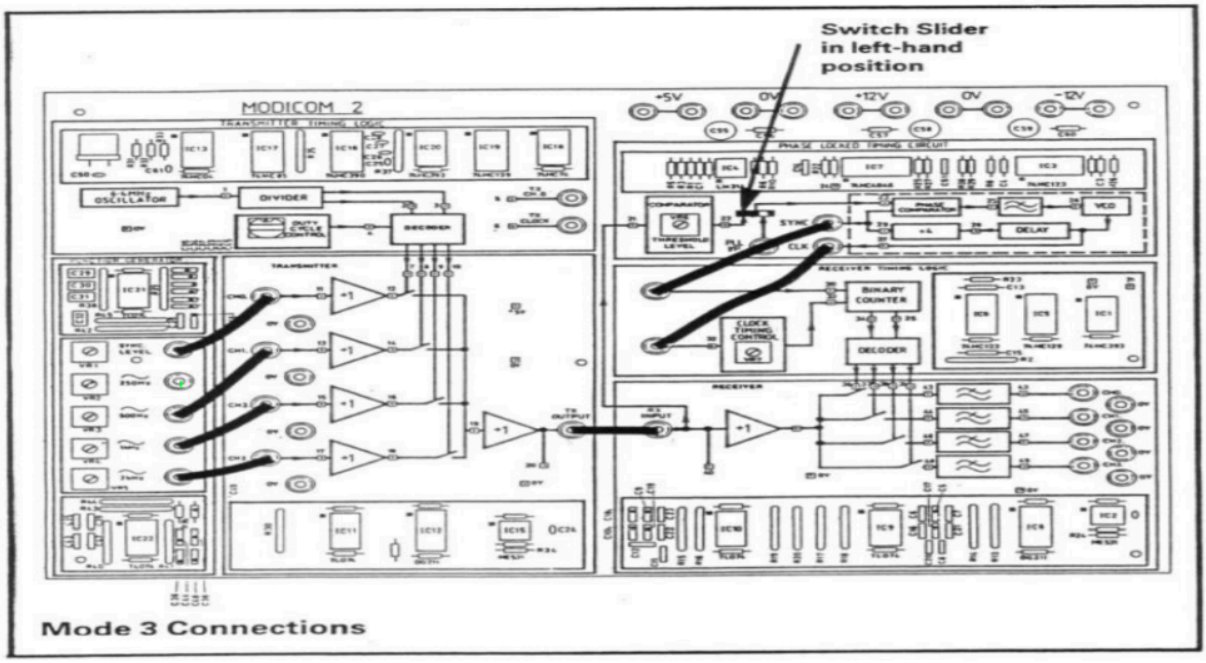
Detailed Description of Comparator Block:

- A comparator has two inputs, V1V_1V1 and V2V_2V2. If V1>V2V_1 > V_2V1>V2, the output might be 5 V (logic high), and if V1<V2V_1 < V_2V1<V2, the output might be 0 V (logic low).
- By setting a threshold or reference voltage, the comparator effectively cleans up the signal edges, creating a stable logic output that can be fed to counters or other digital circuits for synchronization or demultiplexing.

Principle:

- In Mode–3, the system checks how well the comparator helps in shaping the TDM pulses or the sync signal.
- This is crucial if the TDM link experiences amplitude distortion or if the receiver needs a crisp digital edge for clock/demux circuits.

Mode-3 Connection



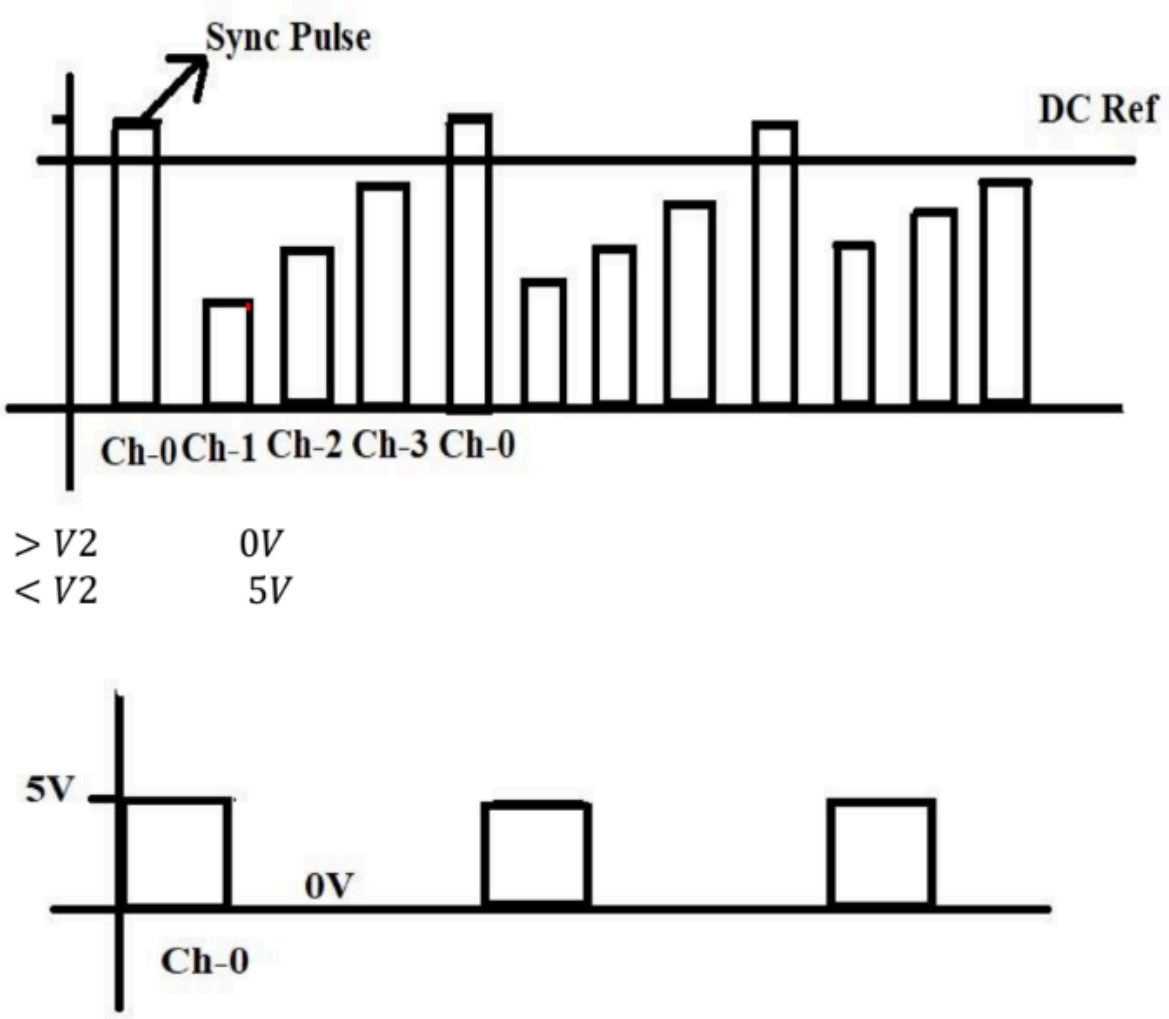


FIG: block diagram showing the comparator input and output waveforms

Wave Shapes Images from Digital Oscilloscope:

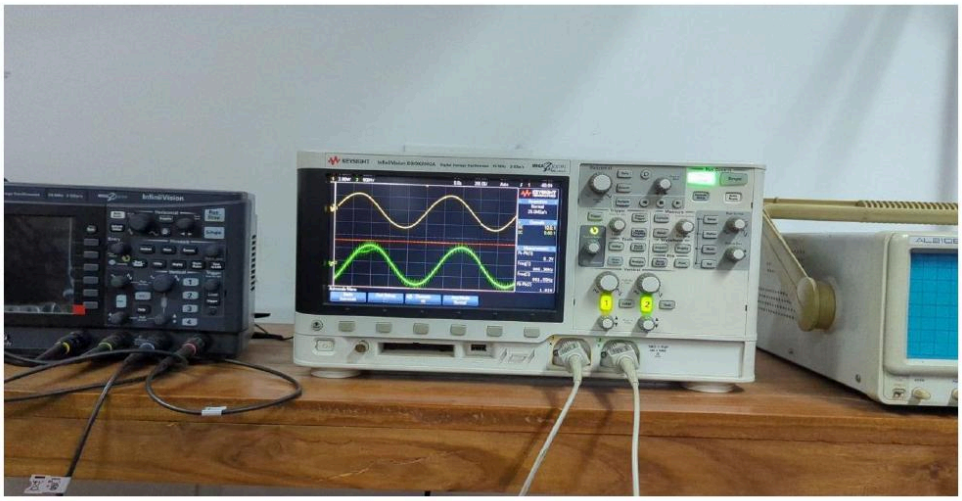


Fig_1: Wave shape of Message Signal (3 no) and Reconstructed Signal of 1 kHz by using Mode of Operation-1

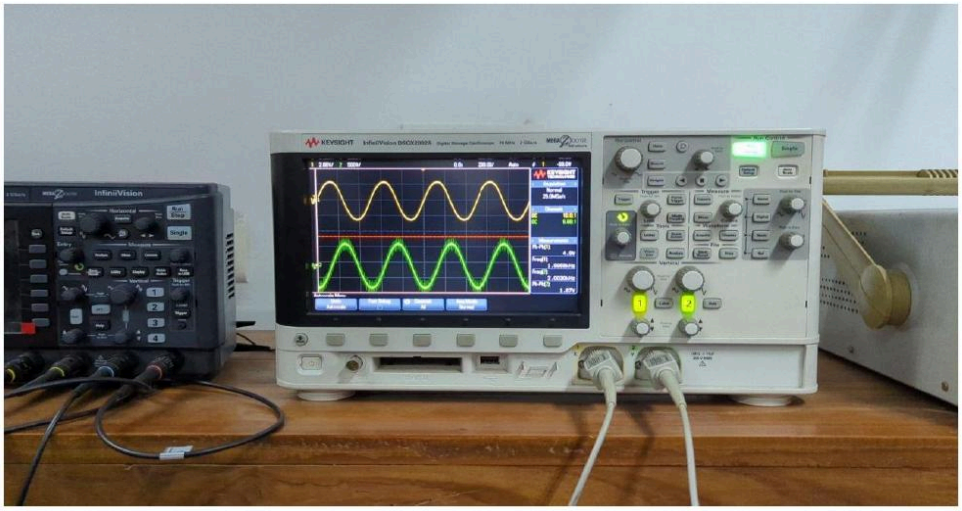


Fig_2: Wave shape of Message Signal (4 no) and Reconstructed Signal of 2 kHz by using Mode of Operation-2

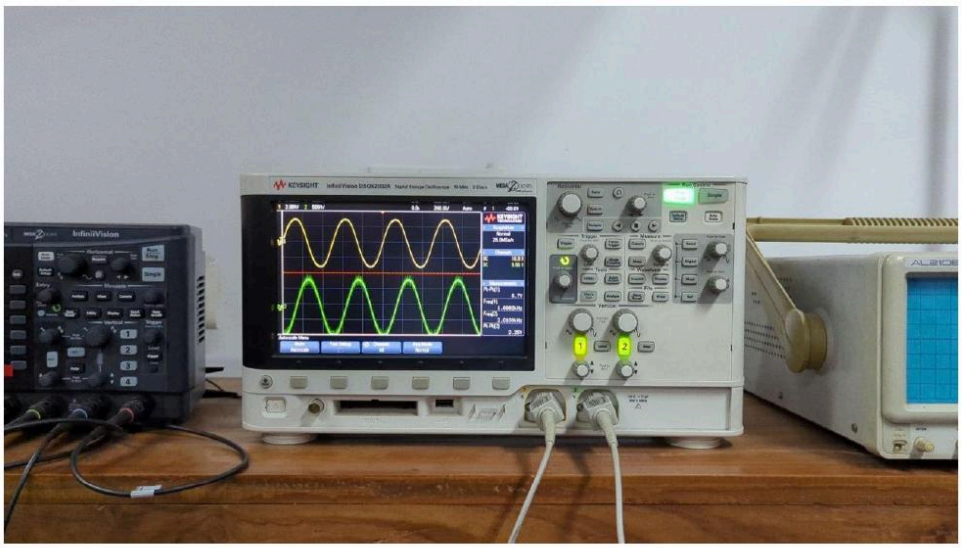


Fig_3: Wave shape of Message Signal (4 no) and Reconstructed Signal of 2 kHz by using Mode of Operation-3

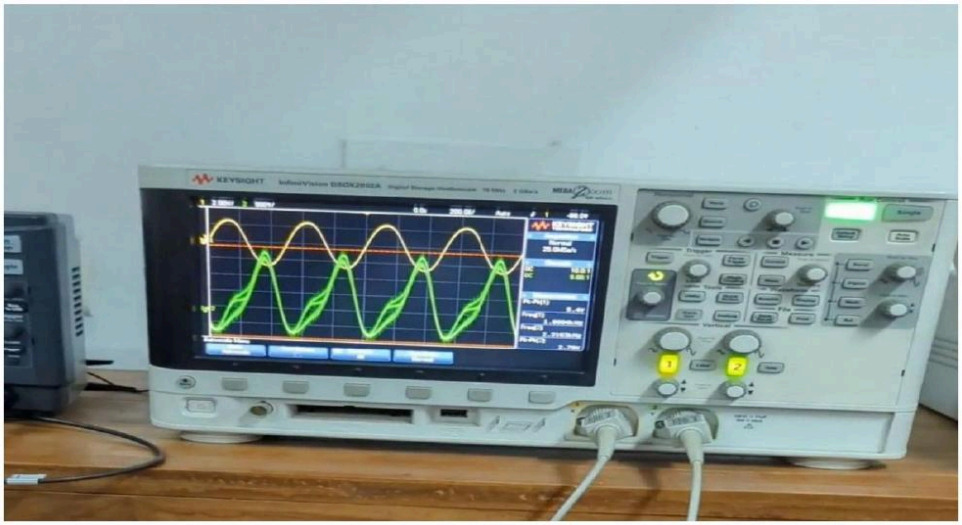


Fig_4: Wave shape of Message Signal (4 no) and Reconstructed Signal When Dc Reference is Set tom the Below of Threshold Value

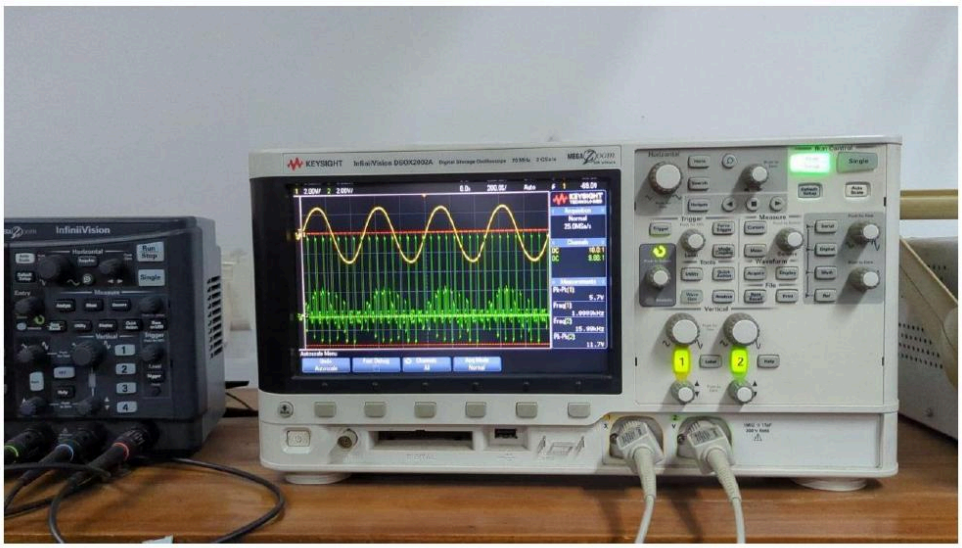


Fig_5: Wave shape of Message Signal and TDM Signal

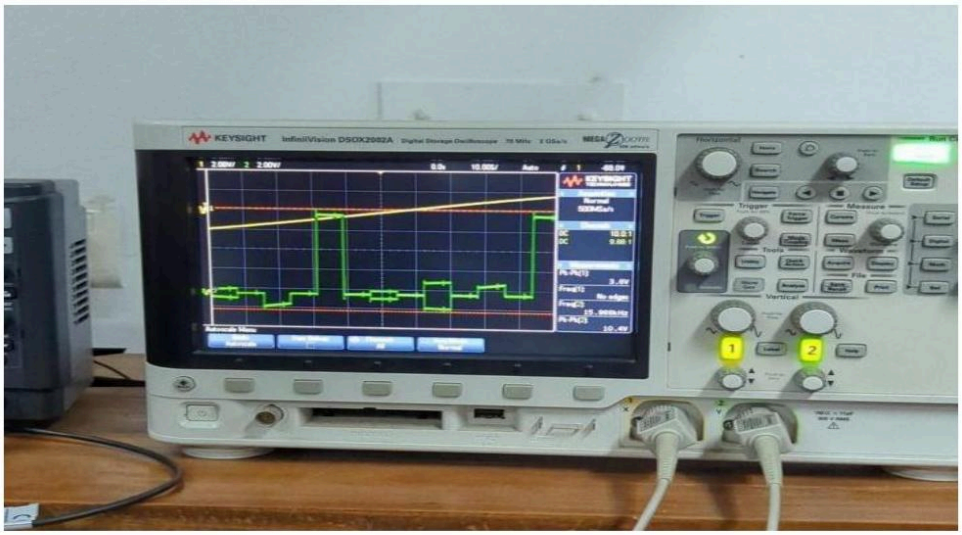
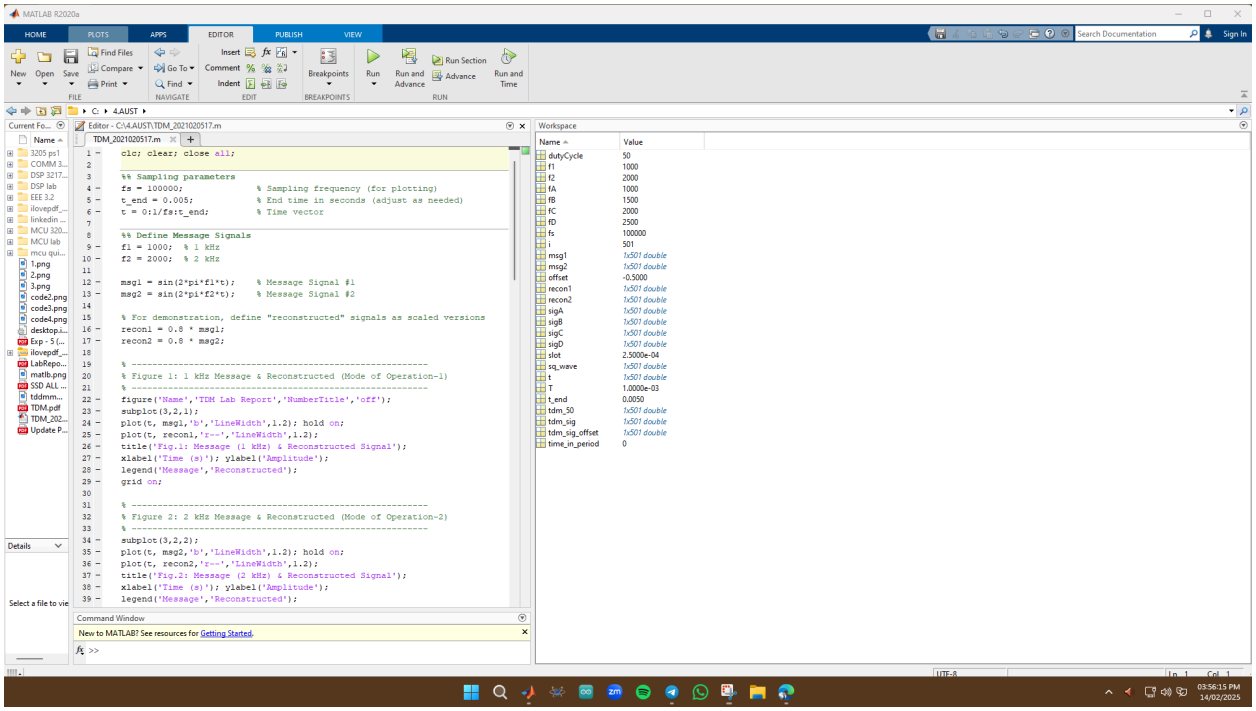
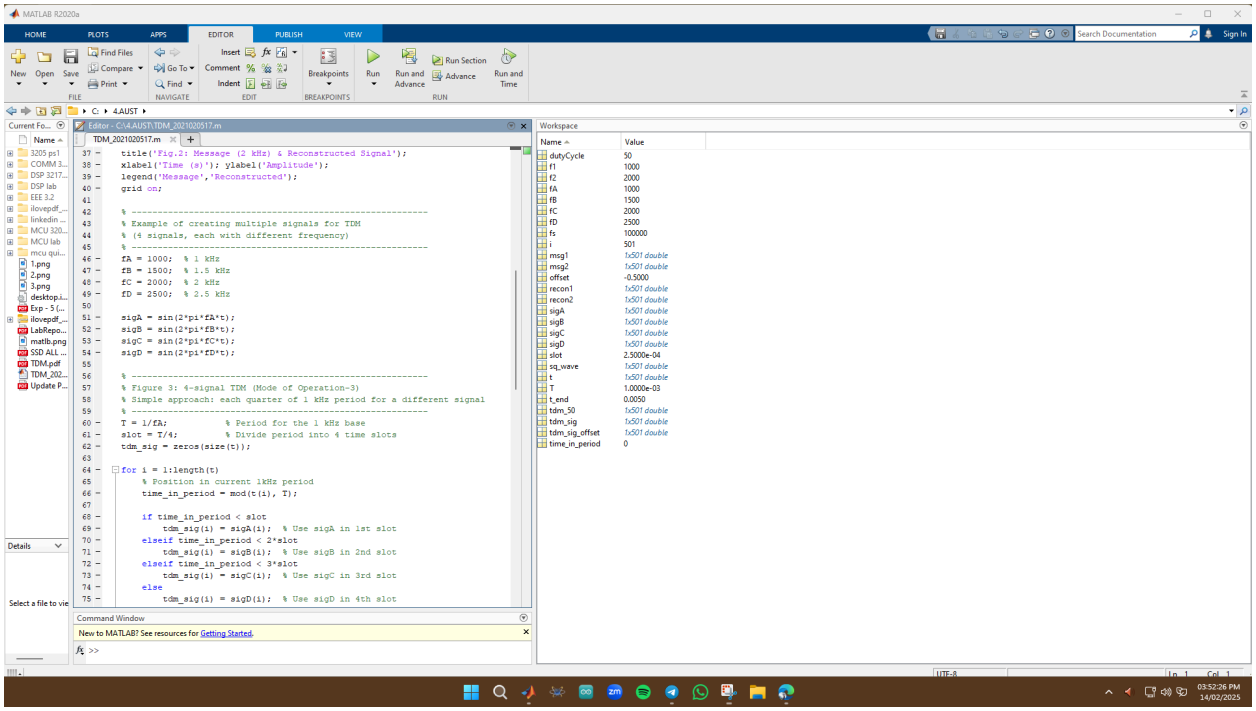
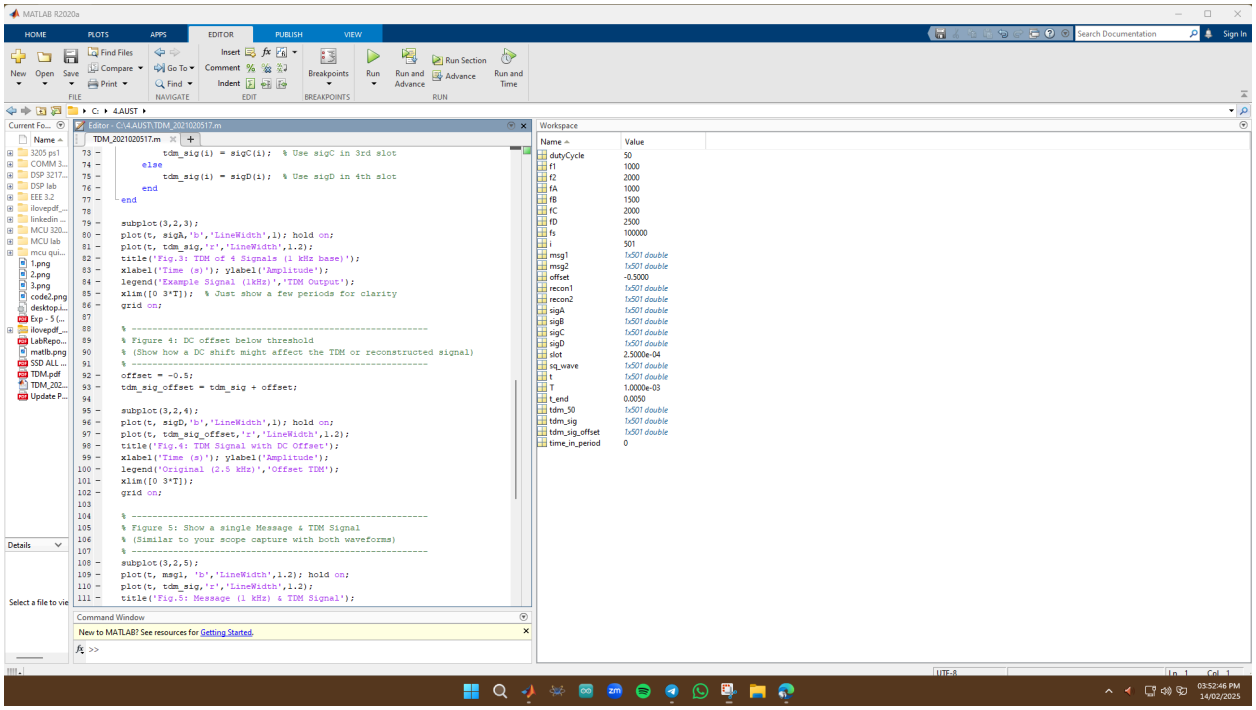


Fig_6: Wave shape of Message Signal and TDM Signal [Duty Cycle 50%]

MATLAB code and waveshapes:



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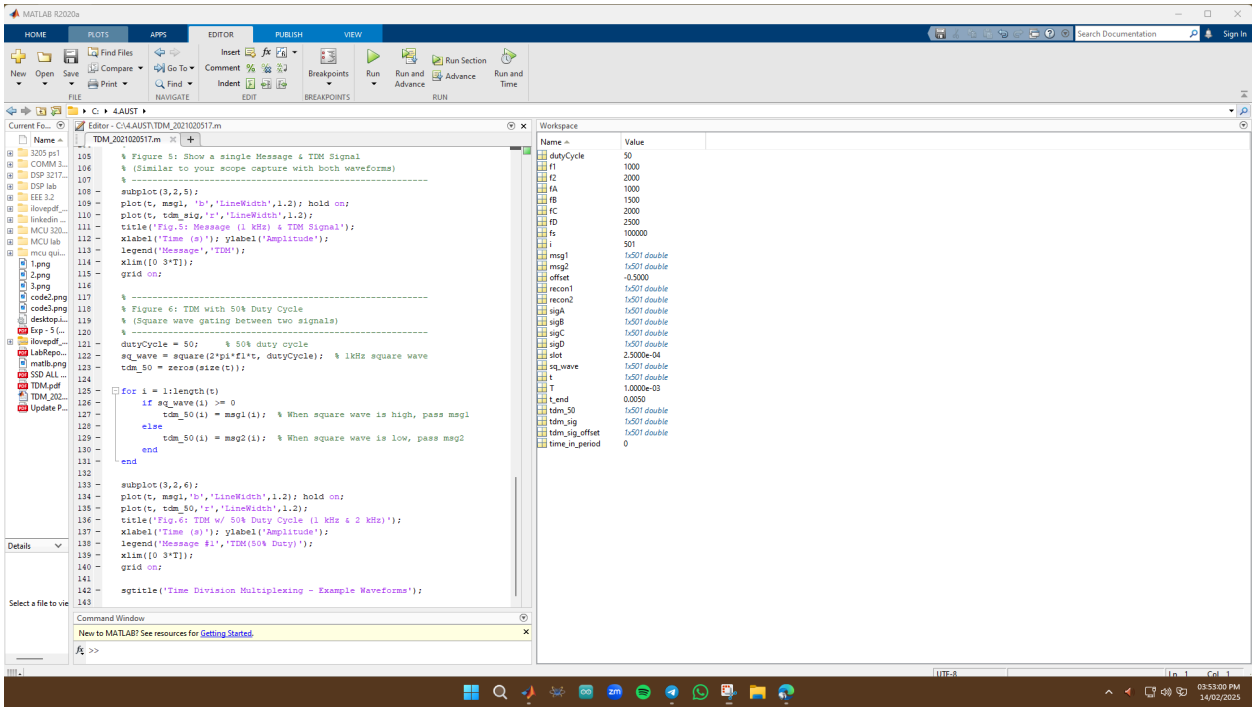
New to MATLAB? See resources for Getting Started.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TDM Lab Report

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Time Division Multiplexing - Example Waveforms

Fig.1: Message (1 kHz) & Reconstructed Signal

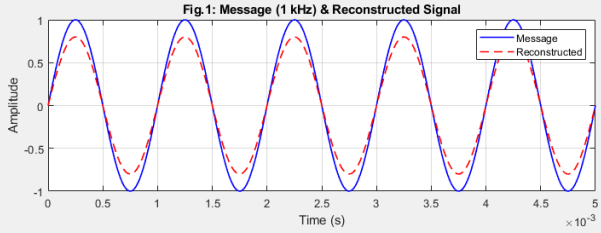


Fig.2: Message (2 kHz) & Reconstructed Signal

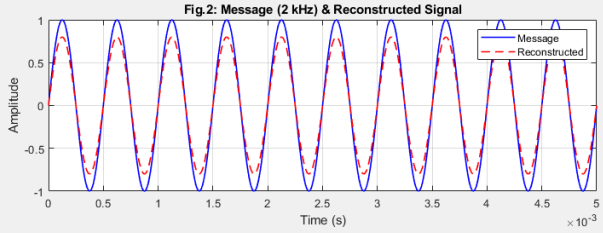


Fig.3: TDM of 4 Signals (1 kHz base)

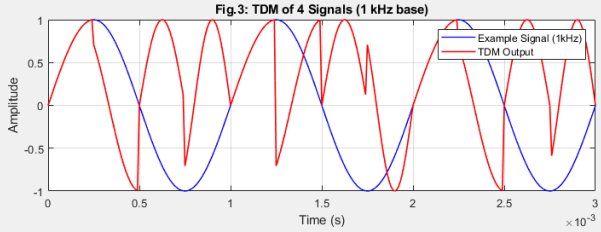


Fig.4: TDM Signal with DC Offset

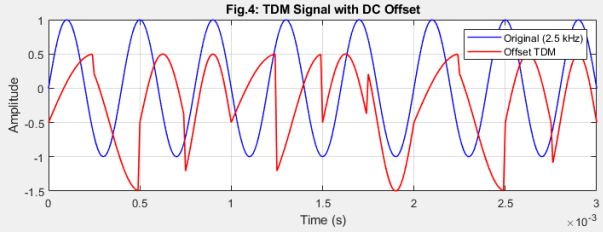


Fig.5: Message (1 kHz) & TDM Signal

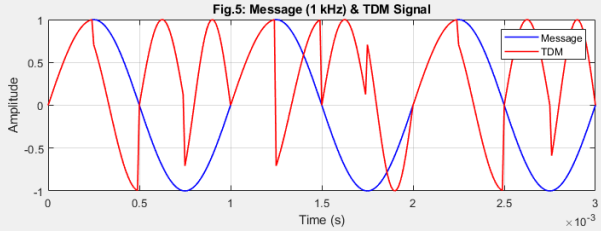
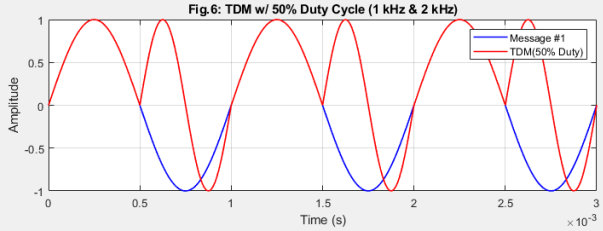


Fig.6: TDM w/ 50% Duty Cycle (1 kHz & 2 kHz)



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DISCUSSION:

Time division multiplexing is used in mobile, router, gaming, optical fibre etc. to make our daily life easier. Multiple user can use a same transmission channel where time is separated for each user. In the experiment, 4 frames were used for 4 users with a time division of T/4. Data of 4 users go through Commutator and synchronization which makes sure to send the data to the desired person. We used Pulse Amplitude Modulation to make the analog signal into discrete signal first. We used multiple LPF before commutator because different users have different frequency. Since, Fm=3.4kHz, Fs = 2x3.4kHz +/- 10% is used in real life as cuttoff frequency. We use LPF after decommutator to reduce noise of channel. Ch-0 channel maintains synchronization. Based on Data, clock and channel, 3 modes can be used. Signal can't be reconstructed if DC ref voltage is too low of DC sync voltage is too low. Increasing Duty cycle increases the visibility of signal.