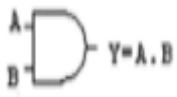
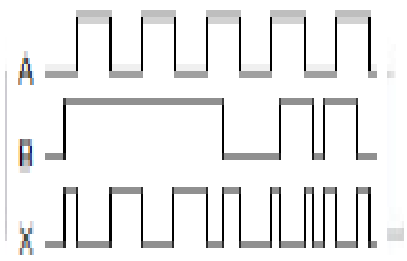
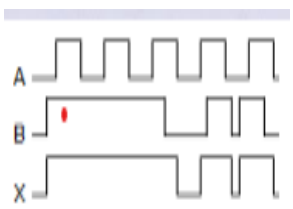
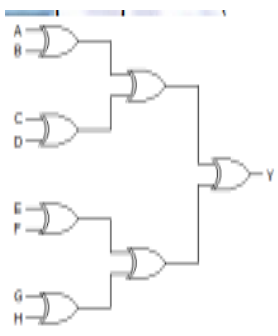
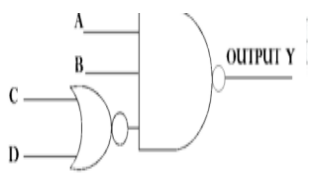
L J Institute of Engineering and Technology, Ahmedabad.

Digital Electronics (DE) Practice Book (Sem-III 2025)

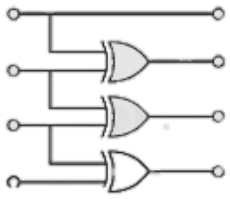
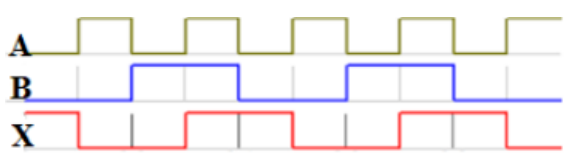
Note: This Practice Book is only for reference purpose. LJU Test question paper may not be completely set from Practice Book.

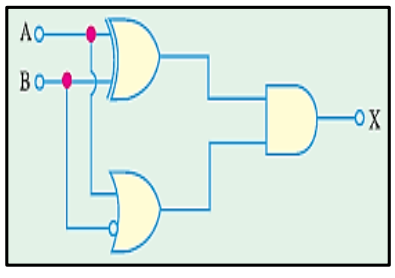
Sr. No.	unit_number	question_text	answer_text	marks	option A	option B	option C	option D
1	1	The given hexadecimal number (1E.53)16 is equivalent to _____.	b	1	(35.684)8	(36.246)8	(34.340)8	(35.599)8
2	1	The octal number (651.124)8 is equivalent to _____.	a	1	(1A9.2A)16	(1B0.10)16	(1A8.A3)16	(1B0.B0)16
3	1	The octal equivalent of the decimal number (417)10 is _____.	a	1	(641)8	(619)8	(640)8	(598)8
4	1	(170)10 is equivalent to _____.	c	1	(FD)16	(DF)16	(AA)16	(AF)16
5	1	Convert (214)8 into decimal.	a	1	(140)10	(141)10	(142)10	(130)10
6	1	Convert (0.345)10 into an octal number.	b	1	(0.16050)8	(0.26050)8	(0.19450)8	(0.24040)8
7	1	Convert the binary number (01011.1011)2 into decimal.	a	1	(11.6875)10	(11.5874)10	(10.9876)10	(10.7893)10
8	1	Convert binary to octal: (110110001010)2 =?	b	1	(5512)8	(6612)8	(4532)8	(6745)8
9	1	Which of the following is not a positional number system?	a	1	Roman Number System	Octal Number System	Binary Number System	Hexadecimal Number System
10	1	The value of radix in binary number system is _____.	d	1	4	1	10	2
11	1	The binary equivalent of the decimal number 10 is _____.	c	1	10	100	1010	101
12	1	The octal equivalent of 1100101.001010 is _____.	b	1	624.12	145.12	154.12	145.21
13	1	The hexadecimal number for (95.5)10 is _____.	(5F.8) 16	1				
14	1	The hexadecimal number ‘A0’ has the decimal value equivalent to _____.	160	1				
15	1	The decimal equivalent of hex number 1A53 is _____.	6739	1				
16	1	_____be the decimal equivalent of 111011.10.		1				
17	1	Given that (16)10 = (100)x, find the value of x.	d	2	X=10	X=1	X=8	X=4
18	1	(4433)5 = ( )10 = ( )2		2				
19	1	1) (673.124)8 = ( )2 2) (4522.25)10 = ( )2 3) (FACE)16 = ( )10 4) (10101010)2 = ( )8 = ( )16		4				
20	1	Convert following Octal Number to Hexadecimal and Binary 414, 574, 725.25.	(10C,17C,1D5.54)16 , (100001100, 101111100, 111010101.010101)2	3				
21	1	Convert the number (435)7into equivalent radix-10 and radix-4 number system.		3				
22	1	Do as directed: (10110100)2= (?)gray = (?)XS-3 = (?)BCD		3				
23	1	(i) Convert (75)10 = (_____)2 (ii) Convert (101011)2 = (_____)10 (iii)Convert (10101101)2 = (_____)16 = (_____)8		3				
24	1	Convert the decimal number 225.225 to binary, octal and hexadecimal.		3				
25	1	Convert following numbers. (a)(4021.2)5 = ( )10 (b) (B65F)16= ( )10 (c) (630.4)8 = ( )10 (d) (41)10 = ( )8		2				
26	1	Convert the following Hexadecimal numbers to Octal. (a) 4F7.A8 (b) BC70.0E (c) 42FD		3				
27	1	Convert following Hexadecimal Number to Decimal B28, FFF, F28	(2856,4095,3880)10	2				
28	1	(1011011101101110)2 = ( )16	(B76E)16	1				
29	1	Convert the decimal number 187 to 8-bit binary.	a	1	(10111011)2	(11011101)2	(10111101)2	(10111100)2
30	1	Convert the decimal number 250.5 to base 3, base 4, base 7 and base 8 .		4				
31	1	Convert (4BAC)16= ( )8 = ( )4 = ( )2 = ( )10. Show all steps of conversion.		2				
32	1	Express decimal number 60.875 into binary form.		1				
33	1	Convert the following numbers form given base to the base indicates. 1. (AEF2.B6)16 = (_____)2 2. (674.12)8 = (_____)10 3. (110110.1011)2 = (_____)16		2				
34	1	Express decimal number 10.875 into binary form.		2				
35	1	Convert the Decimal Number 412.5 to base 3, 4 and 7		3				
36	1	Nibble means_____	b	1	2 bit	4 bit	8 bit	16 bit
37	1	Convert the binary number (1001.0010)2 to decimal.	b	2	90.125	9.125	125	12.5
38	1	i. Convert (FFFF)16=(_____)10. ii. Convert (125.625)10=(_____)2.		2				
39	1	(52)10 = ( )2	(110100)2	1				
40	1	(436)8 = ( )16		1				
41	1	(5C7)16 = ( )10	(1479)10	1				
42	1	(11011.101)2 = ( )10	(27.625)10	1				
43	1	Convert following 1. (4E7.2)16 = (?)8 2. (521.3)8 = (?)2		2				
44	1	Convert (10101101)2 = (_____)16 = (_____)8		2				
45	1	(734)8 = ( )16	d	1	C1D	DC1	1CD	1DC
46	1	(1111.11)2 = (?)8 = (?)10		2				
47	1	(AEF2.B6)16 = (_____)2		1				
48	1	(674.12)8 = (_____)10		1				
49	1	(110110.1011)2 = (_____)16		1				
50	1	(101001011)2 = ( )10		1				
51	1	(11101110)2 = ( )8		1				
52	1	(68)10 = ( )16		1				
53	1	Consider the equation (123)5 = (x8)y with x and y as unknown. The number of possible solutions is _____.	3	1				
54	1	(1217)8 is equivalent to_____	c	1	(1217)16	(2297)10	(028F)16	(0B17)16
55	1	(73)x (in base x number system) is equal to (54)y (in base y number system), the possible values of x and y are	d	2	8,16	8,10	10,12	8,11
56	1	Which of the following number is not allowed in radix – 7 (base 7) system?	b	1	666	739	461	124
57	1	If (2.3)4 + (1.2)4 = y4, then value of y in base 4 system.	a	1	10.1	10.01	10.2	1.02
58	1	If (2.3)4 + (1.2)4 = Y10, then value of Y in base 10 system?	a	2	4.25	10.1	10.01	3.5
59	1	The Octal equivalent of hexadecimal number AB.CD is _____	a	1	253.632	253.314	526.314	526.632
60	1	Which number system has a base 16?	d	1	Octal	Binary	Decimal	Hexadecimal

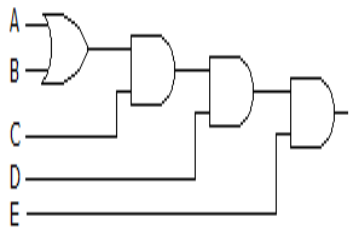
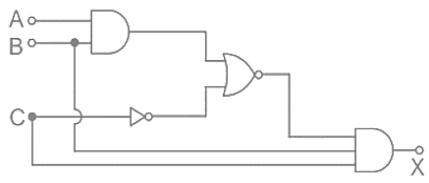
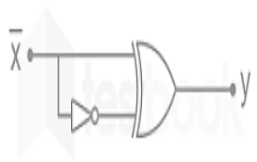
61	1	What is Digital Electronics?	d	1	Engineering of devices that produce digital signal	Field of electronics involving the study of digital signal	Engineering of devices that accepts digital signals	All of the mentioned
62	1	Convert the following numbers as directed: (130)10= ( )2	b	1	(10000011)2	(10000010)2	(10000111)2	(111001)2
63	1	Convert the following numbers as directed: (1011011)2= ( )10	d	1	(91)8	(52)10	(41)10	(91)10
64	1	Convert (B65F)16 = ( )10.	c	1	(44526)10	(78864)10	(46687)10	(48756)10
65	1	Convert (41)10 = ( )2.	d	1	(110011)2	(111000)2	(101010)2	(101001)2
66	1	Convert decimal number (43)10 to binary.	c	1	(110110)2	(101010)2	(101011)2	(111001)2
67	1	Convert octal number (234)8 to hexadecimal.	a	1	(9C)16	(8C)16	(9C)8	(9C)2
68	1	Convert decimal number (0.252)10 to binary.	b	1	(0.00001)2	(0.010000)2	(1.010000)2	(10.00100)2
69	1	Convert the Hexadecimal numbers to Octal: 4F7.A8		2				
70	1	Convert the Hexadecimal numbers to Octal: BC70.0E		2				
71	1	A number (1217)8 can be represented as _____	d	1	$(656)_{10}$	$(01010001111)_2$	$(28F)_{16}$	Both B and C
72	1	The number (100000)2 would appear just immediately after –	d	1	$(37)_8$	(1F)16	(11111)2	All A,B and C
73	1	$(F23.23)_{16} = (?)_8 = (?)_2$	c	1	7442.106, 111100100011.00100011	7442.106, 111110100011.00100011	7443.106, 111100100011.00100011	7443.106, 111100000001.00100011
74	1	If $(154)_b / (14)_b = (8)_{10}$ then what is the value of radix 'b' ?	b	1	10	7	12	8
75	1	How many number of '1' would be appeared in binary representation of -3×512+5×64+7×8+3 ?	d	1	7	5	6	9
76	1	Convert (DEAD)16 into equivalent radix-10 and radix-8 number system.		2				
77	1	Consider the equation (129)5 = (x9)y with x and y as unknown. The number of possible solutions is _____.	a	1	not possible	5	3	4
78	1	convert (FFFF)16 to decimal & octal numbers respectively.	d	1	a) 65235 &177787	b)62325 & 177878	c)65335 & 177878	d)65535 &177777
79	1	The binary equivalent of (11.6275)10 is equals to _____.	d	1	a)101.11011	b)1011.1001	c)101.0011	d)1011.1010
80	1	Convert the hexadecimal number (9999.9999) to octal number.	d	1	a) 1414631.463144	b) 463144.114631	c) 141361.114631	d) 114631.463144
81	1	Which of the following is equivalent to decimal number of (BFA0) hexadecimal number ?	c	1	a) 90456	b) 40956	c) 49056	d) 56049
82	1	Consider the following statements i) octal number is 1/4th the length of corresponding binary number ii) Hexadecimal is 1/3rd length of corresponding binary number iii) In 10 bit binary number, 512 is the weight of 2nd digit from MSB.Which of statement/s is/are not correct from above ?	a	1	a) i,ii,iii	b) i, ii only	c) i, iii only	d) ii, iii only
83	1	Convert the following numbers as per required: (i) (965.198)10 = (?)16 (ii) (3B.4)16 = (?)8 (iii) (1110011100.110001)2 = (?)10 = (?)16		3				
84	1	Convert the decimal number 279.5 to base 3 and 7.		2				
85	1	The hexadecimal equivalent of largest binary number with 14-bits is?	a	1	3FFF	7FFF	8FFF	None of Above
86	2	The 2's complement of the number 1101101 is _____.	10011	1				
87	2	2's complement of any binary number can be calculated by adding 1's complement twice.	False	1				
88	2	The 2's complement of the number 1101110 is _____.	0010010	1				
89	2	*Substract* $(45)_8$ from $(66)_8$ using 2's complement method.		2				
90	2	*Substract* $(45)_{10}$ from $(93)_{10}$ using 1's Complement Method.	(48)10	2				
91	2	Subtract using 2's complement method. $(10010 - 10011)_2$		2				
92	2	Perform subtraction of $(78 - 58)_{10}$ using 2's complement method.		2				
93	2	Using 10's complement, subtract : $(72532\text{-}3250)_{10}$		2				
94	2	Using 2's complement, subtract : $(1010100 - 1000100)_2$		2				
95	2	Perform the subtraction with the following numbers using 1's complement and 2's complements: (a) 11010-1101, (b) 10010-10011		4				
96	2	Perform the operation of subtractions with the following binary number using 2's complement (i) 10010 – 10011 (ii) 100 – 110000 (iii) 11010 – 10000		6				
97	2	Find the 10's complement of the following: (1) $(6106)_{10}$ (2) $(935)_{10}$		4				
98	2	Perform following subtraction using 2's complement method. (11010)2 – (10000)2		2				
99	2	Subtract (32)10 from (58)10 using 8-bit 2's complement arithmetic.		2				
100	2	Substract 14 from 46 using 8-bit 2's complement arithmetic.		2				
101	2	Substract 27.50 from 68.75 using 12-bit 1's complement arithmetic.		2				
102	2	Add the following binary numbers: 1. 11011 + 1101 2. 1010.11 + 1101.0 + 1001.11+1111.11		2				
103	2	Substract the following binary numbers. 1. 1100.10-111.01 2. 10110-1011		2				
104	2	The addition of these binary numbers 101001+ 010011 would generate:	C	1	101110	000111	111100	010100
105	2	The 1's complement of a binary number is obtained by changing ____	C	1	Each 1 to a 0	Each 0 to 1	Each 1 to 0 and each 0 to 1	None of Above
106	2	Substract the following hexadecimal numbers using the 1's complement arithmetic. (i) $48_{16} - 26_{16}$ (ii) $45_{16} - 74_{16}$		4				
107	2	Substract the following hexadecimal numbers using the 2's complement arithmetic. (i) $69_{16} - 43_{16}$ (ii) $27_{16} - 73_{16}$		4				
108	2	Substract the following decimal numbers using the 9's and 10's complement arithmetic. (i) $274_{10} - 86_{10}$ (ii) $376.3_{10} - 765.6_{10}$		4				

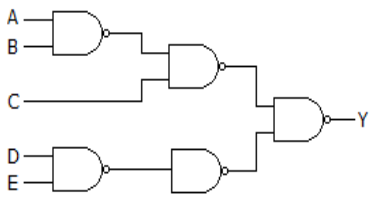
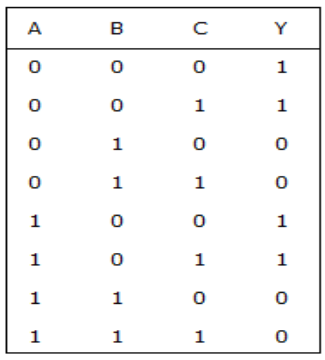
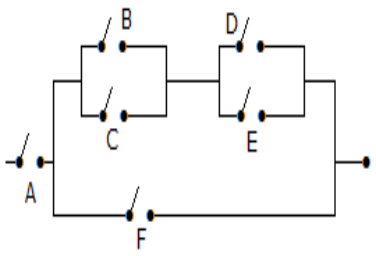
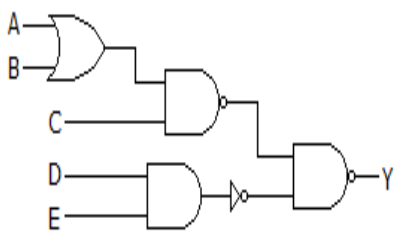
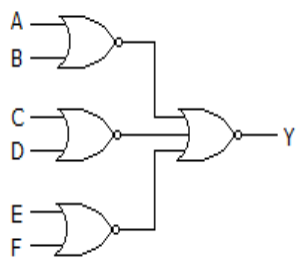
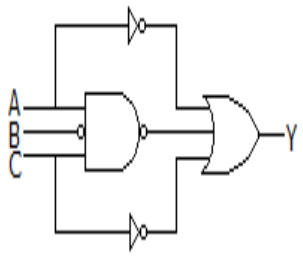
109	2	Substract the following decimal numbers using 2's complement arithmetic: 1. 46 - 19 2. 36.75 - 89.5		4				
110	2	Substract the following numbers using 9's complement: 745.81 - 436.62		2				
111	2	Substract the following numbers using 10's complement: 416.73 - 2928.54		2				
112	2	Express -45 and -73.75 in 2's complement form.		2				
113	2	Add 47.25 to 55.75 using binary arithmetic.		2				
114	2	Add -75 to +26 using 8 bit 2's complement arithmetic.		2				
115	2	Substract the following decimal numbers using 1's complement arithmetic: 1. 46-84 2. 63.75-17.5		4				
116	2	Find out Y, if B = 1 and A = square wave 		1				
117	2	Which gate is equivalent to bubbled OR gate?	D	1	AND	XOR	NOT	NAND
118	2	A NOT gate has…	A	1	1 input and 1 output	2 input 1 output	1 input 2 output	none of above
119	2	If a 3-input NOR gate has eight input possibilities, how many of those possibilities will result in a HIGH output	B	1	2	1	7	8
120	2	If a signal passing through a gate is inhibited by sending a LOW into one of the inputs, and the output is HIGH, the gate is a(n):	B	1	AND	NAND	NOR	OR
121	2	Implement Boolean expression for Ex-OR gate using NAND gates only.		3				
122	2	The output of a ____ gate is only 1 when all of its inputs are 1.	C	1	OR	NOT	AND	EXOR
123	2	The inputs of a NAND gate are connected together. The resulting circuit is ……	C	1	OR	AND	NOT	NONE OF ABOVE
124	2	The NOR gate is OR gate followed by ……	C	1	AND	NAND	NOT	NONE OF ABOVE
125	2	The NAND gate is AND gate followed by ……	A	1	NOT	OR	NOR	NONE OF ABOVE
126	2	Exclusive-OR (XOR) logic gates can be constructed from ……..logic gates.	C	1	OR GATES ONLY	AND gates and NOT gates	AND, OR, NOT Gates	OR gates and NOT gates
127	2	The basic logic gate whose output is the complement of the input is …….	C	1	OR	AND	INVERTER	NONE OF ABOVE
128	2	The universal gate is ……	D	1	EXOR	NAND	NOR	BOTH (B) AND (C)
129	2	The NAND gate output will be low if the two inputs are _____.	1&1	1				
130	2	The output of a logic gate is 1 when all its inputs are at logic 0. the gate is either _____.	(a NOR or an EX-NOR)	1				
131	2	_____ AND gates are required to realize Y = CD+EF+G	B	1	1	2	3	4
132	2	The following waveform pattern is for _____ 	EXOR GATE	1				
133	2	The following waveform pattern is for _____ 	OR GATE	1				
134	2	The 8-input XOR circuit shown has an output of Y = 1. Correct input combination below (ordered A – H) is _____. 		1				
135	2	Find the logic required at R input. 	R=1	1				
136	2	For a given logic circuit, if A=B=1, and C=D=0. Find output Y 	0	1				
137	2	Show that $A \oplus B = AB' + A'B$ and construct the corresponding logic diagrams using truth table		3				

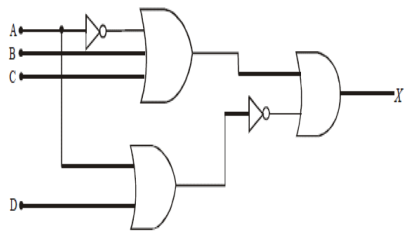
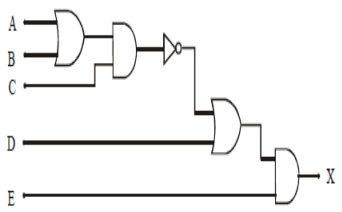
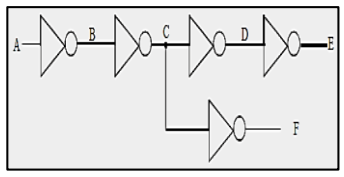
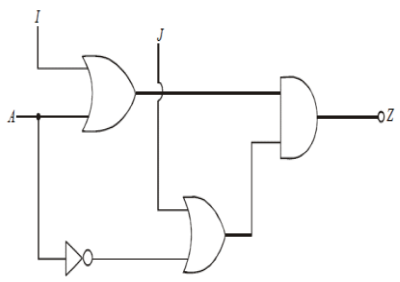
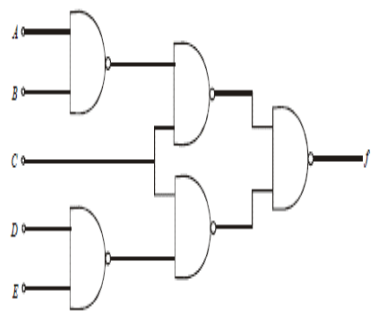
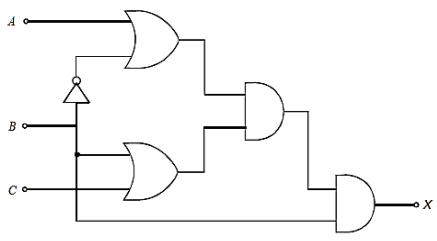
138	2	Show that $A \odot B = AB + A'B'$ = (A⊕B)' = (AB'+A'B)' and construct the corresponding logic diagrams using truth table		3				
139	2	Show that (A+B)(AB)' is equivalent to $A \oplus B$ using truth table		3				
140	2	Derive that logic expression that equals to 1 only when the two bit binary numbers A and B have the same value. Draw the logic diagram and construct the truth table to verify the logic.		3				
141	2	Show that AB + (A+B)' is equivalent to $A \odot B$ using truth table		3				
142	2	Find the logical equivalent of the following expression: (a) $A \oplus 0$ (b) $A \oplus 1$ (c) $A \odot 0$ (d) $A \odot 1$ (e) $0 \oplus A'$		5				
143	2	Draw the logic diagram and construct the truth table for following expression: X= A+B+ (CD)'		3				
144	2	Draw the logic diagram and construct the truth table for following expression: Y= (AB) (A+B)' + (EF)'		3				
145	2	Draw the logic diagram and construct the truth table for following expression: Z = (A'B+CD'+ABC)'		3				
146	2	A calculator performs the binary addition where the 2's complement binary number 1101100 is obtained with no carry , convert the same into BCD	C	1	11000011	00110100	00100000	00110011
147	2	Excess-3 is also known as _____	D	1	Positive weighted code	Negative weighted code	Cyclic code	Self Complementing Code
148	2	Solve: $(11000111)_{XS-3} = (?)_{GRAY}$		2				
149	2	The specific non-weighted code is used in shaft encoder for the process based instrumentation and data acquistion system that initiates encoder sequence with 01111 to the second sequence as 11111 then evaluate would be the equivalent binary number as per sequence?	A	1	01010 to 10101	01111 to 11111	10000 to 100000	01011 to 10111
150	2	The transmitter transmits the 8-bit of information in form of data packet as D0 (LSB) to D7 (MSB) where D0 defines the odd parity bit, D1 as start bit ='1', D2 to D5 as data bits = $(8)_{2421}$ number and D6 and D7 as stop bits='01' respectively in a transreceiver digital communication system. Evaluate D0	B	1	1	0	01	don’tcare
151	2	Which of the following is true? 1. (A+B).(AB)' = A XOR B 2. AB+(A+B)' = A XNOR B 3. A XOR B' = A XNOR B	D	1	ONLY 1	ONLY 2	ONLY 3	ALL OF THE ABOVE
152	2	$(000100100011)_{BCD} = ()_2$	1111011	1				
153	2	Which of the following statements are true? 1. The codes 8421,2421,5211,3321,4311 are some of the positively weighted codes. 2. The codes 642-3, 631-1, 84-2-1, 74-2-1 are some of the negatively weighted codes. 3. Non-weighted codes do not obey the position-weighting principle.	C	1	Both 1 and 2	both 2 and 3	all are true	all are false
154	2	The specific non-weighted code is used in shaft encoder for the process based instrumentation and data acquistion system that initiates encoder sequence with 10101 to the second sequence as 10111 then evaluate would be the equivalent binary number as per sequence?	C	1	10101 to 10111	00000 to 11111	11001 to 11010	11010 to 11011
155	2	Which of the following statements are true? 1. An XOR gate produces an output 1 only when the inputs are not equal. 2. An XNOR gate produces an output 1 only when the inputs are equal. 3. An XOR is also called anti-coincidence gate. 4. An XNOR is also called coincidence gate.	C	1	Both 1 and 2	both 2 and 3	all are true	all are false
156	2	The excess-3 code of decimal 7 is represented by_____.	B	1	0111	1010	0011	0100
157	2	Covert the Gray code 1101 to binary	1001	1				
158	2	Do as directed: 1. Convert the gray code 11011 into decimal.		4				
159	2	Convert decimal 86 into BCD, excess-3 and Gray code. $(10101101)_2 = ()_{BCD} = ()_{GRAY}$		3				
160	2	Convert $(96)_{10}$ to its equivalent Gray code and EX-3 code		4				
161	2	Convert $(10000110)_{BCD}$ to decimal, binary & octal.		3				
162	2	$(396)_{10} = ()_{BCD} = ()_{GRAY} = ()_{XS-3}$		3				
163	2	Decimal 43 in Hexadecimal and BCD number system is respectively _____	B	1	B2, 0100 0011	2B, 0100 0011	2B, 0011 0100	B2, 0100 0100
164	2	Solve: $(101011)_2 + (001111)_2 = ()_{10} = ()_{16}$		2				
165	2	The 2's complement of the binary number 1001001 in XS-3 is ____		1				
166	2	Given A = P XOR Q, B= P XOR Q' and C= PQ, find output Y = A OR B OR C as per data.		2				
167	2	Solve: $(10100101)_{XS-3} = ()_{GRAY}$		2				
168	2	A processor started the operation with reflected code as one bit of change at a time when code is moving from one state to another. The obtained code in one state as 111011 and went to 111001. Convert corresponding code into binary equivalent.		1				
169	2	The transmitter transmits the 8-bit of information in form of data packet as D0 (LSB) to D7 (MSB) where D0 defines the odd parity bit, D1 as start bit ='1', D2 to D5 as data bits = $(F)_{16}$ number and D6 and D7 as stop bits='01' respectively in a transreceiver digital communication system. Evaluate D0	A	1	1	0	01	don’tcare
170	2	Subtract 745.81 from 436.62 given in decimal using 9’s complement method.		2				

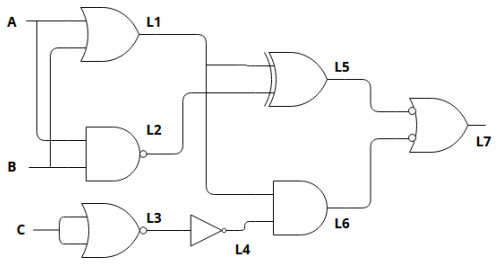
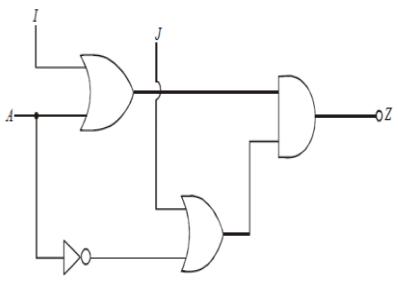
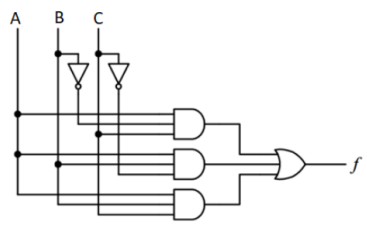
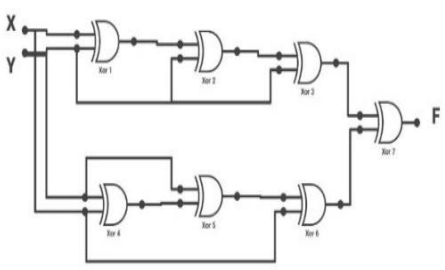
171	2	Solve: (101011)2 - (001111)2 = (?)10 = (?)16		2				
172	2	The quantity (337)10 can be represented in Excess-3 code as:	D	1	100000011001	11000110111	11000111010	11001101010
173	2	Which of the following statements is/are correct for Excess-3 code? 1. It is a self-complementing code. 2. The binary sum of a code and its 1's complement is equal to 1111. 3. It is a weighted code. 4. The binary sum of a code and its 2's complement is equal to 1111. 5. Complement can be generated by inverting each bit pattern.	C	1	all 1, 4, 5	only 1 & 4	all 1, 2 ,5	only 2 & 3
174	2	The given logic circuit represents - 	C	1	4-bit binary to decimal converter	4-bit gray to binary converter	4-bit binary to gray converter	4-bit XS-3 to decimal converter
175	2	Unit distance code is the other name of -	B	1	Sequential code	Cyclic Code	Self complementing code	2421 BCD code
176	2	Which of the following number/s is/are in invalid format?	D	1	$(CAFE)_{16}$	$(5208)_{8}$	$(110000101101)_{XS-3}$	Both B and C
177	2	Which of the following is not an invalid BCD code?	C	1	1011	1010	1001	1100
178	2	An Excess-3 code for the number $(FD)_{16}$ is given by _____	C	1	0010 0101 0011	0011 0010 1000	0101 1000 0110	0101 1001 0110
179	2	Subtract $(3250)_{10}$ from $(72532)_{10}$ using 10's complement method.		2				
180	2	If a 3-input NAND gate has eight input possibilities, how many of those possibilities will result in a HIGH output?	A	1	7	1	3	4
181	2	The 2421 and Excess-3 code of decimal 6 is represented by_____.	A	1	1100 and 1001	1100 and 1100	0110 and 1001	1100 and 0110
182	2	The transmitter transmits the 8-bit of information in form of data packet as D0 (LSB) to D7 (MSB) where D0 defines the even parity bit, D1 as start bit ='1', D2 to D5 as data bits = (5)10 in 84-2-1 code and D6 and D7 as stop bits='10' respectively in a transreceiver digital communication system. Evaluate D0.	D	1	8	2	0	1
183	2	Which Logic operation should be performed between A and B for a given output X? 	A	1	XNOR	XOR	OR	NAND
184	2	Substract 75.125 from 84.625 using 12-bit 1's complement arithmetic.		2				
185	2	BCD equivalent code of octal number (1431)8 is	d	1	1.00101E+11	11100000010	1.001E+11	11110010011
186	2	Convert XS-3 number (11000111) into gray code	d	1	1110011	110110	1100111	1110001
187	2	Subtract (741.41)16 from (436.6)16 by using decimal (r-1) complement method.		3				
188	2	Perform substraction of A – B using binary diminished radix complement , where A is octal number (75) & B is octal number (53).		3				
189	2	Do as directed: a) Convert the gray code 11011 into decimal. b) Convert the decimal 2493 into XS-3 code		2				
190	2	Do as directed : a)Convert the decimal 1525 into gray code. b) convert (10101101)2 to 8421 code & gray code		2				
191	2	A processor started the operation with reflected code as one bit of change at a time when code is moving from one state to another. The obtained code in one state as 110001 and went to 101111. Convert corresponding code into binary equivalent?	a	1	100001 to 110101	101110 to 110101	111111 to 110101	0001 to 111111
192	2	Convert $(19)_{10}$ into XS-3 code and gray code.	b	1	a) (01010000) xs-3 & 11010	b) (01001100) xs-3 & 11010	c) (01001101) xs-3 & 11000	d) (01001110) xs-3 & 10010
193	2	The decimal equivalent of the excess-3 number 110010100011.01110101 is _____.	c	1	1253.75	861.75	970.42	1132.87
194	2	The 10's complement of $(715)_8$ is _____	d	1	359	953	540	539
195	2	$(98.75)_{10}$ is equivalent to _____	d	1	$(142.6)_8$	$(62.C)_{16}$	$(10011000.01110101)_{BCD}$	All of above
196	2	Assign the proper odd parity bit to the code 111001.	b	1	1111011	1111001	111111	0111011
197	2	Which of the following is false? I. A 1-bit gray code has two code words 0 and 1 representing decimal numbers 0 and 1. respectively. II. 2's complement of a 2's complement of a number is the number itself. III. Excess-3 code for 369 is 011110011100.	c	1	Only 1	Only 2	Only 3	All are false
198	2	The 2's complement of the decimal number $(-541)_{10}$ in hexadecimal is ___.	c	1	DEE	DDD	DE3	DED
199	2	$(1111011)_{GRAY} = (\ )_{XS-3}$	a	1	10110101	11111111	10111100	10100101
200	2	Which gates are called universal gates? Design exclusive-OR gate having minimum gates using one of the universal gates.		3				

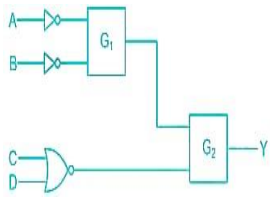
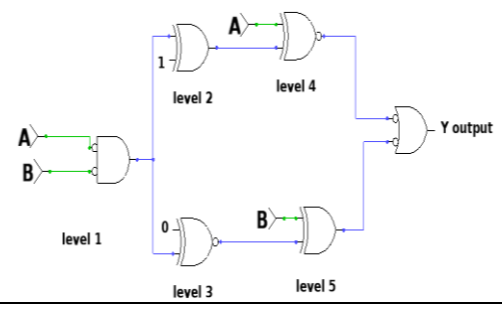
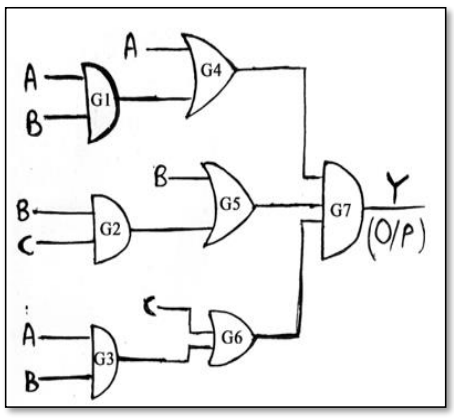
201	2	The transmitter transmits the 8-bit of information in form of data packet as D0 (LSB) to D7 (MSB) where D0 defines the even parity bit, D1 as start bit ='1', D2 to D5 as data bits = (9)10 in 84-2-1 code and D6 and D7 as stop bits='10' respectively in a trans receiver digital communication system. Evaluate D0	B	1	1	0	11	111
202	2	Consider P = $(49.75)_{10}$ and Q = $(55.50)_{10}$. Subtract Q from P using 12-bit 2's complement arithmetic. Express the answer in radix-10 number system.		3				
203	3	What is the use of boolean identities?	A	1	Minimizing the boolean expression	Maximizing the boolean expression	To evaluate logical identity	Searching of logical expression
204	3	_____ is used to implement boolean function.	C	1	Logical notation	Arithmetic logic	Logic gates	expressions
205	3	The boolean function A + BC is a reduced form of _____	B	1	AB + BC	(A + B)(A + C)	A'B + AB'C	(A + C)B
206	3	Simplify Y = AB' + (A' + B)C.	A	1	AB' + C	AB + AC	A'B + AC'	AB + A
207	3	Complement of the expression A'B + CD' is _____	B	1	(A' + B)(C' + D')	(A + B')(C' + D)	(A' + B)(C' + D)	(A + B')(C + D')
208	3	(A + B)(A' B') = ?	A	1	0	1	AB	AB'
209	3	DeMorgan's theorem states that _____	A	1	(AB)' = A' + B'	(A + B)' = A' * B	A' + B' = A'B'	(AB)' = A' + B
210	3	In boolean algebra, the OR operation is performed by which properties?	D	1	Associative properties	Commutative properties	Distributive properties	All of the Mentioned
211	3	The expression for Absorption law is given by _____	A	1	A + AB = A	A + AB = B	AB + AA' = A	A + B = B + A
212	3	According to boolean law: A + 1 = ?	A	1	1	A	0	A'
213	3	The involution of A is equal to _____	A	1	A	A'	1	0
214	3	A(A + B) = ?	D	1	AB	1	0	A
215	3	Find the simplified expression A'BC'+AC'.	C	1	B	A+C	(A+B)C'	AB
216	3	(X + Z)(X + XZ') + XY + Y = ?.	D	1	XY+Z'	Y+XZ'+Y'Z	X'Z+Y	X+Y
217	3	A'(A + BC) + (AC + B'C) = ?.	D	1	(AB'C+BC')	(A'B+C')	(A+ BC)	C
218	3	Simplify the expression XZ' + (Y + Y'Z) + XY.	C	1	(1+XY')	YZ + XY' + Z'	(X + Y +Z)	XY'+ Z'
219	3	Y' (X' + Y') (X + X'Y) = ?	A	1	XY'	X'Y	X + Y	X'Y'
220	3	If an expression is given that x+x'y'z=x+y'z, find the minimal expression of the function F(x,y,z) = x+x'y'z+yz?	C	1	y' + z	xz + y'	x + z	x' + y
221	3	Simplify XY' + X' + Y'X'.	C	1	X' + Y	XY'	(XY)'	Y' + X
222	3	Minimize the following Boolean expression using Boolean identities.F(A,B,C) = (A+BC')(AB'+C)	D	1	A + B + C'	AC' + B	B + AC	A(B' + C)
223	3	Minimization of function F(A,B,C) = AB(B+C) is _____	D	1	AC	B+C	B`	AB
224	3	Algebra of logic is termed as _____	B	1	Numerical logic	Boolean algebra	Arithmetic logic	Boolean number
225	3	Boolean algebra can be used _____	A	1	For designing of the digital computers	In building logic symbols	Circuit theory	Building algebraic functions
226	3	A _____ value is represented by a Boolean expression.	D	1	Positive	Recursive	Negative	Boolean
227	3	A + AB + ABC + ABCD + ABCDE + …. = _____	B	1	1	A	A+AB	AB
228	3	The minimum number of literal obtained on simplifying the expression ABC + A'C + AB'C + A'BC are _____.	C	1	A'C+BC	A(A+B')	C	A'B+AC'
229	3	Reduce the expression: A+B (AC+(B+C')D)		2				
230	3	Reduce the expression: (A+(BC)')'(AB'+ABC)		3				
231	3	Minimize the Boolean expressions: X = ((A'B'C')' + (A'B)')'.		2				
232	3	Find the complement of the following boolean function and reduce to a minimum numbers of literals: B'D + A'BC' +ACD + A'BC		3				
233	3	Draw the logic diagram of the following function. Use one OR gate and one AND gate only. Y = (A+B)(A+C)		3				
234	3	Given boolean function F = XY + X'Y'+Y'Z. Implement it with only OR and NOT gates.		4				
235	3	Prove that a dual of Ex-OR is also its complement.		4				
236	3	The logic expression (A'+B) (A+B') can be implemented by giving the inputs A and B to a two input _____	D	1	NOR Gate	NAND Gate	XOR Gate	XNOR Gate
237	3	Which of the given boolean expression is incorrect?	B	1	A + A'B = A + B	A + AB = B	(A+B)(A+C)=A+BC	(A+B')(A+B)=A
238	3	The simplified form of boolean expression (X+Y+XY)(X+Z) is	C	1	X+Y+Z	XY+YZ	X+YZ	XZ+Y
239	3	AB + A'C + BC = AB + A'C represents which theorem?	A	1	Consensus	Transposition	De Morgan's	None
240	3	The simplified form of boolean expression (A'BC+D)(A'D+B'C') can be written as	A	1	A'D+B'C'D	AD+BC'D	(A'+D)(B'C+D')	AD'+BCD'
241	3	Determine the output X of a logic circuit shown in figure. Simplify the output expression using boolean laws and theorems. Redraw the logic circuit with the simplified expression. 	Simplified Expression is: AB'	3				
242	3	Consider the following boolean expressions: I: x.y + x'y' II: XOR (x', y') III: XOR (x', y) Which of the above expressions represents exclusive NOR operation?	C	1	I and II	I, II and III	I and III	II and III
243	3	Consider the boolean function: f = (a+bc)(pq+r). Complement (f)' of a function f is -	B	1	(a'+b'c')(pq'+r')	a'(b'+c')+(p'+q')r'	(a'+b'c')+(p'q'+r')	a'b'c'+p'q'r'

244	3	Derive the logic expression for the given logic diagram 	A	1	C(A + B)DE	[C(A + B)D + E']	[[C(A + B)D]E']	ABCDE
245	3	Most Boolean reductions result in an equation in only one form.	A	1	TRUE	FALSE		
246	3	According to property of Commutative law, the order of combining terms does not affect _____	B	1	initial result of combination	final result of combination	mid-term result of combination	None
247	3	According to boolean algebra which of the following relation is not valid?	D	1	X(YZ) = (XY)Z	X(Y+Z) = XY + XZ	X+XZ = X	X(X+Y)=1
248	3	Simplify the following expression: F = AB'C + AB'C'+ABC	A	1	F = AC + AB'	F = A'C + AB	F = AC' + AB	F = AC' + AB'
249	3	Which of the following options correctly represents the consensus law of Digital Circuits?	A	1	AB + A'C + BC = AB + A'C	A'B + A'C + BC = AB + A'C	AB + A'C + BC = AB + (AC)'	A'B + A'C + BC = AB + (AC)'
250	3	Verify the equation by using boolean algebra: AB + AC + BC' = AC + BC'		4				
251	3	Find out the minimized form of a logical expression (A'B'C' + A'BC' + A'BC + ABC').		3				
252	3	The boolean expression (X+Y)(X+Y')+(X'Y'+X')' simplifies to	A	1	X	Y	XY	X+Y
253	3	Simplify the following boolean expression to four literals: F = A'C + C'D + B'C + AB	AB+C+D	3				
254	3	The reduced form of complement of equation f = [(ab)'a][(ab)'b]	B	1	0	1	a'b+ab'	a'b'
255	3	The reduced form of dual of equation f = [(ab)'a][(ab)'b]	B	1	0	1	a'b+ab'	a'b'
256	3	Which of the given boolean expression is incorrect?	D	1	(A'+B')' = AB	(A+ (B')')' = A' B'	(A'B')' = A+B	(A'B'')' = A'+B
257	3	The boolean equation x = [(A+B')(B+C)]B can be simplified to -	C	1	X = A'B	X = AB'	X = AB	X = A'B'
258	3	Find the output boolean function for the given logic circuit. 	A	1	X = A'BC	X = AB'C	X = ABC	X = A'B'C
259	3	The output Y of the logic circuit is - 	A	1	1	0	X	X'
260	3	Simplify the following boolean expression and realize it using NOR gates only: $Y = A\bar{B} + AB\bar{C} + ABCD + ABC\bar{D}$		3				
261	3	Simplify the following boolean expression and realize it using NAND gates only: $ABC[AB + \bar{C}(BC + AC)]$		3				
262	3	Match the appropriate pairs: (1) x+(y+z)=(x+y)+z (A) Commutative Law (2) x+y=y+x (B) Absorption Law (3) x+xy=x (C) Complementation law (4) (x')'=x (D) Associative Law	C	1	1-B, 2-A, 3-D, 4-C	1-D, 2-A, 3-C, 4-B	1-D, 2-A, 3-B, 4-C	1-C, 2-A, 3-D, 4-B
263	3	Simplify: $f = AB + ABC + \bar{A}B + A\bar{B}C$	B+AC	2				
264	3	Minimize the following function using boolean algebra: $f = \bar{A}BCD + AB\bar{C}\bar{D} + AB\bar{C}D + ABCD + ABC\bar{D} + A\bar{B}\bar{C}D + A\bar{B}CD + A\bar{B}C\bar{D}$		2				
265	3	Simplify: $f = (A + \bar{B}C) + \overline{(A + \bar{B}C)} = 1$		3				
266	3	Simplify the following boolean expression which represents the output of a logical decision circuit $f(w, x, y, z) = x + xyz + \bar{x}yz + wx + \bar{w}x + \bar{x}y$	x+y	2				
267	3	Simplify the following boolean expression which represents the output of a logical decision circuit $f(A, B, C, D, E) = (AB + C + D)(\bar{C} + D)(\bar{C} + D + E)$	ABC'+D	3				
268	3	Prove the following identity: $\overline{\overline{AB} + \bar{A} + AB} = 0$		2				
269	3	Simplify the following function by using boolean algebra: Y = AB'C'D + A'B'D + BCD' + A'B + BC'		3				
270	3	Simplify the following function by using boolean algebra: Y = (AB + A'C + BC)(A+B'+AB')	AB+A'B'C	2				
271	3	Construct a logic circuit to give an output without any reduction in number of gates. Give the logic gates output step by step. $X = (\overline{AB} + \bar{A}C)(\overline{AD + C})$		3				
272	3	Find out the complement of boolean expression : AB (B'C+AC)		2				
273	3	The boolean function Y = AB + CD is to be realized using only 2-input NAND gates. The minimum number of NAND gates required is -	B	2	2	3	4	5

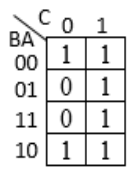
274	3	Realize the given logic circuit into appropriate boolean expression and also minimize it. 		3				
275	3	Make a suitable logic expression from the given truth table and also minimize it up to a single literal remaining. 		2				
276	3	_____ NAND gates required to implement the function : $F = (\bar{X} + \bar{Y})(Z + W)$		3				
277	3	The boolean expression for the given circuit is _____ 	A	1	A {F + (B + C) (D + E)}	A [F + (B + C) (DE)]	A + F + [(B + C) (D + E)]	A [F + (BC) (DE)]
278	3	DeMorgan's first theorem shows the equivalence of _____	B	1	OR gate and Exclusive OR gate	NOR gate and Bubbled AND gate	NOR gate and NAND gate	NAND gate and NOT gate
279	3	((AB)'+(AC)')' = _____	B	1	A+B+C	ABC	A'BC	(A+B+C)'
280	3	Consider four distinct input boolean variables, in which first two and last two variables are ANDed. Then after output of both operation is Ored together. Implement the circuit based on the given information and also find its boolean expression.		2				
281	3	What is the boolean expression for Y in above circuit ? 		2				
282	3	Find out the simplified boolean equation for the given logic circuit. 	A	1	(A + B) (C + D) (E + F)	A+B+C+D+E+F	ABCDEF	ABC + DEF
283	3	Four inputs A, B, C, D are fed to a NOR gate. The output of NOR gate is fed to the two successive inverter. The final output is given by - _____	B	1	A+B+C+D	(A+B+C+D)'	ABCD	(ABCD)'
284	3	For the logic circuit of the given figure, the minimized expression is - 	A	3	Y = (AB'C)'	Y = A+B+C	Y = A + B	Y = ABC
285	3	Choose the correct statement for 'literal' - (I) Literal is a primed variable only. (II) The minimization of the number of literals and the number of terms results in a circuit with less equipment (III) We can not reduce the number of literals in any given Boolean function. (IV) In the Boolean equation y=a' b+b' c+c'd, the terms a'b , b'c and c'd are known as literals.	B	1	Only I and III	Only II	Only II and IV	All are correct
286	3	Simplify the boolean expression to a minimum number of literals: y(wz'+wz)+xy		2				
287	3	Reduce the following boolean function upto minimum five literals (including primed and unprimed variables): $ABC + A'B'C + A'BC + ABC' + A'B'C'$		2				
288	3	Reduce the following boolean function upto minimum four literals (including primed and unprimed variables): $X = \bar{B}D + \bar{A}B\bar{C} + ACD + \bar{A}BC$		2				

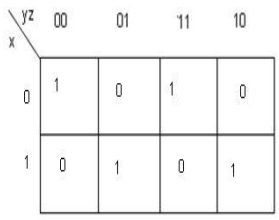
289	3	Find the complement of F = x +yz, then show that F·F' = 0 and F+F' = 1		2				
290	3	Find the complement of the following Boolean functions and reduce them to a minimum number of literals: $(A' + C)(A' + C')(A + B + C'D)'$		3				
291	3	Write the Boolean expression for output X for the logic circuit shown in figure. Also show the ouput of each stage of logic gates: 		3				
292	3	Write the Boolean expression for output X for the logic circuit shown in figure. Also show the ouput of each stage of logic gates: 		3				
293	3	Construct a logic circuit using INVERTER, AND and OR gates for the Boolean expression $X = \overline{(A+B+\bar{C}D\bar{E})} + \bar{B}C\bar{D}$		3				
294	3	A network of cascaded inverters shown in fig. If a logic 1 is applied to A, Determine the logic levels from point B through F. 		2				
295	3	Using boolean laws and rules, simplify the expression: Z = A'BC + AB'C' + A'B'C' + AB'C + ABC		3				
296	3	Using boolean laws and rules, simplify the expression: Z = (AB+AC)' + A'B'C and prove that Z = A' + B'C'		3				
297	3	Demorganize the expression: $\overline{(A+B)\bar{C}\,\bar{D} + (E+\bar{F})}$		2				
298	3	Simplify the boolean expression: T[x,y,z] = (x+y) (x'(y'+z'))'+x'y'+x'z'.		3				
299	3	The circuit shown in Fig. is used to implement the function Z = f (A, B) = A + B. What values should be selected for I and J ? 		3				
300	3	Determine the logic function realized by the circuit shown in Fig. Also minimize the output function f using laws boolean algebra. 		3				
301	3	Determine by means of truth table, the validity of De Morgan's theorem for three variables: (ABC)' = A' + B' + C'		3				
302	3	A switch board contains four electrical switches which are connected in a sequence in a room: 1st switch as main power supply switch of the room, 2nd switch belongs to a fan, 3rd switch belongs to a TV and 4th switch belongs to 0 W bulb. The main power supply switch is also directly connected to the 0W bulb. Design the boolean expression of the switch board of the room such that user can operate switch board as per his requirement. Also show how the boolean expression can be minimized.		3				
303	3	Boolean arithmetic is a :	A	1	way to express logic statements in a traditional mathematical equation format	terrible fraud perpetrated by philosophers to disprove things they don't agree with	very difficult calculation used in astronomy	fast way to solve problems around the house
304	3	Determine and minimize the Boolean expression for the output, X of a logic circuit shown in figure. Also give your comment on the minimized output. Which logic gate is represented by simplified output? 	AND gate	3				

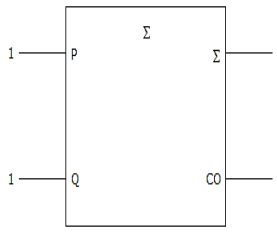
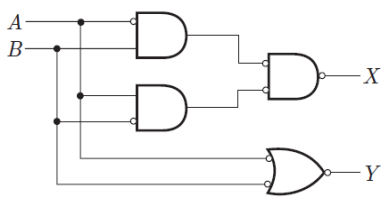
305	3	Simplify the following boolean expression using laws of Boolean algebra. f(w,x,y,z)=x+x'yz+x'yz+wx+w'x+x'y Y=AB'+ABC'+ABCD+ABCD'		3				
306	3	As per _____ theorem, PQ+P'R+QR = _____	C	1	Transposition, PQ+QR	Absorption, PQ+P'R	Consensus, PQ+P'R	Consensus, PQ+PR'
307	3	Which of the following statements are true? 1. An XOR gate produces an output 1 only when the inputs are not equal. 2. An XNOR gate produces an output 1 only when the inputs are equal. 3. An XOR is also called anti-coincidence gate. 4. An XNOR is also called coincidence gate.	D	1	Both 1 and 2	Both 3 and 4	Both 2 and 3	All are true
308	3	Evaluate which one is correct? (1) $(A'+B') \oplus B' = AB'$ (2) $(AB)' \odot (A+B) = 1$ (3) $A' \oplus A \odot 1 = A'+A$	C	1	Only 1	Only 2	Only 3	Only 4
309	3	If a 3-input NAND gate has eight input possibilities, how many of those possibilities will result in a LOW output?	A	1	1	7	5	6
310	3	The given logic diagram describes the process of an industrial operation that depends on distinct values of A, B and C. Find the boolean expressions of each level (Level 1 to level 7) also define following logic diagram belongs to which equivalent logic gate? 		4				
311	3	Consider the following boolean expressions and Check whether the given statement/s is/are Correct or not. I: MN' + M' + M'N' = (MN)' II: Q' (P' + Q') (P + P'Q) = PQ' III: AB (A + B') + A (B + B') = A IV: A' + A'B + A'BC + A'BCD + A'BCDE + …. = A'B	C	1	Only II and IV are correct	Only III is correct	Only I, II and III are correct	All are correct
312	3	The circuit shown in Fig. is used to implement the function Z = f (A, B) = (AB)'. What values should be selected for I and J ? 	Both A & B	1	I= A' AND J= B'	I= 1 AND J=B'	I=A AND J= B	I= B' AND J= A'
313	3	Given W = [(A XOR B) XNOR 1], X= [(A XOR B') XOR 0], Y= [(A XNOR B) XOR 1] and Z= [(A' XOR B) XNOR 0]. Find Output Function = W OR X OR Y OR Z as per data and simplify it using basic theorems and construct simplified function with basic logic gates.		2				
314	3	Determine the output F of a logic circuit shown in figure with truth table and logical expression. Simplify the output expression using boolean laws and theorems. Redraw the logic circuit of simplified expression with two gates only. 		3				
315	3	If a signal passing through a gate is inhibited by sending a LOW into one of the inputs, and the output is HIGH, the gate is a(n):	b	1	a) AND	b) NAND	c) OR	d) NOR
316	3	Choose correct statement/s from following i) an inverter performs complementation operation ii) process performed by inverter is known as inversion iii) an inverter contains two or more input terminal and one output terminal.	a	1	a) Only I & II	b) Only I & III	c) Only II & III	d)All of the above
317	3	if the boolean expression P'Q + QR + PR is minimized , the expression becomes	b	1	a) P'Q + QR	b) P'Q + PR	c) QR + PR	d) P'Q+ QR + PR
318	3	A + AB = A ; A(A+B) = A represents which law ?	b	1	a) commutative	b) Absorption	c) Consensus	d) Transposition
319	3	Exclusive-OR (XOR) logic gates can be constructed from ……..logic gates	d	1	a)AND, OR, NOT	b)OR Gate & NOT gate	c)NOR & NOT Gate	d) a & c both
320	3	The circuit shown below generates the function of F= _____ 	a	1	a) x⊕y	b) 0	c) xȳ + yx + ȳx	d) x + y

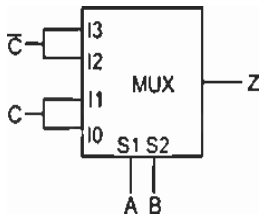
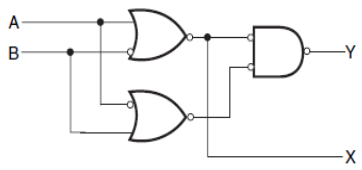
321	3	Transmitter transmit 8 bit of information in form of data packet D0 (LSB) to D7 (MSB) where D0 Defines EVEN PARITY BIT, D1 as start bit '1' , D2 to D5 as data bits (E)16 number & D6 & D7 as stop bit '10' respectively in transreceiver digital communication system. evalue the D0 = _____	a	1	a) 1	b) 11	c) 10	d) 0
322	3	In the figure shown, the output Y is required to be Y = A.B + C'.D' .The gates G1 and G2 must be respectively 	d	1	a) AND & OR	b) OR & NAND	c) NAND & OR	d) NOR & OR
323	3	Draw the logic diagram of boolean expression (A+B)(CD)'(E+F)' G' & its complement seperately using only two input basic logic gates (do not use NAND , NOR , X-OR , X-NOR logic gates)		3				
324	3	Which of the following is true? 1. (A+B). (AB)' = A XOR B 2. AB+(A+B)' = A XNOR B 3. A XOR B' = A XNOR B	d	1	Both 1 and 2	Both 1 and 3	Both 2 and 3	All are true
325	3	Simplify the Boolean expression. AB+(AC)'+AB'C(AB+C)		2				
326	3	The given logic diagram depends on values of A & B. Find the Boolean expressions of each level till output Y and also define following logic diagram belongs to which equivalent gate? 		4				
327	3	Match the following 1) A+A' P. 0 2) A⊕ A Q. 1 3) 0 ⊕ A R. A 4) A'A' S. A'	b	1	a) 1-P, 2-Q, 3-R, 4-S	b) 1-Q, 2-P, 3-R, 4-S	c) 1-S, 2-R, 3-P, 4-Q	d) 1-Q, 2-P, 3-S, 4-R
328	3	MN(M + N') + M(N + N') = _____	a	1	a) M	b) N	c) M'	d) N'
329	3	Find out the Boolean Expression for Logic Diagram given below and simplify the output in the minimal expression, also implement the simplified expression using the AOI logic. 		4				
330	3	Match the following with correct logic expression: Column A Column B 1. A' Θ A ⊕ A' w. 1 2. A' ⊕ 0 ⊕ A x. A' 3. A ⊕ A' Θ A y. 0 4. A' Θ 1 Θ A z. A	b	1	1-x, 2-z, 3-w, 4-y	1-x, 2-w, 3-z, 4-y	1-w, 2-z, 3-x, 4-y	1-y, 2-w, 3-z, 4-x
331	4	The Sum of all Minterm is _____	B	1	0	1	2	4
332	4	The Product of all Maxterm is _____	A	1	0	1	2	4
333	4	The minterm related to F(w,x,y,z)= m6 is	A	1	w'xyz'	wxyz	wx'y'z	wx'yz
334	4	The Maxterm related to F(w,x,y,z)= M7 is	A	1	w+x'+y'+z'	w'+x+y+z	w+x+y+z	w'+x+y'+z
335	4	Convert SOP into POS : F(A,B,C)= ∑m(1,3,7)	D	1	π M(0,2,4,6)	π M(2,4,5,6)	π M(0,2,4)	π M(0,2,4,5,6)
336	4	Convert POS into SOP: F(w,x,y,z) = πM(0,1,2,6,10,12,14,15)	C	1	∑m(3,4,5,7,8,9,11,13,16)	∑m(0,3,4,5,7,8,9,11,13)	∑m(3,4,5,7,8,9,11,13)	∑m(3,4,5,8,9,11,13)
337	4	Express the boolean function F= A + B'C in sum of minterm		2				
338	4	Express the Boolean function F = AB + A'C in a product of maxterm.		2				
339	4	Convert into Product-of-Maxterms: A(A'+B)(C')		2				
340	4	Convert into Sum-of-Minterms: A' + B + CA		2				
341	4	Express Function in Product of Maxterms F(x,y,z) = (xy + z) (y + xz)		2				
342	4	Express the Boolean function in sum of minterms F (A,B,C)=(A'+B)(B'+C)		2				
343	4	Express the Boolean function in sum of minterms F (A,B,C,D)= D(A'+B)+B'D		2				
344	4	Express the Boolean function in sum of minterms and product of max terms. F (A,B,C,D)= (A+B'+C)(A+B')(A+C'+D')(A'+B+C+D')(B+C'+D')		3				
345	4	Express the Boolean function in sum of minterms and product of max terms. F (X,Y,Z) = (XY+Z)(Y+XZ)		3				
346	4	Express the Boolean function in sum of minterms and product of max terms. F (X,Y,Z) = 1		3				
347	4	Express the Boolean function in sum of minterms and product of max terms. F (W,X,Y,Z) = Y'Z+WXY'+WXZ'+ W'X'Z		3				
348	4	Expand A'+ B' to minterm and maxterm		2				
349	4	Expand A+BC'+ABD'+ABCD to minterm and maxterm		2				
350	4	Convert the following Boolean function in product of maxterms and sum of minterms: F(m,n,o,p) = n'o'p+nop+mop'+m'n'o+m'no'p		3				

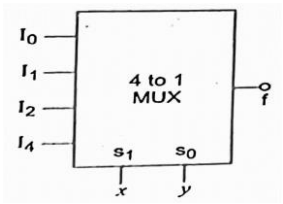
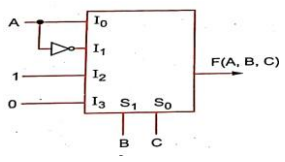
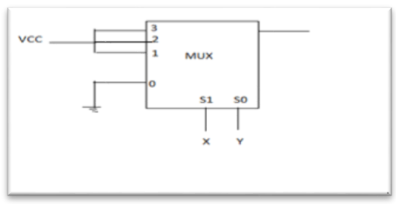
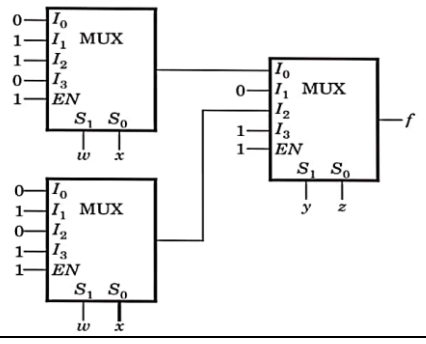
351	4	Expand A(A'+B)(A'+B+C') to minterm and maxterm		2				
352	4	Convert the following to other canonical form F(x,y,z) = ∑(1,3,7)		2				
353	4	Convert the following to other canonical form F(A,B,C,D) = ∑(0,2,6,11,13,14)		2				
354	4	Convert the following to other canonical form F(X,Y,Z) = π (0,3,6,7)		2				
355	4	Convert the following to other canonical form F(A,B,C,D) = π (0,1,2,3,4,6,12)		2				
356	4	A Karnaugh map is an abstract form of _____ diagram organized as a matrix of squares	A	1	Venn	Cycle	Point	Block
357	4	Which of the following code is employed by K-Map for simplification of Boolean Expression?	B	1	XS-3	Gray	BCD	Parity
358	4	The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms	C	1	3	6	8	2
359	4	Which of the following is NOT considered for forming groups in K-map?	A	1	Diagonal	Rolling	Vertical	Horizontal
360	4	There are 3 Variable in the boolean function and the value of the function is 1. Find the number of cells in the K-Map which will contain a 1 when SOP expression is used	B	1	3	8	1	0
361	4	There are 3 Variable in the boolean function and the value of the function is 1. Find the number of cells in the K-Map which will contain a 0 when SOP expression is used _____	D	1	3	8	1	0
362	4	Given F(A, B, C, D) = ∑ m(0, 1, 2, 6, 8, 9, 10, 11) + ∑ d(3, 7, 14, 15) is a Boolean function, where m represents min-terms and d represents don't cares. The minimized logical fuction F is _____	B	1	Independent of variables	Depedent on 2 variable	Depedent on 3 variable	Depedent on 4 variable
363	4	In simplification of a Boolean function of n variables, a group of 2^m adjacent 1s leads to a term with	D	1	m – 1 literals less than the total number of variables	m + 1 literals less than the total number of variables	n + m literals	n – m literals
364	4	Looping on a K-map always results in the elimination of _____	C	1	Variables within the loop that appear only in their complemented form	Variables that remain unchanged within the loop	Variables within the loop that appear in both complemented and uncomplemented form	Variables within the loop that appear only in their uncomplemented form
365	4	Digital input signals A, B, C with A as the MSB and C as the LSB are used to realize the Boolean function F = m0 + m2 + m3 + m5 + m7, where mi denotes the ith minterm. In addition, F has a don't care for m1 + m4 + m6. The simplified expression for F is given by:	A	1	1	(A + C) (A' +C')	A'C' + AC	A'C + AC'
366	4	Simplify the Boolean function using K-Map: F(w,x,y,z) = Σ (0,1,2,4,5,6,8,9,12,13,14)		3				
367	4	Simplify the Boolean function using K-Map: F(w,x,y) = Σ (0,1,3,4,5,7)		2				
368	4	Obtain the simplified expression using K-Map in sum of product for the Boolean functions F= Σ(0,1,4,5,10,11,12,14).		3				
369	4	Simplify the Boolean function F(x,y,z)= ∑m(0,1,2,3,4,5,6) using K- map. Explain groups		3				
370	4	Simplify the following Boolean function using K-map F(w,x,y,z) = Σ(1, 3, 7 , 11 , 15)		3				
371	4	Simplify the following Boolean function using K-Map. F=A′B′C′+B′CD′+A′BCD′+AB′C.		4				
372	4	Obtain the simplified expressions in sum of products using K-map: x'z + w'xy' + w(x'y + xy')		4				
373	4	Simplify following boolean function using K-Map: Y = Σm(1, 5, 7, 9, 11, 13, 15)		3				
374	4	Simplify following boolean function using K-Map: Y = Σm(0, 2, 3, 5)		2				
375	4	Simplify following boolean function using K-Map: Y = Σm(1, 3, 5, 9, 11,13)		3				
376	4	Simplify following boolean function using K-Map: Y = Σm(0, 2, 5, 6, 7, 8, 10, 13, 15)		3				
377	4	Simplify following boolean function using K-Map: Y = Σm(1, 5, 6, 7, 11, 12, 13, 15)		3				
378	4	Simplify following boolean function using K-Map: Y = Σm(1, 3, 4, 5, 7, 9, 11, 13, 15)		3				
379	4	Simplify Boolean function using K-Map: F(w,x,y,z) = ∑(1,3,5,8,9,11,15)		3				
380	4	Simplify the Boolean Function with Karnaugh map: F(w,x,y,z) = Σ(0,1,2,4,5,6,8,9,12,13,14,15)		3				
381	4	Simplify the Boolean Function with Karnaugh map: F = A'B'C'+B'CD'+A'BCD'+AB'C'		4				
382	4	Simplify the Boolean function F(x,y,z)= Σ (0,2,4,5,6) using K- map.Explain groups.		2				
383	4	Simplify following boolean function using K-Map: Y = AB'C'D' + AB'C'D + AB'CD + AB'CD'		4				
384	4	Simplify using K-map F= AB'C + AB'C'D + ABC'D + ABC		4				
385	4	Simplify using K-map F= A'B'C + A'BC + ABC + ABC'		3				
386	4	Minimize following Boolean function using K-map: X(A,B,C,D) = Σ m(0, 1, 2, 3, 5, 7, 8, 9, 11, 15)		3				
387	4	Simplify the Boolean function, F=Σm(0,1,2,5,8,9,10)		3				
388	4	Minimize following Boolean function using K-map F = Σ m(1, 2, 4, 6, 7, 11, 15) + Σ d(0, 3)		4				
389	4	Minimize the following function using K-Map F = Σm(0,2,6,10,11,12,13) + d(3,4,5,14,15)		4				
390	4	Simply the Boolean Function using K-map : F(W,X,Y,Z) = ∑(1, 3, 7, 11, 15) with don't care conditions d(W,X,Y,Z) = ∑(0, 2, 5)		4				
391	4	Reduce the given function using K-map F(A,B,C,D) = Σm (0,1,3,7,11,15) + Σd (2,4)		4				
392	4	Minimize the following logic function using K-maps F(A,B,C,D) =∑m(1,3,5,8,9,11,15) + d(2,13)		4				
393	4	Minimize the following function using K-map F (w,x,y,z) = Σm (0,1,2,3,6,7,13,14) + Σd (8,9,10,12)		4				
394	4	Minimize the following functions using K Map F =ΠM(0,4,9,10,11,14,15)		3				
395	4	Minimize the logic function F (A,B,C,D) = π M (1, 2, 3, 8, 9, 10, 11, 14) . d (7, 15) Use Karnaugh map. Draw the logic circuit for simplified function using NOR gates only.		4				
396	4	Simplify Boolean function F (w,x,y,z) = Σ (0,1,2,4,5,6,8,9,12,13,14) using K-map and Implement it using NAND gates only		4				
397	4	Solve the following Boolean functions by using K-Map. Implement the simplified function by using logic gates F =(w,x,y,z) =∑(0,1,4,5,6,8,9,10,12,13,14)		4				

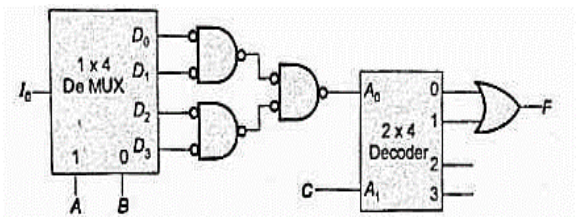
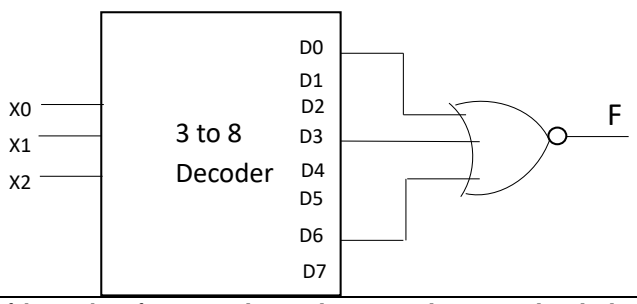
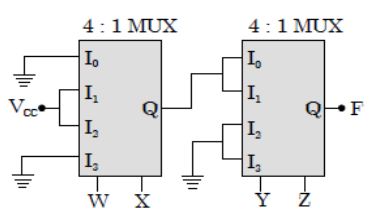
398	4	Reduce the expression F = ∑m(0,2,3,4,5,6) using K-map and implement using NAND gates only.		4				
399	4	Implement the function F=∑(0,6) with NAND gates only.		3				
400	4	Implement the function F=∑(0,6) with NOR gates only		3				
401	4	Obtain the simplified expressions in SOP for the following Boolean function using K-Map method. And implement it using NAND gate. F(A,B,C,D) = ABC+AB'C+BCD'+A'CD		4				
402	4	Reduce using mapping the expression ∑m(0, 1, 2, 3, 5, 7, 8, 9, 10, 12. 13) and implement it with any universal logic.		4				
403	4	Reduce using mapping the expression πM(2, 8, 9, 10, 1, 12, 14) and implement it with any universal logic		4				
404	4	Reduce using mapping the expression ∑m(1, 5, 6, 12,13, 14)+ d(2,4) and implement it in universal logic.		4				
405	4	Reduce using mapping the expression ∑m(0,1, 3, 5, 6, 12,13, 14)+ d(2,7,8,15) and implement it in universal logic.		4				
406	4	Reduce using mapping the expression ∑m(0, 1, 4, 7, 13, 14) + d(5, 8, 15) and implement it in universal logic.		4				
407	4	Reduce using mapping the expression πM(0,1 ,3 4, 5, 7, 10, 13, 14, 15)and implement it in universal logic.		4				
408	4	Reduce using mapping the expression πM(2, 4, 6, 8, 10, 12, 15) and implement it in universal logic.		4				
409	4	Reduce using mapping the expression πM(0, 1, 4, 6, 8, 9, 11) and d(2, 7, 13) and implement it in universal logic.		4				
410	4	Reduce using mapping the expression πM(2, ,4 ,5 7, 9, 12) and d(0, 1, 6) and implement it in universal logic.		4				
411	4	The inputs to a computer circuit are the 4 bits of the binary number A3A2A1A0 The circuit is required to produce a 1 if any of the following conditions hold. 1. The MSB is 1 and all other bits are 0. 2. A2 is a 1 and the all other bits are 0. 3. All of the 4 bits are 0. 4. A1 and A0 is 1 and other bits are 0 Obtain a minimal expression using K-map and implement it with NAND gate		5				
412	4	A8A4A2A1 is an Binary input to a logic circuit whose output is a 1 when A8=0, A4=0 and A2=1,or when A8=0 and A4=1.Design the simplest possible logic circuit with NAND gate only using K-map in SOP form.		5				
413	4	The _____ is a very useful and convenient tool for simplification of Boolean functions for large numbers of variables.	A	1	Quine McCluskey tabulation method	K-map	SOP K-map	POS k-map
414	4	The implicants which will definitely occur in the final expression are called	C	1	Prime implicant	Non-prime implicant	Essential Prime implicant	implicant
415	4	_____ is a group of minterms which can't be combined with any other groups.	C	1	Odd implicant	Even implicant	Prime implicant	Non-prime implicant
416	4	In the Quine-McClusky method of minimization of the function f(A, B, C, D) the PI corresponding to -1 1- is	A	1	BC	AD	B'C'	A'D'
417	4	In the Quine-McClusky method of minimization of the function f(A, B, C, D) the PI corresponding to -1 -0 is	A	1	BD'	B'D	AC	A'C'
418	4	Unchecked terms in the PI table forms are called_____	A	1	Prime implicant	Non-prime implicant	Essential Prime implicant	implicant
419	4	Simplify following Boolean function by using the tabulation method F=∑(0,1,3,7,8,9,11,15)		5				
420	4	Simplify the following Boolean expression by means of the Tabulation method. F(A,B,C,D) = ∑m (1,2,3,5,6,7,8,9,12,13,15).		5				
421	4	Simplify the following boolean function using tabulation method and draw logic diagram using AND-OR-NOT gates. F(w, x, y, z) = Σ(0, 1, 2, 8, 10, 11, 14, 15)		5				
422	4	Obtain the set of prime implicants for Σ m (0, 1, 6, 7, 8, 9, 13, 14, 15)		5				
423	4	Obtain the set of prime implicants for Σ m (0,1 ,3, 4, 5, 7, 10, 11, 13, 14, 15)		5				
424	4	Obtain the set of prime implicants for Σ m (0,1, 2 ,3 6, 7, 8, 10, 11, 12, 15)		5				
425	4	Obtain the set of prime implicants for Σ m(5, 6, 12, 13, 14)		4				
426	4	Simplify Boolean function by using the tabulation method F = ∑m(1,2 ,5 6, 8, 9, 10,11,12,15)		5				
427	4	Simplify Boolean function by using the tabulation method F = ∑m(0, 1, 2,4, 6,7, 8, 9, 11,13)		5				
428	4	Simplify Boolean function by using the tabulation method F = ∑m(0,1,2,4,5,6, 7,9,12)		5				
429	4	Find Essential Prime Implicants of F = ∑m(1,2,3,5,7,10,11,14,15)		5				
430	4	Design Prime Implicant chart and calculate essential Prime Implicants for the function F = ∑m(0,1,4,5,7,8,13,14,15)		5				
431	4	Calculate number of essential prime implicants for F = ∑m(3,4,5,9,10,11,14)		4				
432	4	Simplify the following Boolean function F(W,X,Y,Z)=∑m(2,6,8,9,10,11,14,15) using Quine-McClukey tabular method.		5				
433	4	Using the tabular method of simplification, find all equally minimal solutions for the function F(A,B,C,D) = (1,4,5,10,12,14)		5				
434	4	Consider the function f(A, B, C, D) = (0,1,2,3,5,7,8,10,12,13,15) and its prime implicants are A'B' from pair (0,1,2,3) , B'D' from (0,2,8,10) , A'D from (1,3,5,7) , BD from (5,7,13,15) , AC'D' from (8,12) and ABC' from (12,13). Design Prime implicant chart and find out essential prime implicants.		3				
435	4	Calculate essential prime implicants using Prime implicant chart and also obtain simplified logical expression for F= (3,4,5,6,7,10,11,12,13,15)		4				
436	4	Simplify the following boolean function F(w, x, y, z) = ∑m(6, 7, 8, 9, 10, 11, 12, 13, 14, 15) using Quine-McCluskey method.		4				
437	4	Which Boolean function the following Karnaugh map represent?  	B	1	A + C	A' + C	A + C'	A + CA'
438	4	$\bar{A}B + CD$ is the simplified version of the Boolean expression F only if there were a 'don't care' entry. What is that don't care term ? $F = ABCD + \bar{A}\bar{B}CD + \bar{A}B$	A	1	AB'CD	AB'C'D	A'BCD	A'BC'D
439	4	There are 4 variables P, Q, R and S in Boolean function and the value of the function is 0. Find the number of cells in the K-map which will contain 0 when POS expression is used.	D	1	15	1	0	16

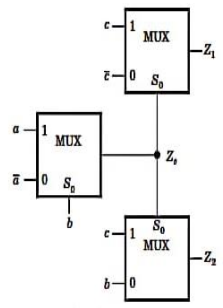
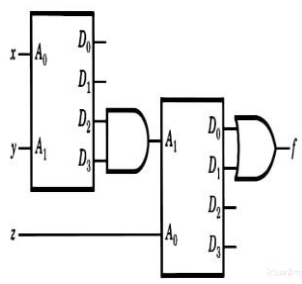
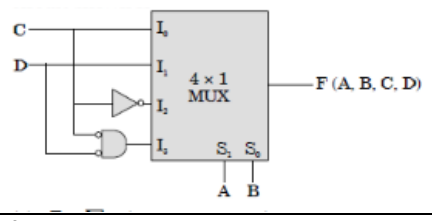
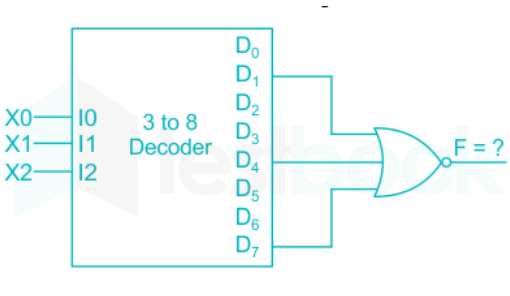
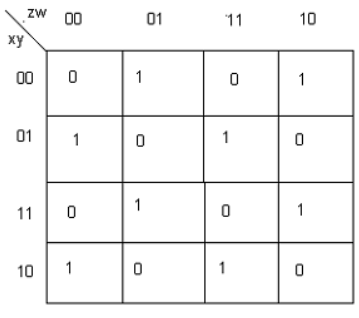
440	4	Convert the following Boolean function in product of max terms and sum of minterms: F(p,q,r,s) = (p' + q + r) (q' + r + s) (p + s')		2				
441	4	Obtain the simplified Boolean expression for the following Boolean function with don't care condition and implement the simplified function with NOR gates only. F (w, x, y, z) = w'y'x'z' + w'x'yz' + x'yz'w + yzwx' + wy'z'x + wzxy' + ywxz' + wxyz d (w, x, y, z) = w'x'yz + zw'xy + y'z'wx' + y'zwx'		5				
442	4	Obtain the simplified boolean expression for the following boolean function with don't care condition and implement the simplified function with two input NAND gates only. F(w,x,y,z) = w′ x z + w′ y z + x′ z′ y + w y′ x z d = w y z		5				
443	4	Simplify Boolean function F (W, X, Y, Z) = Σ (0, 1, 2, 4, 5, 6, 8, 9, 10, 12,13) using K-map and implement it using NAND gates only.		3				
444	4	Simplify Boolean function using the tabulation method F (A, B, C, D) = ∑m (0, 1, 2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15)		5				
445	4	Express the Boolean function F (X, Y) = 1 in canonical form.	A	1	x'y' + x'y + xy' + xy	xy	x + y	X'Y' + XY + XY' + XY
446	4	Given F(A, B, C, D) = ∑ m(2, 6, 8, 9, 10, 11) + ∑ d(3, 7, 14, 15) is a Boolean function, where m represents min-terms and d represents don't cares. The minimized logical function F is		1				
447	4	Express the Boolean function in sum of minterms and product of max terms. F (W,X,Y,Z) = YZ+WXY+WXZ+ WXZ		3				
448	4	Minimize the logic function F(A,B,C,D) = πM(1, 2, 3, 8, 9, 10, 11, 14).d (7, 15) Use Karnaugh map. Draw the logic circuit for simplified function using NOR gates only.		4				
449	4	Simplify Boolean function by using the tabulation method F(A,B,C,D)=∑m(2,3,6,7,8,9,10,11,12,13,14,15)		5				
450	4	F=∑ m (1,3,4,5,7,9,13) is a simplified version of the Boolean expression D+A'.B only if there were a 'don't care' entry. What is that don't care term?	a	1	6,11,15	6,11,14	6,10,15	7,9,15
451	4	Which Boolean function does the following k-map represent? 	a	1	XNOR	AND	OR	NAND
452	4	Implement the following functions using the don't-care conditions. F = A′B′C′ + AB′D + A′B′CD′ d = ABC + AB′D′ Also implement the simplified expression using NAND gates only.		4				
453	4	Implement the following functions using the don't-care conditions. F = A′B′C′ + AB′D + A′CD′ d = ABC + AB′D′ Also implement the simplified expression using NOR gates only.		3				
454	4	Given the Boolean function F in three variables R, S and T as F=R'ST'+RS'T+RST (a) Express F in the minimum product-of-sums form. (b) Assuming that both true and complement forms of the input variables are available, draw a circuit to implement F using the minimum number of 2 input NOR gates only		2				
455	4	Simplify the following function using Tabulation method: Show all steps along with PI chart and EPI terms. F(W,X,Y,Z)=∑m(0, 2, 3, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15)						
456	4	Simplify the following function using Tabulation method: F(W,X,Y,Z)=∑m(0,1,2,5,6,7,8,9,10,14)		5				
457	4	Express Function in Maxterms and Minterms: **F(x,y,z) = (xy + z) (y + xz)**		3				
458	4	In certain application, four inputs A, B, C, D (both true and complement forms available) are fed to logic circuit, producing an output F which operates a relay. The relay turns on when F(ABCD)=1 for the following states of the inputs (ABCD):'0000','0010' ,'0101','0110','1101' and '1110'. States '1000' and '1001' do not occur, and for the remaining states, the relay is off. Remaining states, the relay is off. Minimize F with the help of a Karnaugh map and realize it using a minimum number of 3- input NAND gates.		3				
459	5	A digital system consists of _____ types of circuits	A	1	2	3	4	5
460	5	Half-adders have a major limitation in that they cannot _____	C	1	Accept a carry bit from a present stage	Accept a carry bit from a next stage	Accept a carry bit from a previous stage	Accept a carry bit from the following stages
461	5	If A, B and C are the inputs of a full adder then the carry is given by _____	B	1	A AND B OR (A OR B) AND C	A AND B OR (A XOR B) AND C	(A AND B) OR (A AND B)C	A XOR B XOR (A XOR B) AND C
462	5	How many minimum AND, OR and EXOR gates are required for the basic configuration of full adder?	B	1	1, 2, 2	2, 1, 2	3, 1, 2	4, 0, 1
463	5	In a combinational circuit, the output at any time depends only on the _____ at that time.	C	1	Voltage	Intermediate values	Input values	Clock pulses
464	5	Procedure for the design of combinational circuits are: A. From the word description of the problem, identify the inputs and outputs and draw a block diagram. B. Draw the truth table such that it completely describes the operation of the circuit for different combinations of inputs. C. Simplify the switching expression(s) for the output(s). D. Implement the simplified expression using logic gates. E. Write down the switching expression(s) for the output(s).	C	1	B, C, D, E, A	A, D, E, B, C	A, B, E, C, D	B, A, E, C, D
465	5	Implement a combinational circuit of half adder using AOI gate.		3				
466	5	Implement a combinational circuit of half adder using NAND logic gates.		3				
467	5	Implement a combinational circuit of half adder using NOR logic gates.		3				
468	5	Implement a combinational circuit of full adder using only 2- input NAND logic gates.		4				

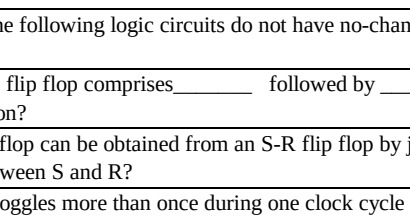
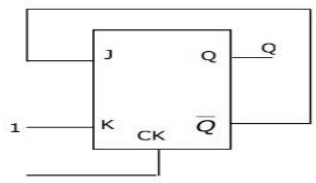
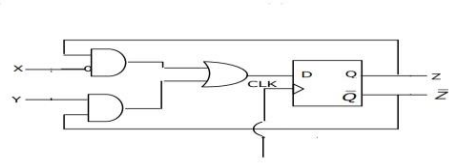
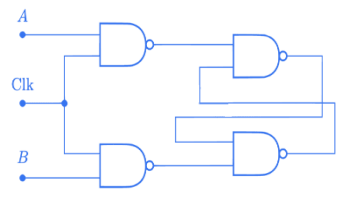
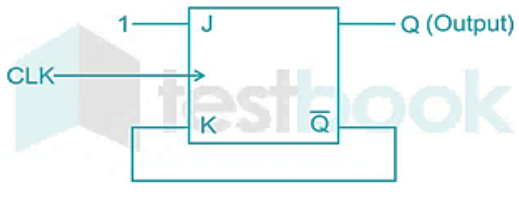
469	5	Implement a combinational circuit of full adder using only 2- input NOR logic gates.		4				
470	5	Implement a combinational circuit of full adder using AOI gates.		3				
471	5	Implement a combinational circuit of half subtractor.		3				
472	5	Implement a combinational circuit of half subtractor using NAND logic gates.		3				
473	5	Implement a combinational circuit of half subtractor using NOR logic gates.		3				
474	5	Implement a combinational circuit of full subtractor using only 2- input NAND logic gates.		4				
475	5	Implement a combinational circuit of full subtractor using only 2- input NOR logic gates.		4				
476	5	Implement a combinational circuit of full subtractor using AOI gates.		3				
477	5	Show how a full-adder can be converted to a full-subtractor with the addition of inverter circuit.		5				
478	5	With logic circuit describe the function of: Full adder,write the simplified Boolean functions for its outputs.		5				
479	5	Design the truth table of full adder and implement using minimum number of logic gates.		4				
480	5	Design the truth table of full subtractor and implement using minimum number of logic gates.		4				
481	5	Design a full adder circuit using two half adders and gates.		4				
482	5	Differentiate between serial and parallel adders.		3				
483	5	In a half-subtractor circuit with X and Y as inputs, the Borrow (M) and Difference (N = X - Y) are given by	M=X'Y,N=X⊕Y	1	M=X⊕Y,N=XY	M=XY,N=X⊕Y	M=X'Y,N=X⊕Y	M=X'Y,N=(X⊕Y)'
484	5	A combinational logic circuit has memory characteristics that "remember" the inputs after they have been removed.	False	1				
485	5	To implement the full-adder sum functions, two exclusive-OR gates can be used.	True	1				
486	5	A half-adder does not have _____.	A	1	carry in	carry out	two inputs	all of the above
487	5	Which of the statements below best describes the given figure? 	A	1	Half-carry adder; Sum = 0, Carry = 1	Half-carry adder; Sum = 1, Carry = 0	Full-carry adder; Sum = 1, Carry = 0	Full-carry adder; Sum = 1, Carry = 1
488	5	A full-adder adds _____.	A	1	two single bits and one carry bit	two 2-bit binary numbers	two 4-bit binary numbers	two 2-bit numbers and one carry bit
489	5	The carry propagation delay in 4-bit full-adder circuits:	A	1	is cumulative for each stage and limits the speed at which arithmetic operations are performed	is normally not a consideration because the delays are usually in the nanosecond range	decreases in direct ratio to the total number of full-adder stages	increases in direct ratio to the total number of full-adder stages, but is not a factor in limiting the speed of arithmetic operations
490	5	Two 4-bit binary numbers (1011 and 1111) are applied to a 4-bit parallel adder. The carry input is 1. What are the values for the sum and carry output?	C	1	∑4 ∑3 ∑2 ∑1=0111, C_{out} = 0	∑4 ∑3 ∑2 ∑1 = 1111, C_{out} = 1	∑4 ∑3 ∑2 ∑1= 1011, C_{out} = 1	∑4 ∑3 ∑2 ∑1= 1100, C_{out} = 1
491	5	A full-adder has a C_{in} = 0. What are the sum 0 and the carry (C_{out}) when A = 1 and B = 1?	B	1	∑= 0, C_{out} = 0	∑ = 0, C_{out} = 1	∑= 1, C_{out} = 0	∑= 1, C_{out} = 1
492	5	An adder in which bits of the operand are added one after another_____	C	1	Half adder	Half subtractor	Serial Adder	parallel Adder
493	5	What is the major difference between half-adders and full-adders?	C	1	Full-adders are made up of two half-adders	Full adders can handle double-digit numbers	Full adders have a carry input capability	Half adders can handle only single-digit numbers
494	5	A combinational circuit calculates the arithmetic sum in a parallel way. What is the name of the adder?	B	1	Sequential Adder	Parallel Adder	Serial Adder	Both 1) & 2)
495	5	To implement a half adder and half subtractor ,the no. of basic(AND,OR,NOT) gates required is____ and ____ respectively.	6,5	1				
496	5	A binary half-subtractor having two inputs A and B, the correct set of logical outputs D(=A minus B) and X(=borrow) are 1.The difference output D=A'B+AB' 2.The borrow output B=AB' Which of the above is/are correct?	A	1	1 Only	2 Only	none	Both 1 and 2
497	5	The number of full and half-adders required to add 16-bit numbers is	B	1	8half-adders, 8 full-adders	1 half-adder,15 full-adders	16 half-adders, 0 full-adders	4 half-adders, 12 full-adder
498	5	How Serial Adder differ from Parallel Adders?		1				
499	5	The half-adder can be implemented from which of the following equation?	D	1	S = xy′ + x′y C = xy	S = (x + y) (x′ + y′) C = x y	S = (C + x′y′)′ C = xy	All of above
500	5	Full adder has____	A	1	3 inputs	8 inputs	4 inputs	10 inputs
501	5	half adder is an example of-	A	1	Combinational circuit	Sequential circuit	Asynchronous circuit	None of these
502	5	How many full adders are needed to add two 4-bit numbers with a parallel adders?	B	1	2	4	16	8
503	5	The logic diagram shown in the figure performs the function of building block 	A	1	Half adder	Full adder	Half substractor	Multiplier
504	5	Two binary digits are applied to input of two input Ex-or gate. The output of the logic can generate	C	1	Sum output	Difference output	Either sum or difference output	Carry output of a half adder
505	5	Two binary digits are applied to the input of two input AND gate. The output of the logic can generate	B	1	Borrow out of half substractor	Carry out of half adder	Sum output of half adder	Difference output of half adder
506	5	Number of half and full adder required to construct a sixty four bit binary adder would be	A	1	One half adder and 63 full adders	64 full adders	64 half adders	one full adder and 63 half adder
507	5	A full substractor can be constructed from two half substractor and one	A	1	Two input OR gate	Two input AND gate	Two input Ex-or gate	Three input OR gate
508	5	A full adder can be constructed from two half adder and one	A	1	Two input OR gate	Two input AND gate	Two input Ex-or gate	Three input OR gate

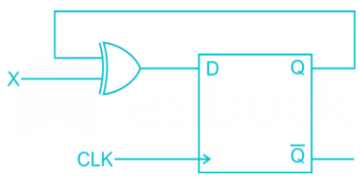
509	5	A 4 ×1 MUX is shown in the figure below, the output Z is_____ (Where S1 is MSB and S2 is LSB) 	D	1	F(A,B,C) = A ⊕ C	F(A,B,C) = A⊙C	F(A,B,C) = (A⊙C)'	Both 1 and 3
510	5	A, B and Cin are the three inputs of a full adder circuit and D0, D1, ..., D7 are the inputs of 8×1 multiplexer. S2 (MSB), S1 and S0 (LSB) are the selection lines of the multiplexer. To implement the expression of sum of full adder circuit using this multiplexer, the connections of the input ports and selection lines are	A	1	D0=D3=D5=D6=0,D1=D2=D4=D7=1, S2=A,S1=B and S0=Cin	D0=D3=D5=D6=1,D1=D2=D4=D7=0,S2=Cin,S1=B and S0=A	D0=D2=D3=D6=0,D1=D4=D5=D7=1,S2=A,S1=B and S0=Cin	D0=D1=D5=D7=1, D2=D3=D4=D6=0, S2=Cin,S1=B and S0=A
511	5	There are eight news channels are connected at 8:1 MUX with the selection line of S2, S1, S0: if Ch-1 as “AAJ TAK”, Ch-2 as “NDTV”, Ch-3 as “24x7”, Ch-4 as “ZEE NEWS”, Ch-5 as “INDIA TV”, Ch-6 as “BBC NEWS”, Ch-7 as “TV18”, Ch-8 as “DD NEWS” and Selection lines are S2, S1, S0 as 101 so which channel would be selected:	C	1	AAJ TAK	NDTV	BBC NEWS	TV18
512	5	What are the advantages of parallel adders over serial adders? Two 4-bit binary numbers (1011 and 1111) are applied to a 4-bit parallel adder. The carry input is 1. What are the values for the sum and carry output?		4				
513	5	Design Truth Table and give Boolean function for Full-Subtractor circuit and implement it using half subtractor and gates.		4				
514	5	Which of the following statements is/are not correct? 1) A half-adder is an arithmetic circuit that adds two binary digits. 2) A half-subtractor is an arithmetic circuit that subtracts two binary digits. 3) A full-subtractor is an arithmetic circuit that subtracts two binary digits along with borrow bit. 4) A full-adder is an arithmetic circuit that adds one binary digit and carry bit.	B	1	Only 1	Only 4	Only 3	Only 2
515	5	Which of the following is correct Boolean function of sum and carry of Full adder, the inputs are A, B and C (internal carry)?	C	1	S = A xor B xor C, Cout = AB + BC’ +AC	S = A xnor B xor C, Cout = AB + BC +AC	S = A xor B xor C, Cout = AB + (A xor B).C	S = A xor B xor C, Cout = AB + (A xor B’).C
516	5	Which of the following Boolean function of difference and borrow out (Bout) of full subtractor circuit, if the inputs are A, B and C (previous borrow)?	B	1	D = A XOR B XOR C, Bout = A’B + AC + B’C’	D = A XOR B XOR C, Bout = A’B + A’C + BC	D = A XOR B XOR C, Bout = A’B + A’C + B’C	D = A XOR B XOR C, Bout = AB + AC + BC
517	5	The logic diagram shown in the following figure performs the function of a very common arithmetic building block. Identify the logic function. 	A	1	Half subtractor	Full adder	Full subtractor	Half adder
518	5	In BCD addition, 0110 is required to be added to the sum for getting the correct result, if -	D	1	The sum of two BCD numbers is not a valid BCD number	The sum of two BCD number is greater than (1010)BCD only	a carry is produced	Both A and C
519	5	Design the digital circuit that adds $(8)_{BCD}$ with $(7)_{BCD}$ in parallel and produces a sum digit also in BCD format. Show the appropriate circuit diagram and steps that describe the BCD addition process.		4				
520	5	Design Binary Parallel Adder for addition of two binary numbers A= 1010 and B= 1110		2				
521	5	Design 4-Bit BCD adder which perform BCD addition of two decimal number 5 and 7.		3				
522	5	Design Logic diagram of Full adder and Full Subtractor with the help of truth table and logical equation.		4				
523	5	How many full adders are needed to add 4-bit numbers A and B with a Serial adder?	A	1	1	8	16	4
524	5	which of the following statement/s are true , I) In combinational circuits, memory are used for store the previous input so output of combinational circuits is depends on present as well as previous inputs. II) for n bit additions of binary number, number of full adder required for these is (n-1)n III) In full adder & full subtractor , there is similarity of sum bit (s) in case of full adder & borrow bit (bin) in case of full subtractor. IV) In output of BCD adder has range for sum output in 00000 to 10001.	d	1	a) i, ii, iii, iv	b) i, ii, iii	c)i, iii, iv	d) none of the above
525	5	Illustrate the adder circuit which adds two 4 bit numbers which are (3)BCD & (9)BCD through BCD addition & obtain the answer in BCD form.		5				
526	5	Illustrate the Addition of (15)10 & (7)10 By using binary adders of which requires an n-full adder for n-bit addition. (with logic diagram)		3				
527	5	Illustrate the combinational circuits that subtracts one bit from another one bit, when already there is a borrow from this column for subtraction in preceding column, and outputs the difference bit and borrow bit along with truth table, Boolean function & logic circuit diagram.		3				
528	5	Which statement/s is/are true? 1) A half adder is also known as XNOR gate because XNOR is applied to both inputs to produce the sum. 2) Half adder can add only two bits (A and B) and has nothing to do with the carry. 3) If the input to a half adder has a carry, then it will neglect it and adds only the A and B bits that means the binary addition process is not complete and that’s way it is called a half adder. 4) A half adder is a two input and two output combinational circuit.	b	1	both 1 and 2	Three 2, 3 and 4	Three 1,3 and 4	All of the above
529	5	Design the digital circuit that adds (8)BCD digit with (5)BCD digit in parallel and produces a sum digit also in BCD.		4				

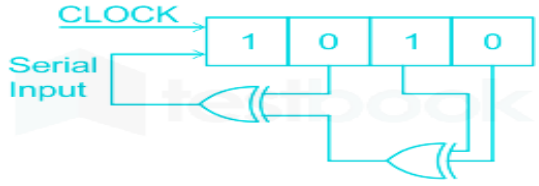
530	5	Design a 4-bit parallel adder to find the sum and output carry for the addition of the following two 4-bit numbers which are A0A1A2A3 = 1011 and B0B1B2B3 = 1111 and the input carry (C0) is 0. List bitwise sum and output carry for the 4-bit parallel adder.		2				
531	5	Design the digital circuit that adds $(7)_{BCD}$ with $(9)_{BCD}$ in parallel and produces a sum digit also in BCD format. Show the appropriate circuit diagram and steps that describe the BCD addition process.		4				
532	5	Design a combinational circuit that generates BCD sum of (3)BCD and (9)BCD number with necessary equations and truth table.		3				
533	5	Design a combinational circuit that add $(9)_{BCD}$ and $(8)_{BCD}$ number with necessary equations.		4				
534	5	Implement F (P,Q,R) =PR′+P′QR′+Q′R+P′ by using 3x8 line decoder.		2				
535	5	Illustrate the comparison circuit of two numbers A & B having the bit value is 3 bits as A2A1A0 and B2B1B0, using suitable comparator with block diagram and logic diagram.		3				
536	5	Implement F (W, X, Y, Z) = ΠM (1,4,7,10,12) using 8x1 MUX having Y as input to MUX and W, X and Z as selection lines of MUX.		3				
537	5	Prove that a full adder can be obtained by two half adder and an OR gate.		3				
538	6	_____ is the example of multiplexer.	D	1	2 x 1	1 x 2	4 x 1	both (a) & (c)
539	6	_____ is used for connecting two or more sources to a single destination among computer units.	B	1	De-multiplexer	Multiplexer	encoder	decoder
540	6	A multiplxer is also called as _____	C	1	data collector	data distributor	data selector	data controller
541	6	2 to 1 line multiplexer can be realized using _____	D	1	1 AND, 2 OR & 1 NOT gates	2 AND, 2 OR & 1 NOT gates	2 AND, 1 OR & 2 NOT gates	2 AND, 1 OR & 1 NOT gates
542	6	_____ is the major functioning responsibility of the multiplexing combinational circuit?	C	1	Decoding the binary information	Generation of all minterms in an output function with OR-gate	Generation of selected path between multiple sources and a single destination	Encoding of binary information
543	6	_____ logic inputs should be given to the input lines Io, I1, I2 and I3, if the MUX is to behave as two input XNOR gate? 	B	1	110	1001	1010	1111
544	6	_____ is the function of an enable input on a multiplexer chip?	C	1	To apply Vcc	To connect ground	To active the entire chip	To active one half of the chip
545	6	A 4 ×1 MUX is used to implement a 3 - input boolean function as shown in figure. The boolean function F(A,B,C) implement is_____ 	A	1	F(A,B,C) = Σ(1,2,4,6)	F(A,B,C) = Σ(1,2,6)	F(A,B,C) = Σ(2,4,5,6)	F(A,B,C) = Σ(1,5,6)
546	6	In a multiplexer, the selection of a particular input line is controlled by _____	B	1	Data controller	Selection lines	Logic gates	Both data controller and selected lines
547	6	_____select lines would be required for an 8-line-to-1-line multiplexer.	D	1	2	4	8	3
548	6	_____ NOT gates are required for the construction of a 4-to-1 multiplexer.	A	1	2	5	3	4
549	6	The output of the 4 to 1 MUX shown in figure is: 	B	1	x' + y'	x + y	xy + x'	(xy)' + x
550	6	_____ is the output of design. 	A	1	w'xy'z' + wx'y'z' + xy + yz	wx'yz + w'xyz + x'y' + y'z'	w'xy'z' + w'x'y'z + yz' + zx	w'xyz + wxyz' + gz + z'x'
551	6	Design and elaborate 2 x 1 multiplexer.		4				
552	6	Implement and elaborate 4 x 1 multiplexer.		4				
553	6	Construct and elaborate 8 x 1 multiplexer.		4				
554	6	Realize the following function of three variables with 8:1 MUX. F (A, B, C) = Σ (0, 1, 3, 4, 7)		4				
555	6	Obtain an 8 to 1 multiplexer with a dual 4 to 1 line multiplexers having separate enable inputs but common selection lines. Use a block diagram construction.		5				
556	6	Implement the following function with a multiplexer: F (A, B, C, D) = Σ (0, 1, 3, 4, 8, 9, 15)		4				
557	6	_____ is the example of Demultiplexer.	B	1	2 x 1	1 x 2	4 x 1	both (a) & (c)
558	6	How many selector lines required in a single input n- output demultiplexer ?	D	1	2	n	2^n	log n(base 2)
559	6	The word demultiplex means _____	D	1	One into many	Many into one	Distributor	One into many as well as Distributor
560	6	In 1-to-4 demultiplexer, _____ select lines are required	A	1	2	3	4	5
561	6	Most demultiplexers facilitate _____ type of conversion	B	1	Decimal-to-hexadecimal	Single input, multiple outputs	AC to DC	Odd parity to even parity
562	6	Design and elaborate 1 x 2 demultiplexer.		4				
563	6	Implement and elaborate 1 x 4 demultiplexer.		4				
564	6	Construct and elaborate 1 x 8 demultiplexer.		4				

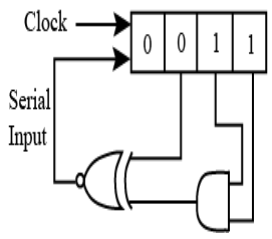
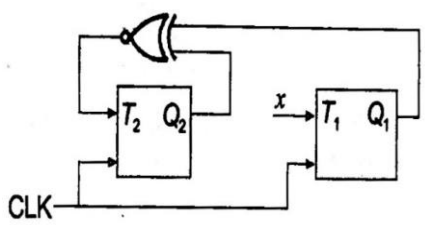
565	6	_____ converts binary coded information to unique outputs such as decimal, octal digitals etc.	A	1	decoder	demultiplexing	multiplexing	encoder
566	6	In a decoder, if the input lines are 4 then_____ number of maximum output lines .	B	1	2	16	4	8
567	6	_____ can be represented for decoder.	B	1	Sequential circuit	Combinational circuit	Logical circuit	None of the mentioned
568	6	BCD to seven segment conversion is a _____	A	1	Decoding process	Encoding process	Comparing process	None of these
569	6	With which decoder it is possible to obtain many code convertions?	D	1	2 line to 4 line	3 to 8 line	not possible with any decoder	4 to 16 line
570	6	A device which converts BCD to seven segment is called as _____.	C	1	multiplexer	encoder	decoder	inverter
571	6	For design 3 to 8 decoder _____ 2 to 4 decoder is required.	D	1	3	5	4	2
572	6	When _____ the outputs either don't change or they are invalid in SR latch.	C	1	S=R=0	S=R=1	Both A & B	S=0, R=1
573	6	Decoder is constructed from _____.	C	1	Inverters	AND gates	Inverters and AND gates	None of the mentioned
574	6	Design and elaborate 3 to 8 line decoder.		5				
575	6	Implement half adder using 2 × 4 line decoder.		2				
576	6	Implement full adder circuit using 3 × 8 line decoder		4				
577	6	Design and elaborate 2 to 4 line decoder.		5				
578	6	Consider the logic circuit given below. The minimized expression for F is ____ 	A	1	C'	Io	C	Io'
579	6	Implement A + B'C' by using 3 × 8 line decoder.		3				
580	6	Construct binary to octal decoder and justify with block diagram.		4				
581	6	For 8-bit input encoder_____ combinations are possible	B	1	8	2^8	4	2^4
582	6	Design Octal to Binary encoder.		4				
583	6	Design 4 × 2 encoder logic diagram with truth table.		5				
584	6	Implement 8 × 3 encoder logic circuit along with truth table.		5				
585	6	_____ is the 4 bit gray code of binary number 1010 .	B	1	1110	1111	1101	1011
586	6	_____ is the binary number of 1110 gray code.	A	1	1011	1101	1010	110
587	6	Design and implement a 4 bit binary to gray code converter		5				
588	6	Design and implement a 4 bit gray to binary code converter		5				
589	6	Design and implement a BCD to seven segment code converter		4				
590	6	If A & B is 1 and 0 respectively then _____ will be output.	B	1	A = B	A > B	A < B	A'B
591	6	_____ gate is basic comparator.	C	1	NOR	NAND	XNOR	NOT
592	6	Two inputs are $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$ gives 4-bit equality condition then _____ will be implementation.	B	1	A . B	A ⊙ B	A + B	A > B
593	6	When in comparator A & B is coincide then _____ is the output.	C	1	A > B	A < B	A = B	A.B
594	6	Implement 1- bit magnitude comparator with logic diagram.		4				
595	6	Design 2- bit comparator with logic diagram.		5				
596	6	_____ number of x-or gates used in 3 bit even parity generator.	D	1	3	4	5	2
597	6	Design an SOP circuit that will generate an odd parity bit for 3-bit input.		5				
598	6	Implement logic circuit for the 3-bit even parity generator along with k-map.		5				
599	6	Design for P = Σm(0, 3, 5, 6) parity generator with logic diagram.		5				
600	6	_____ variables required for 4 bit even parity checker.	D	1	1	2	3	4
601	6	_____ times 1's possible in 4-bit even parity checker.	A	1	8	7	6	9
602	6	For error detection and correction codes ,_____ functions are very useful in the system.	C	1	NAND	NOR	EX-OR	OR
603	6	_____ number of x-or gates required in 4 bit even parity checker.	B	1	2	3	4	5
604	6	Design k- map for 4- bit odd parity checker.		4				
605	6	Design SOP expression of P = Σm (0, 3, 5, 6, 9, 10, 12, 15) parity checker with k-map and logic diagram.		6				
606	6	Design a combinational circuit and evaluate expression for binary to gray code converter for given binary input B3B2B1B0 and gray output G3G2G1G0.		4				
607	6	Design full subtractor logic circuit using 3x8 decoder and OR gates. Use X, Y and Z as input variables and D & B as output variables		3				
608	6	Which logic gate is generated for multiplexer inputs B' (MSB) and 1 (LSB) having selection line A?	A	1	NAND	OR	NOR	XNOR
609	6	How many 2x1 multiplexers are required for implementing 16x1 multiplexer?	C	1	12	11	15	16
610	6	Find F for given circuit. 		1				
611	6	If the number of n generated output lines is equal to 2^m in demultiplexer then it requires _____ selection lines.		1				
612	6	In the circuit shown, W and Y are MSB's of select inputs. The output function F is given by - 		1				

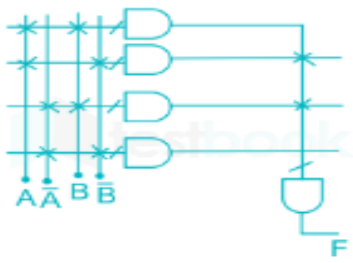
613	6	Which of the above statement/s is/are correct? 1. A 8-to-3 line decoder is also called as binary to octal decoder. 2. A DEMUX circuit is also known as data selector circuit. 3. A 8-to-1 MUX routes the desired data input to the output is controlled by 2 select lines. 4. For an n:1 multiplexer the number of select lines are given by $\log_n 2$	D	1	Both 1 and 2	Both 1 and 4	only 3	None of the given
614	6	Design two input NOR gate and XNOR gate using 2-to-1 line Multiplexer.		2				
615	6	Implement the function F(A,B,C,D) = A'B+CD'+AC' using MUX with 3 select lines. Use B, C, and D as select lines.		3				
616	6	The Combinational Logic Circuit with the function of P (A, B, C) = Σm(1, 2, 4, 7) is _____ parity generator with expression _____	A	1	Even Parity, A XOR B XOR C	Odd Parity, A XOR B XOR C	Even Parity, A XNOR B XOR C	Odd Parity, A XOR B XNOR C
617	6	Design a Combination Logic Circuit which accepts 3-Bit gray number and provide its binary equivalent as output.		3				
618	6	Construct Binary to Octal Decoder along with truth-table and equation. Also Implement Full adder using decoder.		3				
619	6	Design a combinational logic circuit that compare single bit binary numbers A and B to check if they are equal, greater or less.		3				
620	6	A MUX network is shown in fig. What is the value of output Z1 = ? 		1				
621	6	A logic circuit of 2 x 4 decoder shown in figure , output of decoder are as follow : D0 = A'0 A'1 , D1 = A'0 A1, D2 = A0 A'1 , D3= A0 A1. Then value of f(x,y,z) =…… 	c	1	a) 0	b) z	c) z'	d)1
622	6	The output Y of a 2-bit comparator is logic 1 whenever the 2- bit input A is greater than the 2-bit input B. The number of combination for which the output is logic is 1 is __	b	1	a) 4	b) 6	c) 8	d)10
623	6	During the design of BCD to 7 segment decoder (or converter) , what value is initialized to display 9 ? (options are in decimal equivalent of outputs of decoder)	b	1	a) 126	b) 123	c)127	d)115
624	6	Design NAND logic gate & NOR logic gate using 2x1 multiplexer.		3				
625	6	The logic function F(A,B,C,D) =AC+ ABD + ACD is to be realised using 8x1 mux using the variable B,C,D as control input.		3				
626	6	Illustrate the comparison circuit of two numbers A & B having the bit value is 1 nibble to each numbers, using suitable comparator with block diagram and logic diagram.		5				
627	6	The Boolean function realized by the logic circuit shown is 	a	1	F=∑m(2,3,5,7,8,9,12)	F=∑m(2,3,4,,5,7,8,9,12)	F=∑m(2,3,5,8,9,12)	F=∑m(2,3,5,7,8,9,11)
628	6	Find F for given circuit. 	d	1	F=∑m(1,4,7)	F=∑m(1,2,4,7)	F=∑m(1,2,4,5,6)	F=∑m(0,2,3,5,6)
629	6	Identify that this K-Map belongs to which digital circuit? 	C	1	Odd parity generator	Odd parity checker	Even parity checker	Even parity generator
630	6	Design a combinational circuit with three inputs x,y, and z and three outputs A,B, and C. when the binary input is 0,1,2 or 3, the binary output is one greater than the input. When the binary input is 4,5,6 or 7, the binary output is one less than the input.		4				
631	6	Implement the function F(W, X, Y, Z) =WX + WYZ + XYZ using MUX with 3 select lines. Use W, Y, and Z as select lines and X as a Data input.		4				

632	6	Design a combinational logic circuit which converts 4-bit Gray input (G3G2G1G0) to binary output (B3B2B1B0) with necessary equations.		4				
633	6	Design a full subtractor circuit using 3*8 decoder with its diagram.		3				
634	6	A magnitude comparator is a digital comparator which has ___ output terminals.	c	1	1	2	3	4
635	6	A logic circuit takes 4-BCD inputs {A, B, C and D) to give an output F. Output F is '1' if the input is an invalid BCD-code. The minimized Boolean equation is ____	b	1	AC+BD	AB+AC	B'C+AD'	A'B+A'C
636	6	The network shown in given figure is ___ 	b	1	OR gate	NAND gate	XOR gate	NOR gate
637	7	Which of the following flip-flops is free from the race around problem?	C	1	T flip-flop	SR flip-flop	Master-Slave Flip-flop	D flip-flop
638	7	The characteristic equation of S-R latch is _____	A	1	Q(n+1) = S + Q(n)R'	Q(n+1) = SR + Q(n)R	Q(n+1) = S'R + Q(n)R	Q(n+1) = S'R + Q'(n)R
639	7	D flip flop can be made from a J-K flip flop by making	D	1	J=K	J=K=1	J=0,K=1	J=K'
640	7	In a J-K flip flop, when Jn = 0 and Kn = 1, the output Qn+1 will have a value of:	B	1	1	0	Qn	Qn+1
641	7	In JK flip flop, which combination will toggle the output?	B	1	J=0,K=0	J=1,K=1	J=1,K=0	J=0,K=1
642	7	Master slave flip flop is also referred to as?	B	1	Level triggered flip flop	Pulse triggered flip flop	Edge triggered flip flop	Edge-Level triggered flip flop
643	7	In a positive edge triggered JK flip flop, a low J and low K produces?	D	1	High state	Low state	Toggle state	No Change State
644	7	How is a J-K flip-flop made to toggle?	D	1	J = 0, K = 0	J = 1, K = 0	J = 0, K = 1	J = 1, K = 1
645	7	D flip-flop is a circuit having _____ along with one inverter.	C	1	2 NAND gates	3 NAND gates	4 NAND gates	5 NAND gates
646	7	When is a flip-flop said to be transparent?	B	1	When the Q output is opposite the input	When the Q output follows the input	When you can see through the IC packaging	When the Q output is complementary of the input
647	7	On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when _____	C	1	The clock pulse is LOW	The clock pulse is HIGH	The clock pulse transitions from LOW to HIGH	The clock pulse transitions from HIGH to LOW
648	7	The output Qn of J-K flip flop is 1. It changes to 0 when a clock pulse is applied. The inputs Jn and Kn are respectively	C	1	0 and X	1 and X	X and 1	X and 0
649	7	In a J-K flip flop, when J = 1 and K = 1 then it will be considered as	D	1	set conditions	reset conditions	no change	toggle condition
650	7	Which of the following logic circuits do not have no-change condition?	D	1	JK-FF	SR-FF	T-FF	D-FF
651	7	In J-K-M-S flip flop comprises_____ followed by _____ configuration?	D	1	S-R flip-flop, S-R flip flop	S-R flip-flop, J-K flip flop	J-K flip-flop, J-K flip flop	J-K flip-flop, S-R flip flop
652	7	Which flip flop can be obtained from an S-R flip flop by just putting one Inverter between S and R?	B	1	T	D	J-K	latch
653	7	If a JK FF toggles more than once during one clock cycle it is called	A	1	racing	pinging	spiking	bouncing
654	7	In a D flip flop the output state Q is related with D input in what way?	A	1	Q is same as D	Q is complement of D	Q is independent of D	Q is dependent of D
655	7	In a J_K flip-flop, we have J= Q' and K=1 (see figure). Assuming the flip-flop was intially cleared and then clocked for 6 pulses, the sequence at the Q output will be 	D	1	010000	011001	010010	010101
656	7	In figure, A = 1 and B = 1. The input B is now replaced by a sequence 101010 ___, the outputs x and y will be	A	1	fixed at 0 and 1, respectively	x = 1010…. While y = 0101….	x = 1010…. While y = 10101….	fixed at 1 and 0, respectively
657	7	A sequential circuit using D flip-flop and logic gates is shown in the figure, where X and Y are the inputs and Z is the output. The circuit is 	D	1	S-R Flip flop with inputs X = R and Y = S	S-R Flip flop with inputs X = S and Y = R	J-K Flip flop with inputs X = J and Y = K	J-K Flip flop with inputs X = K and Y = J
658	7	In a master-slave flip-flop, when is the master enabled?	B	1	when the gate is LOW	when the gate is HIGH	both of the above	neither of the above
659	7	Consider the given circuit. In this circuit, the race around 	A	1	Does not occur	occurs when CLK = 0	occurs when CLK = 1 and A=B =1	occurs when CLK = 1 and A=B =0
660	7	Master slave configuration is used in flip flop to	c	1	increase its clocking rate	reduces power dissipation	eliminates race around condition	improve its reliability
661	7	Initial state: Q = 0 The output sequence Q of the circuit shown above is– 	D	1	0000 …….	0001110…	11001100 ……	11111 …….
662	7	In T flip-flop the output frequency is—	C	1	Same as the input frequency	Double of its input frequency	One-half its input frequency	None of these
663	7	A 2MHz clock is applied to J=K=1. What is the frequency of flip flop O/P signal?	B	1	2MHz	1MHz	500 Hz	0
664	7	The output Qn+1 of a J-K flip-flop for the input J =1, K=1 is	D	1	0	1	Qn	Qn'
665	7	The characteristic equation of J-K flip-flop is _____	D	1	Q(n+1)=JQ(n)+K'Q(n)	Q(n+1)=JQ'(n)+KQ'(n)	Q(n+1)=JQ'(n)+KQ(n)	Q(n+1)=JQ'(n)+K'Q(n)

666	7	Find Excitation table of JK,D,T,SR flop flop from their truth table.		4				
667	7	Convert JK flip flop to T flip flop.		4				
668	7	Design master slave JK flipflop.		4				
669	7	Convert T Flipflop in to D flipflop.		4				
670	7	Discuss working of clocked delay type flip-flop with characteristic table and logic diagram.		4				
671	7	Distinguish between combinational and sequential logic circuits.		4				
672	7	Distinguish between latch and flipflops.		2				
673	7	Convert SR flip-flop into JK flip-flop.		4				
674	7	Draw the circuit diagrams and Truth table of all the Flip flops (SR, D, T and JK).		4				
675	7	Implement D flip flop using JK flip flop.		4				
676	7	Convert JK flip flop to SR flip flop.		4				
677	7	Convert D flip flop into SR flip flop.		4				
678	7	Implement T flip flop using D flip flop.		4				
679	7	What is race-around condition in JK flip-flop?		2				
680	7	Design edge triggered flip flop in detail.		4				
681	7	Design S R flip flop usingNAND and NOR gate		4				
682	7	Convert D flip flop into JK flip flop.		4				
683	7	Which flipflop is generated by shorting the inputs of JK flipflop? Evaluate the characteristic equation and give excitation table of generated flipflop.		4				
684	7	Which of the following is/are correct for a D-type flip flop?	C	1	The output toggles if one of the input is held HIGH	The one of the output can be invalid condition	The Q output is either SET or RESET as soon as the D input goes HIGH or LOW	Both inputs are always same with each other
685	7	The output Qn of an SR flip-flop is 1. It changes to 0 when a clock pulse is applied. The inputs S and R respectively –	B	1	X and 1	0 and 1	X and 0	1 and X
686	7	The invalid state of NAND based SR latch occurs when –	B	1	S = 1, R = 1	S = 0, R = 0	S = 1, R = 0	S = 0, R = 1
687	7	Consider the following statements: 1. Race-around condition occurs in a JK flip-flop when the inputs are 1, 1 and CLK = 1. 2. A flip-flop is used to store one bit of information. 3. In active-HIGH SR latch, Set = 1, Reset = 0 indicates RESET state. 4. Master-slave configuration is used in a flip-flop to store 2-bits of information. Which of the above statement/s is/are incorrect?	B	1	Both 1 and 2	Both 3 and 4	Both 2 and 3	all are incorrect
688	7	In a JK flip-flop, output Qn = 1 and it does not change when a clock pulse is applied. What is the possible combination of inputs (Jn, Kn) in this condition?	A	1	(X,0)	(X,1)	(1,0)	(1,X)
689	7	Consider two flip flops X and Y. Flip flop X has single input in which output (Qn+1) follows the input. Flipflop Y has two inputs and output, becomes invalid when both inputs are HIGH. Convert Flip flop X into Y.		4				
690	7	Consider two flip flops A and B. Flip flop A has a single input and positive edge triggered clock pulse, and has a property that output of the next state (Qn+1) is equal to the input. Flip-flop B contains 2 input terminals and positive edge triggered clock pulse. Flip-flop B toggles more than once during one clock cycle. Convert the flip-flop A into B and also show the required steps of conversion.		4				
691	7	In a positive edge triggered T Flip Flop, high T produces?	A	1	TOGGLE STATE	NO CHANGE STATE	INVALID STATE	UNSTABLE STATE
692	7	Which of the following statement/statements is/are true for Master-Slave Flip-Flop? 1) It is a pulse-triggered Flip-Flop 2) This can be used to eliminate the race-around condition. 3) Master is enabled when the clock is at a low level	A	1	ONLY 1 AND 2	ONLY 1, 2 AND 3	ONLY 3	ONLY 2
693	7	Implement SR Flip-Flop using Gated Transparent Latch		3				
694	7	Design two input SET-RESET Flip-Flop which eliminates invalid state and formulate its characteristic equation with the help of truth table.		3				
695	7	Choose the correct statement/s from following . 1) In SR-latch using NAND gates, set & reset input are normally in low state & one of them will be pulsed high whenever we want to change latch output. 2) In SR-lath using NOR gates, set & reset input are normally in high state & one of them will be pulsed low whenever we want to change latch output. 3) Race around condition can be avoided by using level triggered JK flipflop.	d	1	a) 1,2,3	b) 2 & 3	c)1 & 3	d) none of above
696	7	Illustrate the SR-latch using active high input with its logic diagram and truthtable & state that how flip flop is differed from the latch.		3				
697	7	Convert JK flip flop to SR flip flop with the help of characteristics table and excitation table of flipflops & draw the equivalent of logic diagram of converted flip flop.		5				
698	7	In a JK-FF, When Jn=0 and Kn=1, the output Qn+1 will have a value of ___	b	1	1	0	Qn	Qn+1
699	7	How JK-FF can be converted into SR-FF?		4				
700	7	Which flip flop is generated by sorting the inputs of JK flipflop? Evaluate the characteristics equation and give excitation table of generated flipflop.		3				
701	7	Design a pulse triggered flipflop which can eliminates race around condition.		2				
702	7	Discuss how SR flipflop can be made using JK Flipflop.		3				
703	7	____ are the applications of flipflops.	d	1	Storage Devices	Data Transfers	Register	All of above
704	7	The equivalent flip – flop by the circuit shown above is 	c	1	JK	SR	T	Master Slave
705	7	Latches constructed with NOR and NAND gates tend to remain latched condition due to which configuration?	b	1	Gate Impedance	Cross Coupling	Synchronous operation	Asynchronous operation
706	7	An JK flipflop can be converted to T flipflop by connecting___	d	1	J to Q	K to Q	K to Q'	J to K
707	8	Design 4-bit Universal Shift Register.		5				
708	8	An 8 bit serial in/ serial out shift register is used with a clock frequency of 2MHz to achieve a time of delay of	C	1	16µs	8µs	4µs	2µs
709	8	With a 200 khz clock frequency, eight bits can be serially entered into a shift register in	B	1	4 µs	40µs	400µs	40ms

710	8	A serial in/parallel out initially contains all 1s. The data nibble 0111 is waiting to enter, after four clock pulses, the register contains	C	1	0000	1111	0111	1000
711	8	Assume that a 4 bit serial in/ serial out shift register is initially clear. we wish to store the nibble 1100. what will be the 4 bit pattern after the second clock pulse ?	C	1	1100	0011	0000	1111
712	8	SIPO is a abbreviation of	A	1	serial in parallel out	parallel in serial out	serial in serial out	serial in peripheral out
713	8	A function of register is	A	1	Store data	multiplex a data	demultiplex a data	decode a data
714	8	Design 4-bit bidirectional shift register with Parallel load.		4				
715	8	A bidirectional 4 bit nibble is storing the nibble 1110. its input is low. the nibble 0111 is waiting to be entered on the seriall data input line. after two clock pulse the shift register is storing	D	1	1110	0111	1000	1001
716	8	The group of bits 10110111 is serially shifted(right most bit first) into an 8bit parallel output shift register with an initial state 11110000. After two clock pulses, the register contains	D	1	10111000	10110111	11110000	11111100
717	8	Show the working of Universal Shift Register using symbol, block diagram and truth table		5				
718	8	Design a circuit for 4-bits parallel register with load with D Flip-Flops. Load input decides whether to load new input or to apply no change conditions.		5				
719	8	True or False. Data can be changed from special code to temporal code by using Counter.	False (Using Shift register)	1	TRUE	FALSE		
720	8	True or False. A universal shift register has both serial and parallel input and output capacity.	True	1	TRUE	FALSE		
721	8	The shift register is initially loaded with bit pattern 1010. Shift register is clocked in which count gets shifted by one position to right with each shift. The bit at serial input is pushed to left most position(MSB). After how many clock pulse will the content of shift register will be 1010? 	B	1	3	7	11	15
722	8	Which of the following is not the characterstic of shift register?	A	1	Serial in/parallel in	Serial out/parallel in	Serial in/parallel out	Parallel in/parallel out
723	8	True or False. A counter has a specified sequence of states, but a shift register does not.	True	1	TRUE	FALSE		
724	8	Explain the working of 4 bit asynchronous counter.		4				
725	8	Design 4-bit binary ripple counter		4				
726	8	Enlist the classification of counters and Design asynchronous 4-bit binary ripple counter.		4				
727	8	Design 4-bit up-down binary synchronous counter.		4				
728	8	Design 3 bit binary counter with necessary diagrams.		4				
729	8	Design BCD synchronous Counter.		4				
730	8	Design a synchronous Counter that goes 0,2,3,7,0,2,3,…		5				
731	8	Demonstrate about a synchronous counter using 3 bits.		5				
732	8	Design 3-bit synchronous up counter using D flip flop.		4				
733	8	Justify:- A counter works as frequency divider with suitable example.		4				
734	8	Design a synchronous BCD counter with D flip flops.		4				
735	8	Design a mod-12 Synchronous up counter using D-flipflop.		4				
736	8	Design and implement a Modulo – 6 Asynchronous counter using JK flipflop.		4				
737	8	Design and implement a Modulo – 6 Synchronous counter using JK flipflop.		4				
738	8	Enlist the significant difference between synchronous and asynchronous counters.		4				
739	8	Design BCD ripple counter with its operation and develop its logic diagram.		4				
740	8	With logic diagram explain the operation of 4 bit binary ripple counter. Explain the count sequence. How up counter can be converted into down counter?		5				
741	8	Design and explain 4 – bit Ripple UP/ DOWN counter using positive edge triggered Flip flop.		5				
742	8	Design a counter to generate the repetitive sequence 0,1,2,4,3,6.		5				
743	8	Design Modulo-8 counter using D flip flop.		5				
744	8	Design a counter that counts the sequence as 0, 1, 2, 4, 5, 6 and rolls over to 0 again. Use +ve edge triggered D-FF or JK-FF.		5				
745	8	Design and explain BCD Counter.		5				
746	8	Design 4 bit ripple counter using timing diagrams.		5				
747	8	Design 3-bit ripple up-counter using negative edge triggered T-FF or JK- FF . Also draw the waveforms..		5				
748	8	Design a counter to generate the repetitive sequence 0, 3, 5, 7, 4 using D FF.		5				
749	8	Design sequential counter for sequence 0,2,4,3,7,6,1 using JK flip-flops.		5				
750	8	Design a 3-bit synchronous up counter using K-maps and positive edge-triggered JK FFs.		5				
751	8	Design and explain 4-bit Ripple UP/DOWN Counter using negative edge triggered Flipflop.		5				
752	8	Design and implement a Modulo-4 Asynchronous counter using T Flip flop.		5				
753	8	Design and implement a Modulo-6 Asynchronous counter using T Flip flop.		5				
754	8	Design 4-bit ripple counter using negative edge triggered JK flip flop.		5				
755	8	What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of ‘n’ number of flip-flops?	C	1	0 to 2^n	0 to 2^n +1	0 to 2^n - 1	0 to $2^{n+1/2}$ - 1
756	8	Design a counter for following binary sequence 0-1-3-4-6-0		5				
757	8	In a 4 bit johnson counter sequence, there are a total of how many states or bit patterns	D	1	1	3	4	8
758	8	If a 10 bit ring counter has an initial state 1101000000, what is the state after the second clock pulse?	B	1	1101000000	11010000	1100000000	1100000011

759	8	Construct a Johnson counter with Ten timing signals.		4				
760	8	Implement 4-bit ring counter using D FF.		5				
761	8	Design 4 bit twisted ring counter using JK Flip flop.		5				
762	8	For 4 bit Johson counter, If there are four flip flop namely FF0, FF1, FF2 and FF3 the which of the following is true?	A	1	output of FF3 is connected to the input of FF0	output of FF2 is connected to the input of FF1	output of FF3 is connected to the input of FF1	output of FF3 is connected to the output of FF0
763	8	For 4 bit Ring counter, If there are four flip flop namely FF1, FF2, FF3 and FF4 the which of the following is true?	B	1	output of FF3 is connected to the input of FF1	output of FF4 is connected to the input of FF1	output of FF4 is connected to the input of FF2	output of FF4 is connected to the output of FF1
764	8	Design synchronous counter with the following binary sequence: 0, 4,2,1,6,7 and repeat. Use JK flip-flops.		4				
765	8	A 4-bit serial in parallel out shift register is initially set to 1111. The data 1010 is applied to the input. After 3 clock cycles the output will be:		1				
766	8	On the fifth clock pulse, a 4-bit Johnson sequence is Q0 = 0, Q1 = 1, Q2 = 1, and Q3 = 1. On the sixth clock pulse, the sequence is _____.		1				
767	8	What is the time delay (td in μs) of an 8-bit serial-in/serial out shift register with a clock frequency of 4 MHz?		1				
768	8	Consider the following statements: 1. An n-bit ring counter is a mod-2n counter whereas an n-bit twisted ring counter is a mod-n counter. 2. The maximum modulus of ripple counter with seven flip-flops is 14. 3. Series counters have high speed but have more complex circuitry than parallel counters. 4. An n-bit counter has n number of flip-flops, 2^n number of states and also known as divide-by-2n counter. Which of the following statement/s is/are incorrect ?	D	1	3 and 4	2, 3 and 4	1, 2, and 4	1, 2, 3 and 4
769	8	Design a synchronous decade counter using JK-flip-flop.		5				
770	8	Design synchronous counter with the following binary sequence: 0, 4,2,1,6,7 and repeat. Use positive edge triggered T flip-flops.		4				
771	8	Design a synchronous counter which goes through sequence 0, 2, 4, 6, 7, 5, 3, 1, 0, … using positive edge triggered T flip-flops		3				
772	8	Draw the state diagram and state table of BCD ripple counter, develop its logic diagram, and explain its operation using reset input. (No need of waveforms) Use negative edge triggered JK flip-flops.		4				
773	8	Draw 4-Bit Asynchronous Ripple Up/Down Counter using Negative Edge triggered T Flip-Flop		2				
774	8	The shift register shown in figure is initially loaded with the bit pattern 0011. Subsequently the shift register is clocked with each clock pulse the pattern gets shifted by one bit position to the right. With each shift, the bit at the serial input is pushed to the left most position (MSB). Clock pulses taken by the shift register to get the content 0011 again are_____ 	c	1	A) 3rd	b) 4th	c) 5th	d) 6th
775	8	In a Johnson's counter, all the negative triggered J-K flip flop are used. Initially all the flip flops are in reset condition and the outputs are Q3 Q2 Q1 Q0 = 0000. What are the outputs of flip flops after the fifth negative going pulse ?	d	1	0101	1000	0010	1110
776	8	Consider the partial implementation of a 2 bit counter using T-flip flop following the sequence 0-2-3-1-0, as shown below : To complete the circuit the input X should be …… 	c	1	a) Q'2	b) Q2 + Q1	c)Q1 XOR Q2	d) Q1 XNOR Q2
777	8	Design decade counter using JK-FF which is clocked such that each flip-flop in the counter is triggered at the same time.		3				
778	8	How many flip flops are required to design mod-20 counter?	a	1	5	6	10	20
779	8	Design a shift register which gives double number of states from the number of flipflops connected with its state diagram.		4				
780	8	Design a mod-11 asynchronous counter using JK FF with necessary waveforms.		5				
781	9	ROM is made up of _____	DECODER & OR gate	1	NAND & OR gate	NOR & DECODER	DECODER & OR gate	NAND & DECODER
782	9	which of following is non-volatile memory ?	EEPROM	1	RAM	DRAM	EEPROM	SRAM
783	9	ROM has the capability to perform_____	read operation only	1	write operation only	read operation only	both write & read operation	erase operation
784	9	The ROM , which has to be custom built by factory, known as _____	mask ROM	1	EEPROM	MASK ROM	EPROM	PROM
785	9	How does PLA differ from a ROM		2				
786	9	Illustrate the mask rom and compare with it to EPROM		2				
787	9	Illustrate architecture of FPGA & its Application in modern times .		2				
788	9	EPROM contents can be erased by exposing it to infrared rays.	FALSE	1				
789	9	Elucidate that Full subtractor can be implemented using PAL.		2				
790	9	Is PROM differ from PLA & PAL ? if so, illustrate similarities & disimilarities among them.		2				
791	9	Illustrate PLA & compare it with PAL		2				
792	9	PLA can be used ...	to realise a combinational logic	1	as a microprocessor	as a dynamic memory	to realise a sequential logic	to realise a combinational logic
793	9	PALs tend to execute _____ logic	SOP	1	SAP	SOP	PLA	SPD
794	9	Differentiate PAL with PLA.	The PLA has a programmable OR array and a programmable AND array, while the PAL only has a programmable AND Array	1	The PLA has a programmable OR array and a programmable AND array, while the PAL only has a programmable AND Array	The PAL has a programmable OR array and a programmable AND array, while the PLA only has a programmable AND array	The PAL has more possible product terms than the PLA.	PALs and PLAs are the same thing.

795	9	Product terms are the outputs of which type of gate within a PLD array?	AND	1	OR	XOR	AND	FLIP FLOP
796	9	Illustrate PLD 's with FPGA & state application of FPGA		2				
797	9	Implement the following using PLA F1 = ∑(2, 4, 5, 10, 12, 13, 14) and F2 = ∑ (2, 9, 10, 11, 13, 14, 15).		4				
798	9	illustrate neat diagram of an architecture of Field programming gate array & state their advantage over other Programmable logic devices		4				
799	9	A combinational circuit is defined by functions. F1(A,B,C) = ∑(3, 5, 6, 7) & F2(A,B,C) = ∑(0, 2, 4, 7) Implement the circuit with PLA having three inputs, four product term and two outputs		4				
800	9	Implement following functions using ROM. (Use suitable combinational circuit) F1 = Σm(1, 2, 3, 7) F2 = Σm(0, 2, 4, 6)		3				
801	9	Using 8x4 ROM, realize the expressions **F1** = AB'C + ABC' + A'BC, **F2** = A'B'C + A'BC' + AB'C', **F3** = A'B'C' + ABC. Show the contents of all locations.		4				
802	9	A combinational circuit is defined by the function F1 (A, B, C) = Σ m (0,1,2,4) and F2 (A, B, C) = Σ m (0,5,6,7). Implement the circuit with a PLA having 3 inputs, 4 product term & 2 outputs.		4				
803	9	A combinational circuit is defined by the function F1 (A, B, C) = Σ m (4, 5, 7) F2 (A, B, C) = Σ m (3, 5, 7) Implement the circuit with a PLA having 3 inputs, 3 product term & 2 outputs		4				
804	9	Implement the following equation by using PLA. F1 = AB' +AC and F2 = AC + BC		4				
805	9	Tabulate the truthtable for 8x4 ROM and implement the four boolean function listed below. Also minimize A(X,Y,Z) = Σ(1,3,5,6) , B(X,Y,Z) = Σ(0,1,6,7) , C(X,Y,Z) = Σ(3,5), D(X,Y,Z) = Σ(1,2,4,5,7).		4				
806	9	Illustrate the construction in which a 3 bit adressable ROM, the following function are required. h0= Σ(0,2,5,6) h1=Σ(0,2,4,6,7) h2=Σ(0,2,7) h3=Σ(1,2,3,5,7)		4				
807	9	Illustrate the following function using PROM f1=Σm(0,1,3,4,7) & f2=Σm(1,2,5,6)		4				
808	9	Show the connection in PAL to yeild the following Y0= A' + BC' , Y1= A'B'CD + A'BC, Y2 =A'CD + A B, Y3 = A'B + C'D		4				
809	9	The minimum number of AND and OR gates required for implementation of function using PLA is: F1= Σm(0,1,3,6,7) F2= Σm(3,5,6,7)		2				
810	9	Which of the following statement is correct about differentiating PAL and PLA? 1.PALs and PLAs are the same thing 2.The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane 3.The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane 4.The PAL has more possible product terms than the PLA.	A	2	only 2	only 3	only 4	only 1
811	9	Consider the following statement regarding PROM & EPROM 1) erasable programmable ROM using UV erasing is known as EPROM. 2) ROM that makes use of electrical voltage for erasing is known as electrically altered ROM 3)PROM can be programmed many times after fabrication. which of the above statement/s is / are correct ?	B	1	only 3	1 and 2	2 and 3	1 and 3
812	9	Implement the following boolean functions using suitable PAL: w (A,B,C,D) = Σm (1, 3, 4, 6, 9, 11, 12, 14) x (A,B,C,D) = Σm (1, 3, 4, 6, 9, 11, 12, 14, 15) y (A,B,C,D) = Σm (0, 2, 4, 6, 8, 12) z (A,B,C,D) = Σm (2, 3, 8, 9, 12, 13)		4				
813	9	A combinational circuit is defined by functions. F1(A, B, C) = ∑ (0, 1, 2, 3, 6) and F2(A,B,C) = ∑(3, 5, 7). Implement the circuit with PLA having three inputs, three product term and two outputs		5				
814	9	Implement FULL ADDER using Programmable Array Logic		3				
815	9	A combinational circuit is defined by functions: X(A,B,C) = ∑m (2,3,5,7) Y(A,B,C) = ∑m (0,1,5) Z(A,B,C) = ∑m(0,2,3,5) Implement the circuit using PAL.		3				
816	9	FPGA stands for _____	c	1	Full Programmable Gate Array	Full Programmable Genuine Array	Field Programmable Gate Array	Field Programmable Gate Area
817	9	Determine the output of logic array given in the following figure. The X's represent connected link.  	b	1	AB'+A'B	0	1	A'B'+AB
818	9	Implement the following functions using PROM: F1 = A(BC)'+ABC & F2= ABC + (AB)'+AC'.		3				
819	9	Implement the following Boolean functions using PLA with 3 inputs, 3 product terms and 2 outputs. F1 = ∑m(1,3,5) and F2 = ∑m(5,6,7)		4				
820	10	When used with an IC, what does the term "QUAD" indicate?	b	1	2 circuits	4 circuits	6 circuits	8 circuits
821	10	Give comparison of TTL and CMOS family		3				
822	10	Compare following for CMOS and TTL : Figure of merit, Noise margin, and Power dissipation		3				
823	10	Compare for CMOS and TTL: 1) Fan in 2) Noise Margin 3) Propagation Delay		3				
824	10	_____ is the measure of maximum number of inputs that a single gate output can drive or accept.	Fan-in	1				
825	10	_____ means the maximum number of inputs that can be fed by a single output.	Fan-out	1				

826	10	Propagation delay is defined as _____	a	1	the time taken for the output of a gate to change after the inputs have changed	the time taken for the input of a gate to change after the outputs have changed	the time taken for the input of a gate to change after the intermediates have changed	the time taken for the output of a gate to change after the intermediates have changed
827	10	CMOS refers to _____	b	1	Continuous Metal Oxide Semiconductor	Complementary Metal Oxide Semiconductor	Centred Metal Oxide Semiconductor	Concrete Metal Oxide Semiconductor
828	10	Fan-in and Fan-out are the characteristics of _____	b	1	Registers	Logic families	Sequential Circuits	Combinational Circuits
829	10	Which logic family consumes the less power?	a	1	CMOS	TTL	PMOS	NMOS
830	10	Implement NAND gate using CMOS logic		2				
831	10	Implement NOR gate using CMOS logic		2				
832	10	TTL stands for _____	b	1	Totempole Logic	Transistor transistor logic	Transistor totempole Logic	None of Above
833	10	Which of the IC families have the largest fan-out?	a	1	CMOS	NMOS	PMOS	TTL
834	10	The figure of merit of a logic family is given by the product of	b	1	gain and bandwidth	propogation delay time and power dissipation	fan-out and propagation delay time	noise margin and power dissipation
835	10	Which equation is correct?	d	1	$V_{NL} = V_{IL}(max) + V_{OL}(max)$	$V_{NH} = V_{OH}(min) + V_{IH}(min)$	$V_{NL} = V_{OH}(min) – V_{IH}(min)$	$V_{NH} = V_{OH}(min) – V_{IH}(min)$
836	10	If a logic circuit has fan out 4 it means .	c	1	It has 4 inputs	It has 4 outputs	It can drive maximum 4 inputs	It can give 4 times the input
837	10	Classify the logic families. Give comparison with the advantages and disadvantages of CMOS and TTL logic families.		4				
838	10	The digital logic family which has minimum power dissipation is_____ .	CMOS	1				
839	10	Compare CMOS and TTL in terms of Power dissipation, Fan-out, Noise margin and Propagation delay. Also implement NAND gate using TTL and CMOS logic.		5				
840	10	Implement NAND gate using logic family which has very low power dissipation per gate compare to other logic families.		2				
841	10	Design NOR gate using CMOS logic with its working principle and compare TTL and CMOS logic families, highlighting their unique features and characteristics.		3				
842	10	Implement 2 input NAND Gate using TTL Logic		2				
843	10	Compare CMOS over TTL logic families & illustrate NAND & NOT logic gates using CMOS.		3				
844	10	Define following terms: 1) Fan Out 2) Noise margin		2				