

# Input Protection

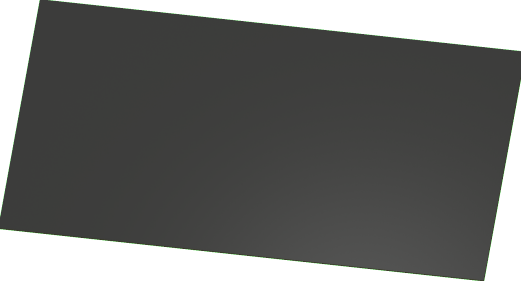
## Variant: DRAFT

2026-02-07

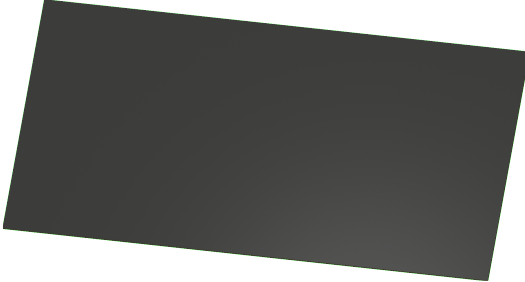
Rev + (Unreleased)

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### TOP VIEW



### BOTTOM VIEW



### NOTES

Comment

Not fitted components are marked as **X**

**DRAFT** – Very early stage of schematic, ignore details.

**PRELIMINARY** – Close to final schematic.

**CHECKED** – There shouldn't be any mistakes. Contact the engineer if found.

**RELEASED** – A board with this schematic has been sent to production.

### DESIGN CONSIDERATIONS


DESIGN NOTE:  
Example text for  
informational design  
notes.

DESIGN NOTE:  
Example text for  
debug notes.

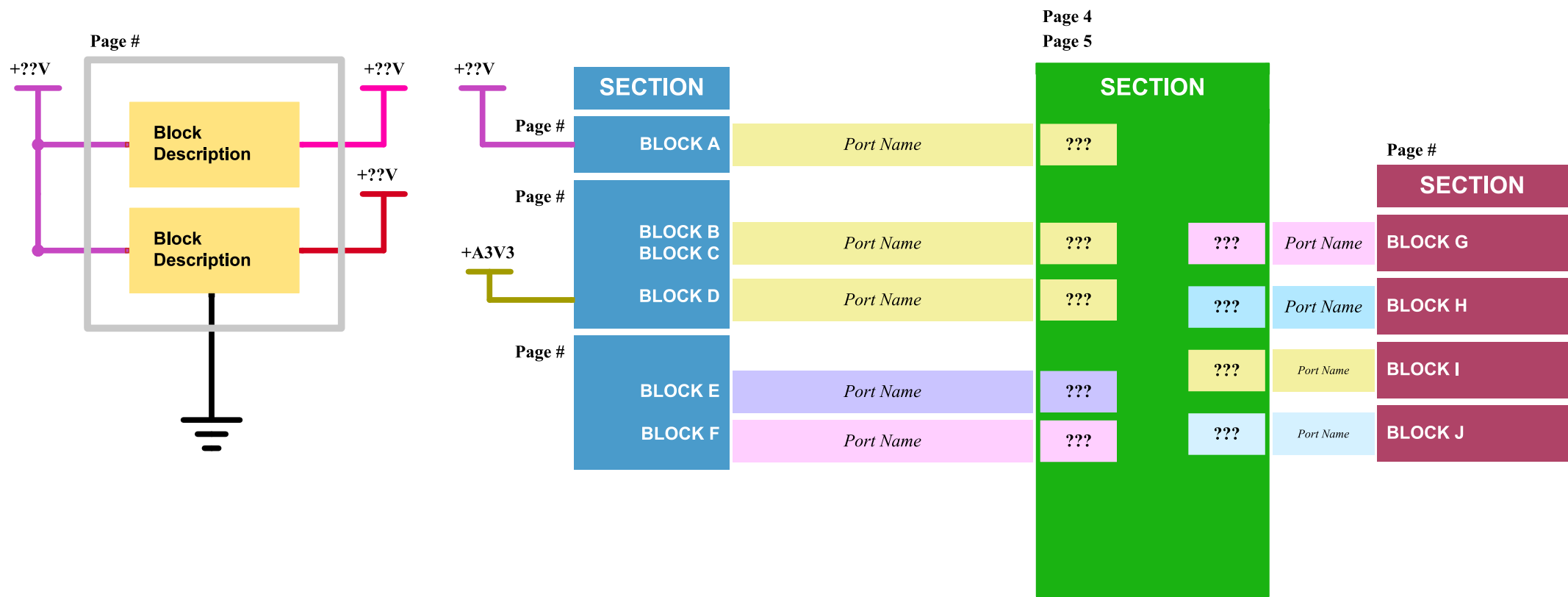
DESIGN NOTE:  
Example text for  
cautionary design  
notes.

DESIGN NOTE:  
Example text for  
critical design  
notes.

LAYOUT NOTE:  
Example text for  
critical layout  
guidelines.


|  |  |                                  |    |
|--|--|----------------------------------|----|
| PROJECT<br>Assignment 1                | <div> <b>Ryan Dynamics</b></div> <div>THIS DESIGN AND/OR DRAWING IS THE PROPERTY OF RYAN DYNAMICS AND SHALL NOTBE REPRODUCED WITHOUT AUTHORISATION.</div> |                                  |    |
| DRN<br>2025-01-12 R. HICKS             |  |                                  |    |
| CHK                                    |  |                                  |    |
| ENG APP                                | Input Protection   |                                  |    |
| MFR APP                                |  |                                  |    |
| SHEET PATH<br>/                        | GIT HASH<br>9521b57  | DRAWING No                       | A3 |
| FILENAME<br>Input-Protection.kicad_sch | VARIANT<br>DRAFT   | REVISION + (Unreleased)<br>SHEET |    |
|  |  | 1 OF 4                           |    |

[2] BLOCK DIAGRAM



TARGET SPECIFICATIONS:

INPUT VOLTAGE: -50 to +50 V  
OUTPUT VOLTAGE: +12 to +17 V  
Spec 3 ?  
Spec 4 ?

|                                     |  |   |    |
|-------------------------------------|--|---|----|
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| DRN<br>2025-01-12 R. HICKS          |  |   |    |
| CHK                                 |  |   |    |
| ENG APP                             | Input Protection   |   |    |
| MFR APP                             |  |   |    |
| SHEET PATH<br>/Block Diagram/       | GIT HASH<br>9521b57  | DRAWING No<br>BLOCK DIAGRAM             | A3 |
| FILENAME<br>Block Diagram.kicad_sch | VARIANT<br>DRAFT   | REVISION + (Unreleased) SHEET<br>2 OF 4 |    |

# [3] SCHEMATIC

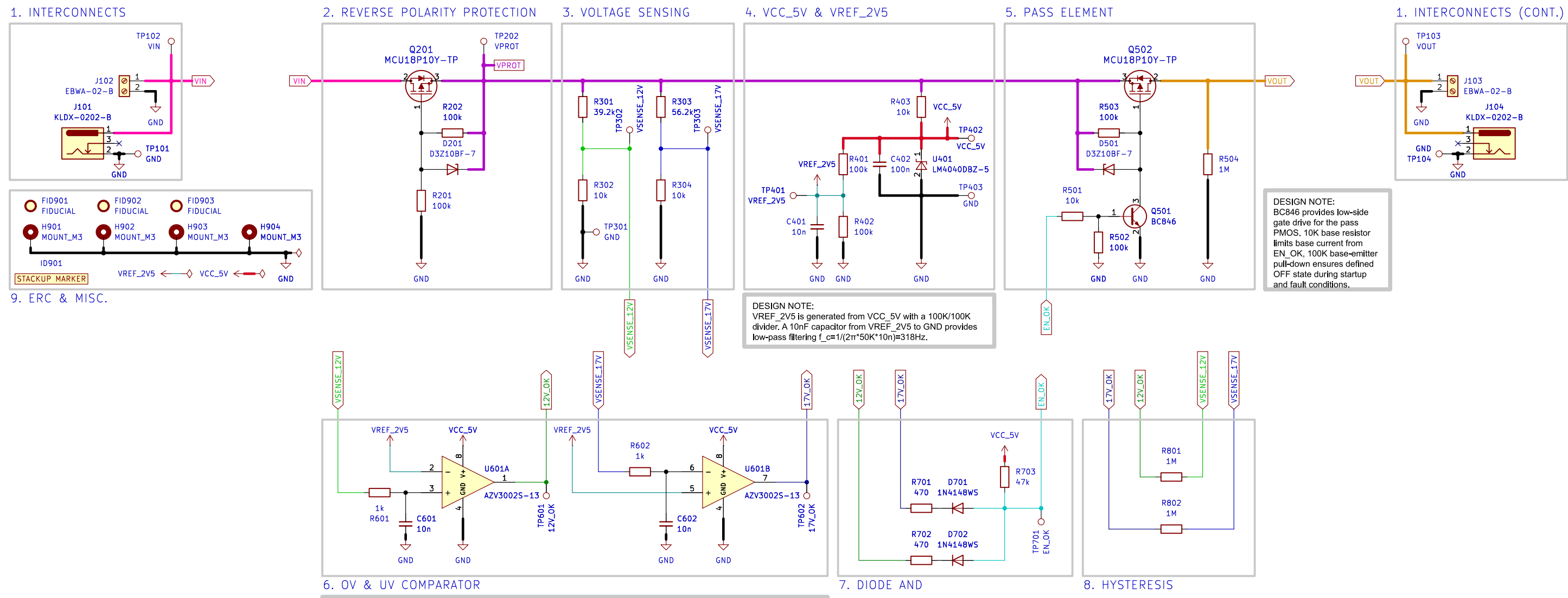
DESIGN NOTE:  
This PMOSFET is acting as an ideal diode [1].

10V zener from Gate to Source to limit VGS <= 10V under all VIN and transient conditions to protect PMOSFET. 100K Gate to Source resistor to not allow floating Gate. 100K Gate pulldown resistor so Gate is off and not affected by leakage or capacitive coupling when VIN removed or reversed.


DESIGN NOTE:  
 $V_{SENSE} = V_{PROT} \cdot R_{BOT} / (R_{TOP} + R_{BOT})$   
We are comparing with 2V5 VREF,  $V_{TRIP} = 2.5 \cdot (R_{TOP} + R_{BOT}) / R_{BOT}$ . We'll pick  $R_{BOT} = 10k$  for stiffness which leaves:  
 $R_{TOP} = 2000 \cdot (2 \cdot V_{TRIP} - 5)$ .  
For 12V,  $R_{TOP} = 38k$ . For 17V,  $R_{TOP} = 58k$ .

DESIGN NOTE:  
Per TI [2] choose Rs such that  $IR_{MIN} < IR < IR_{MAX}$  ( $IR_{MAX} = 15mA$ ), accounting for VIN range and load. With  $V_{IN\_MIN} = 12V$ ,  $V_{IN\_MAX} = 50V$ ,  $V_{OUT} = 5V$ ,  $IR_{MIN} = 75\mu A$  and  $I_{LOAD\_MAX} = (2.5V \text{ divider}) + (I_{EN\_OK} \text{ pull-up}) + I_q(AZV3002) \approx 250\mu A + 50\mu A + 9\mu A$ ,  $R_{s\_MAX} = (V_{IN\_MIN} - V_{OUT}) / (I_{LOAD\_MAX} + IR_{MIN}) = 18k$ ,  $R_{s\_MIN} = (V_{IN\_MAX} - V_{OUT}) / IR_{MAX} = 3k$ .  $R_s = 10k$  is selected to guarantee regulation at 12V & limit shunt current at 50V.

DESIGN NOTE:  
The pass PMOSFET is used as a high-side load disconnect controlled by the window comparator logic. When EN\_OK is high, the Gate is pulled low via the NPN driver, turning the device on and allowing VOUT to track VPROT with a small RDS(on) drop. When EN\_OK is low, the Gate is released and pulled toward Source, fully turning the device off and isolating the load. 1Meg output resistor to ground prevents floating Drain.




DESIGN NOTE:

|                                 |  |                       |   |
|---------------------------------|--|-----------------------|---|
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| DRN<br>2025-01-12 R. HICKS      |  |                       |   |
| CHK                             | Input Protection   |                       |   |
| ENG APP                         |  |                       |   |
| MFR APP                         | SCHEMATIC  |                       |   |
| SHEET PATH<br>/Schematic/       |  |                       |   |
| FILENAME<br>Schematic.kicad_sch | VARIANT<br>DRAFT   | DRAWING No<br>9521b57 | REVISION + (Unreleased) SHEET<br>3 OF 4 |

[1] <https://www.ti.com/lit/an/slva57b/slva57b.pdf?ts=1770319054914>  
[2] <https://www.ti.com/lit/ds/symlink/lm4040-n.pdf?ts=1752678691365>

# [4] REVISION HISTORY

|            |                            |
|------------|----------------------------|
| PROJECT    | Assignment 1               |
| DRN        | 2025-01-12 R. HICKS        |
| CHK        |                            |
| ENG APP    |                            |
| MFR APP    |                            |
| SHEET PATH | /Revision History/         |
| FILENAME   | Revision History.kicad_sch |

|  |                  |                         |
|--|------------------|-------------------------|
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| Input Protection   |                  |                         |
| GIT HASH   | DRAWING No       | A4                      |
| 9521b57  | REVISION HISTORY |                         |
| VARIANT  | DRAFT            | REVISION + (Unreleased) |
|  |                  | SHEET 4 OF 4            |