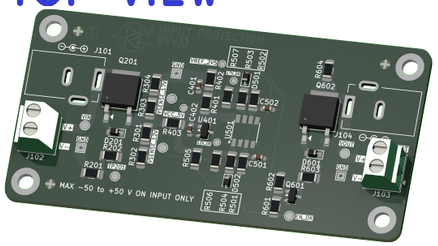
INPUT PROTECTION

Variant: PRELIMINARY

2026-02-09

Rev + (Unreleased)

TOP VIEW



BOTTOM VIEW

NOTES

Comment

Not fitted components are marked as X

DRAFT – Very early stage of schematic, ignore details.
PRELIMINARY – Close to final schematic.
CHECKED – There shouldn't be any mistakes. Contact the engineer if found.
RELEASED – A board with this schematic has been sent to production.

DESIGN CONSIDERATIONS

DESIGN NOTE: Example text for informational design notes.

DESIGN NOTE: Example text for debug notes.

DESIGN NOTE: Example text for cautionary design notes.

DESIGN NOTE: Example text for critical design notes.

LAYOUT NOTE: Example text for critical layout guidelines.

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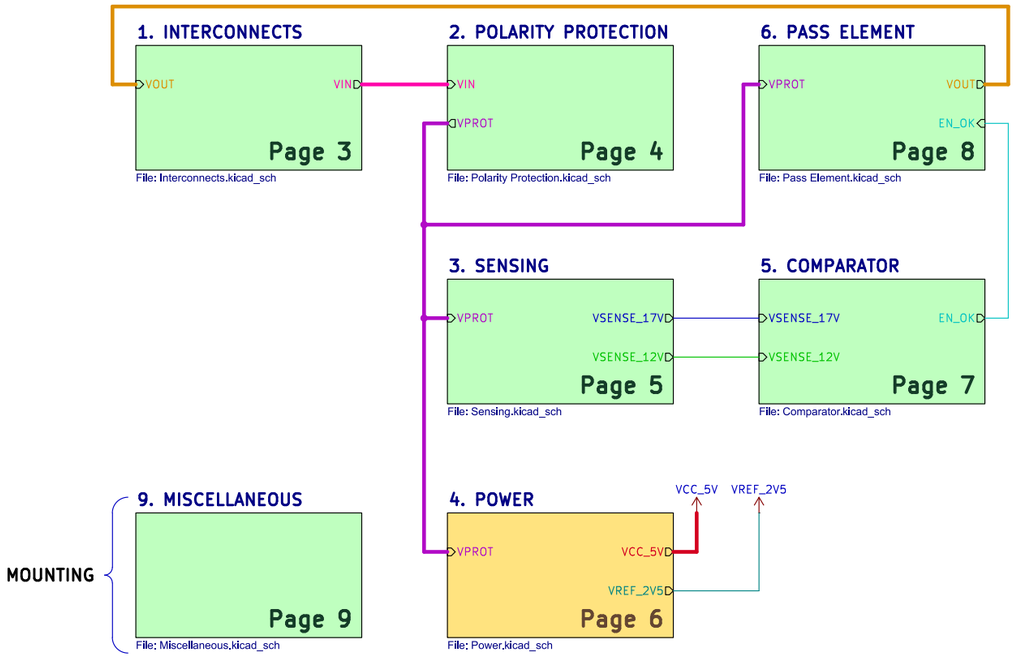
CHK			
ENG APP	INPUT PROTECTION		
MFR APP			
SHEET PATH /	GIT HASH 3eaf265	DRAWING No	A3
FILENAME Input-Protection.kicad_sch	VARIANT PRELIMINARY	REVISION + (Unreleased)	SHEET 1 OF 10

[2] ARCHITECTURE



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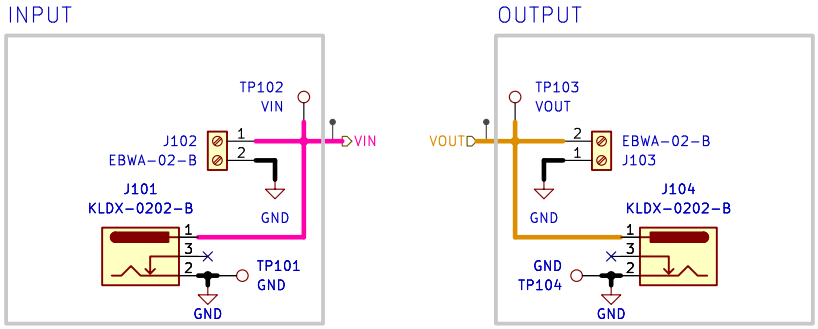
ENG APP	INPUT PROTECTION		
MFR APP			
SHEET PATH /ARCHITECTURE/	GIT HASH 3eaf265	DRAWING No ARCHITECTURE	A3
FILENAME Project Architecture.kicad_sch	VARIANT PRELIMINARY	REVISION + (Unreleased)	SHEET 2 OF 10

[3] 1. INTERCONNECTS



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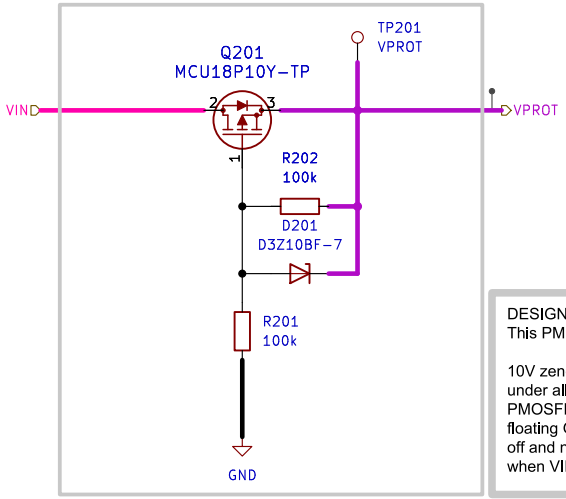
MFR APP			
SHEET PATH /ARCHITECTURE/1. INTERCONNECTS/	GIT HASH 3eaf265	DRAWING No 1. INTERCONNECTS	A4
FILENAME Interconnects.kicad_sch	VARIANT PRELIMINARY	REVISION + (Unreleased)	SHEET 3 OF 10

[4] 2. POLARITY PROTECTION



DESIGN NOTE:
This PMOSFET is acting as an ideal diode [1].

10V zener from Gate to Source to limit VGS <= 10V under all VIN and transient conditions to protect PMOSFET. 100K Gate to Source resistor to not allow floating Gate. 100K Gate pulldown resistor so Gate is off and not affected by leakage or capacitive coupling when VIN removed or reversed.

[1] https://www.ti.com/lit/an/slvae57b/slvae57b.pdf?ts=1770319054914

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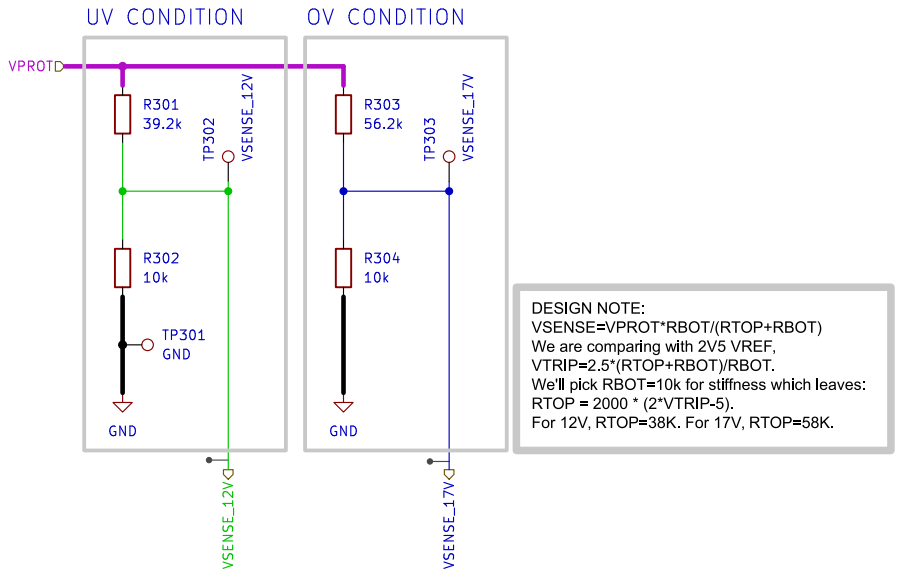
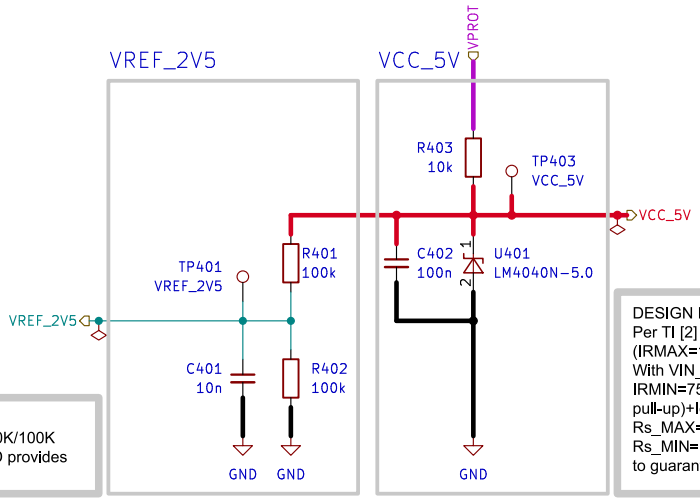
DRN 2025-01-12 R. HICKS			
CHK			
ENG APP	INPUT PROTECTION		
MFR APP			
SHEET PATH /ARCHITECTURE/2. POLARITY PROTECTION/	GIT HASH 3ea2265	DRAWING No POLARITY PROTECTION	A4
FILENAME Polarity Protection.kicad_sch	VARIANT PRELIMINARY	REVISION + (Unreleased)	SHEET 4 OF 10

[5] 3. SENSING



PROJECT ASSIGNMENT 1	Ryan Dynamics		
DRN 2025-01-12 R. HICKS			
CHK			
ENG APP	INPUT PROTECTION		
MFR APP			
SHEET PATH /ARCHITECTURE/3. SENSING/	GIT HASH 3eaf265	DRAWING No 3. SENSING	A4
FILENAME Sensing.kicad_sch	VARIANT PRELIMINARY	REVISION + (Unreleased)	SHEET 5 OF 10

[6] 4. POWER



DESIGN NOTE:
VREF_2V5 is generated from VCC_5V with a 100K/100K divider. A 10nF capacitor from VREF_2V5 to GND provides low-pass filtering f_c=1/(2π*50K*10n)=318Hz.

DESIGN NOTE:
Per TI [2] choose Rs such that IRMIN<IR<IRMAX (IRMAX=15mA), accounting for VIN range and load. With VIN_MIN=12V, VIN_MAX=50V, VOUT=5 V, IRMIN=75µA and ILOAD_MAX≈I(2.5 V divider)+I(EN_OK pull-up)+Iq(AZV3002)≈250µA+50µA+9µA, Rs_MAX=(VIN_MIN−VOUT)/(ILOAD_MAX+IRMIN)≈18K Rs_MIN=(VIN_MAX−VOUT)/IRMAX≈3K. Rs=10K is selected to guarantee regulation at 12V & limit shunt current at 50V.

[2] https://www.ti.com/lit/ds/symlink/lm4040-n.pdf?ts=1752678691365

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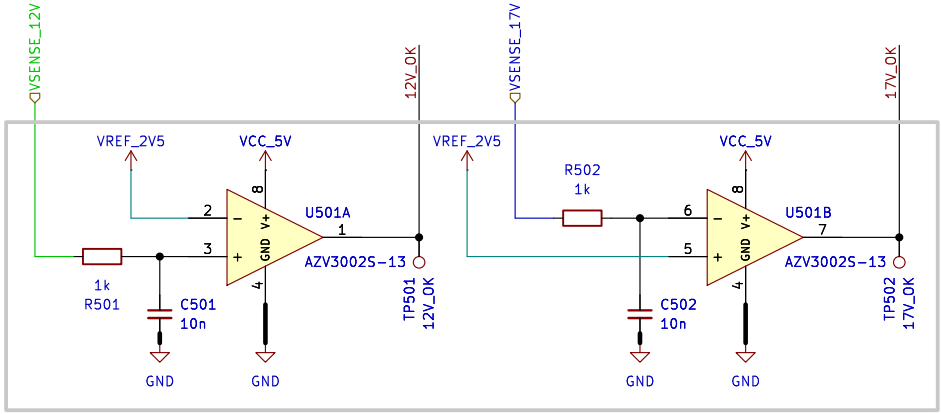
ENG APP	INPUT PROTECTION		
MFR APP			
SHEET PATH /ARCHITECTURE/4. POWER/	GIT HASH 3eaf265	DRAWING No 4. POWER	A4
FILENAME Power.kicad_sch	VARIANT PRELIMINARY	REVISION + (Unreleased)	SHEET 6 OF 10

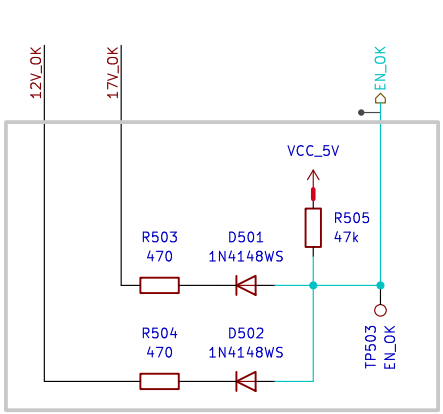
[7] 5. COMPARATOR



OV & UV COMPARATOR

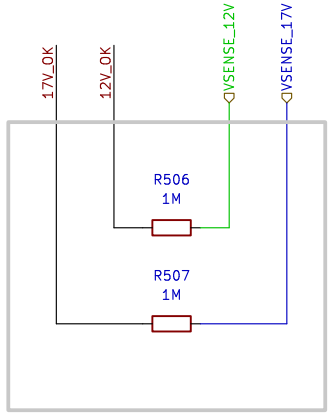
DESIGN NOTE:
The AZV3002S-13 dual comparator is used to implement the 12-17 V window detector.
Each comparator compares a scaled VPROT sense voltage (VSENSE) against VREF_2V5 to generate 12V_OK and 17V_OK signals.
The device is selected for its low supply current (10uA worst) and rail-to-rail input.

DESIGN NOTE:
A simple low pass filter is placed on the VSENSE inputs of the comparators to smooth transitions and reduce chatter near the transition points. f_c=1/(2π*1K*10n)=16Hz.



DIODE AND

DESIGN NOTE:
EN_OK is generated using diode logic AND combining the 12V_OK and 17V_OK. A pull-up resistor biases EN_OK high, while either comparator output can clamp the node low through its diode, ensuring the pass MOSFET is enabled only when both voltage conditions are satisfied.
Series resistors limit output interaction and improve stability with push-pull comparator outputs.



HYSTERESIS

DESIGN NOTE:
1M feedback resistor from comparator output to sense input provides external hysteresis to prevent chatter near the 12 V and 17 V thresholds.
With divider RTH≈RTOP||RBOT≈8K and a 5 V output swing, hysteresis at VSENSE is about ΔVSENSE≈5*RTH/RHYS≈40mV, or ~0.2-0.3 V seen at VPROT.

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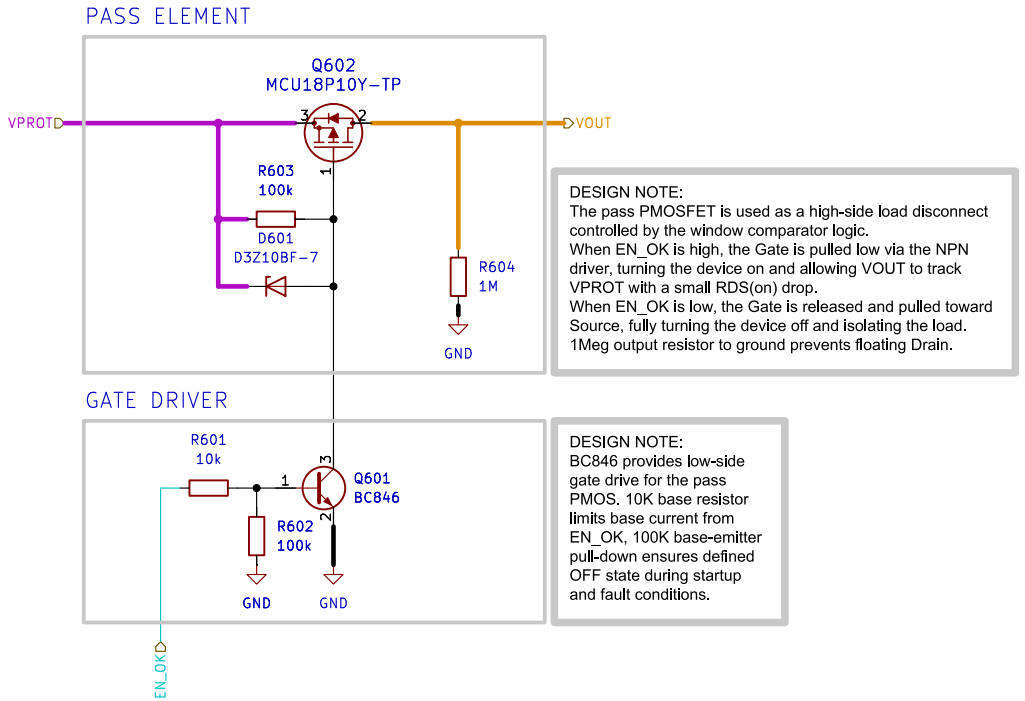
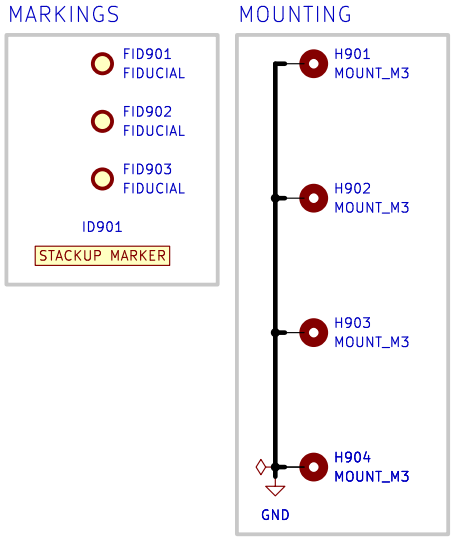
MFR APP			
SHEET PATH /ARCHITECTURE/5. COMPARATOR/	GIT HASH 3eaf265	DRAWING No 5. COMPARATOR	A4
FILENAME Comparator.kicad_sch	VARIANT PRELIMINARY	REVISION + (Unreleased)	SHEET 7 OF 10

[8] 6. PASS ELEMENT



PROJECT ASSIGNMENT 1	Ryan Dynamics		
DRN 2025-01-12 R. HICKS			
CHK			
ENG APP	INPUT PROTECTION		
MFR APP			
SHEET PATH /ARCHITECTURE/6. PASS ELEMENT/	GIT HASH 3eaf265	DRAWING No 6. PASS ELEMENT	A4
FILENAME Pass Element.kicad_sch	VARIANT PRELIMINARY	REVISION + (Unreleased)	SHEET 8 OF 10

[9] 9. MISCELLANEOUS



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ENG APP	INPUT PROTECTION		
MFR APP			
SHEET PATH /ARCHITECTURE/9. MISCELLANEOUS/	GIT HASH 3eaf265	DRAWING No 9. MISCELLANEOUS	A4
FILENAME Miscellaneous.kicad_sch	VARIANT PRELIMINARY	REVISION + (Unreleased) SHEET 9 OF 10	

[10] REVISION HISTORY

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CHK			
ENG APP	INPUT PROTECTION		
MFR APP			
SHEET PATH /REVISION HISTORY/	GIT HASH 3eaf265	DRAWING No REVISION HISTORY	A4
FILENAME Revision History.kicad_sch	VARIANT PRELIMINARY	REVISION + (Unreleased) SHEET 10 OF 10	