

INPUT PROTECTION

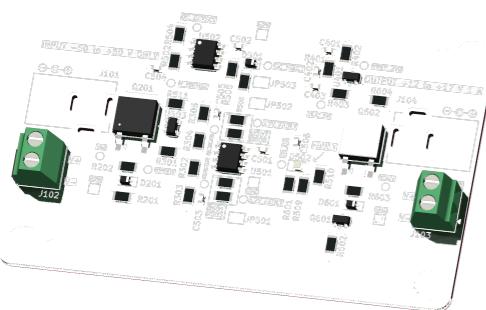
Variant: CHECKED

2026-02-10

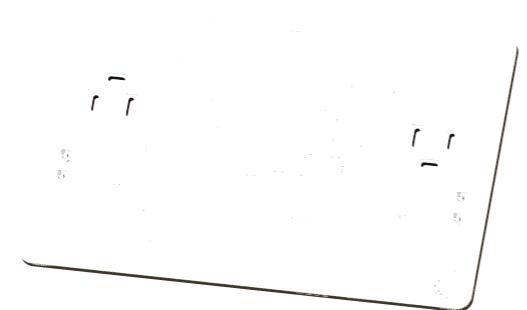
Rev + (Unreleased)

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TOP VIEW



BOTTOM VIEW



NOTES

Comment

Not fitted components are marked as

DRAFT – Very early stage of schematic, ignore details.

PRELIMINARY – Close to final schematic.

CHECKED – There shouldn't be any mistakes. Contact the engineer if found.

RELEASED – A board with this schematic has been sent to production.

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for debug notes.

DESIGN NOTE:
Example text for cautionary design notes.

DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

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SHEET PATH

/

FILENAME

Input-Protection.kicad_sch

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GIT HASH

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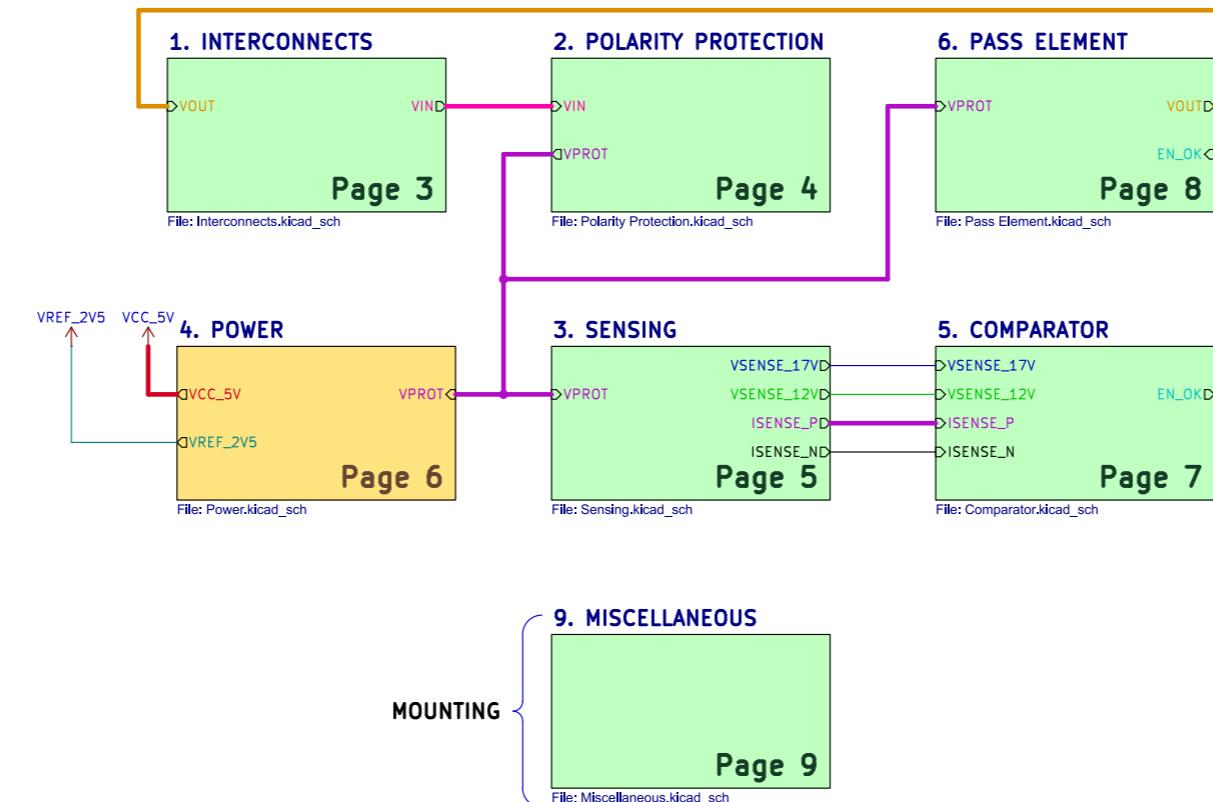
3eaf265

DRAWING No

A3

1 OF 10

[2] ARCHITECTURE



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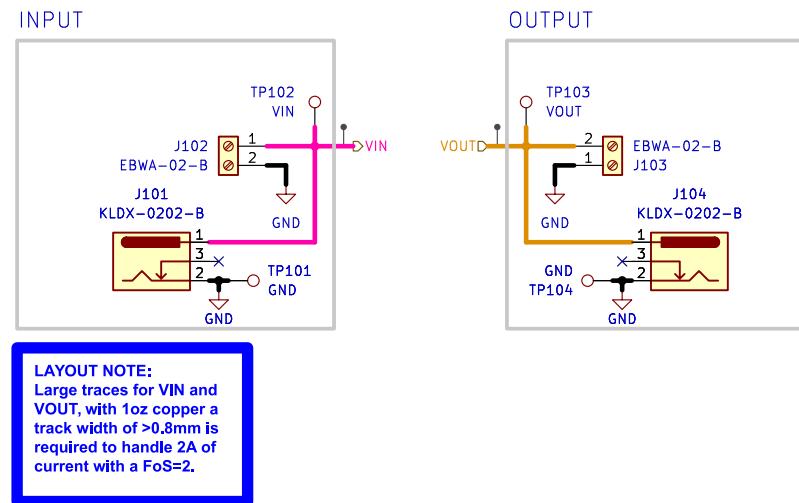


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/ARCHITECTURE/	3eaf265	ARCHITECTURE			
FILENAME	VARIANT	CHECKED	REVISION + (Unreleased)	SHEET	2 OF 10
Project Architecture.kicad_sch					

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[3] 1. INTERCONNECTS



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1. INTERCONNECTS

A4

FILENAME Interconnects.kicad_sch

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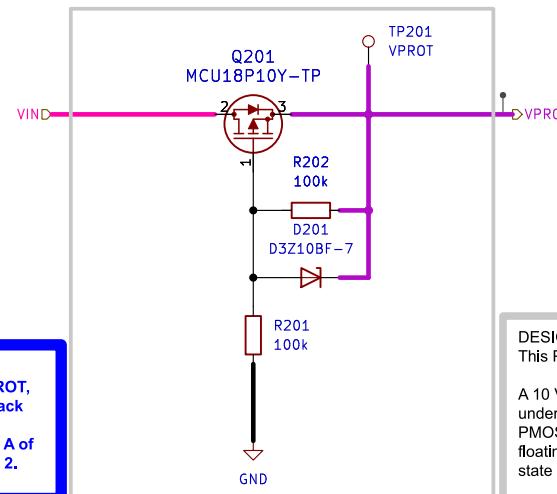
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[4] 2. POLARITY PROTECTION



DESIGN NOTE:
This PMOS is acting as an ideal diode [1].

A 10 V zener from gate to source limits $V_{GS} \leq 10$ V under all VIN and transient conditions to protect the PMOS. A 100k gate to source resistor stops the gate floating. A 100k gate pulldown resistor sets default state to OFF when no voltage at VIN is present.

[1] <https://www.ti.com/lit/an/slvae57b/slvae57b.pdf?ts=1770319054914>

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FILENAME Polarity Protection.kicad_sch

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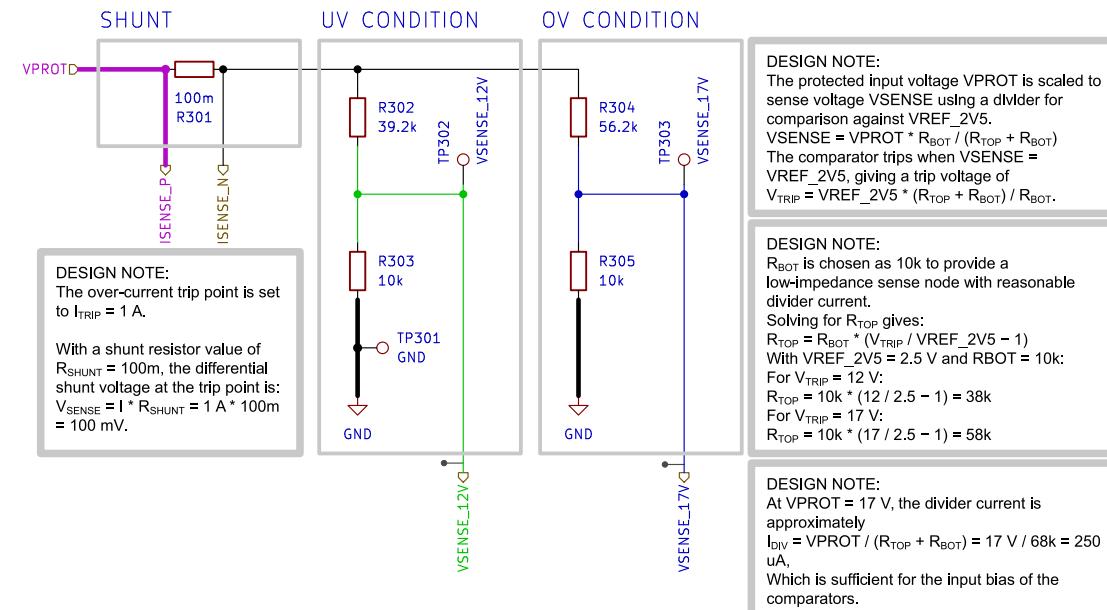
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[5] 3. SENSING



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FILENAME Sensing.kicad_sch

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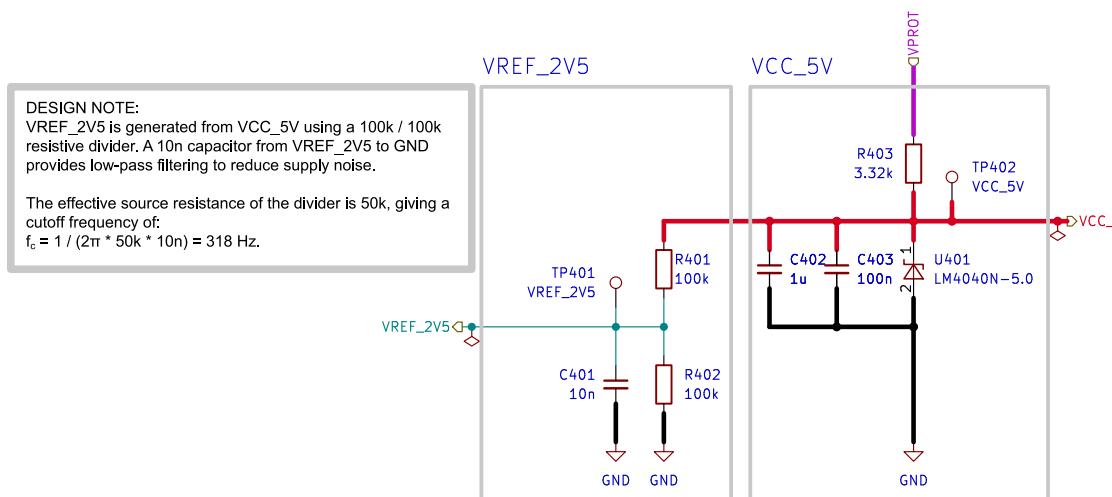
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[6] 4. POWER



DESIGN NOTE:
Per TI [2], choose the series resistor R_s such that $I_{RMIN} < I_R < I_{RMAX}$ across the full input range, while supplying the worst-case load current from VCC_5V.

Assume:
 $V_{IN,MIN} = 12 \text{ V}$, $V_{IN,MAX} = 50 \text{ V}$, $V_{OUT} = 5 \text{ V}$
 $I_{RMAX} = 15 \text{ mA}$, $I_{RMIN} = 75 \mu\text{A}$
Worst-case VCC_5V load current with EN_OK high is estimated as:
 $I_{LOAD,MAX} = I_{DIV,2V5} + I_{Q,LM393} + I_{Q,INA169} + I_{B,NPN}$
where:
 $I_{DIV,2V5} = 5 \text{ V} / (100k + 100k) = 25 \mu\text{A}$
 $I_{Q,LM393} = 2 * 600 \mu\text{A} = 1.2 \text{ mA}$ (two LM393 packages)
 $I_{Q,INA169} = 125 \mu\text{A}$
 $I_{B,NPN} = (5 \text{ V} - 0.7 \text{ V}) / 10k = 430 \mu\text{A}$
Note:
The fault LED current is drawn only when EN_OK is low and is therefore not included in the EN_OK-high load budget.
Thus:
 $I_{LOAD,MAX} = 25 \mu\text{A} + 1.2 \text{ mA} + 125 \mu\text{A} + 430 \mu\text{A} = 1.78 \text{ mA}$
This gives:
 $R_s,MAX = (V_{IN,MIN} - V_{OUT}) / (I_{LOAD,MAX} + I_{RMIN}) = 7 \text{ V} / (1.78 \text{ mA} + 0.075 \text{ mA}) = 3.8k$
 $R_s,MIN = (V_{IN,MAX} - V_{OUT}) / I_{RMAX} = 45 \text{ V} / 15 \text{ mA} = 3k$
 R_s (R403) is selected as 3.32k to ensure regulation at $V_{IN,MIN}$ while limiting shunt current at $V_{IN,MAX}$.

[2] <https://www.ti.com/lit/ds/symlink/lm4040-n.pdf?ts=1752678691365>

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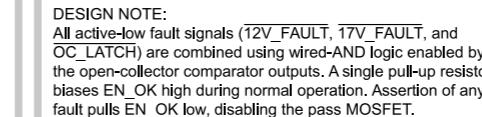
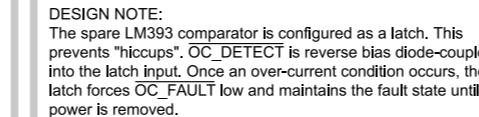
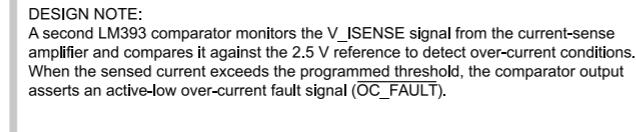
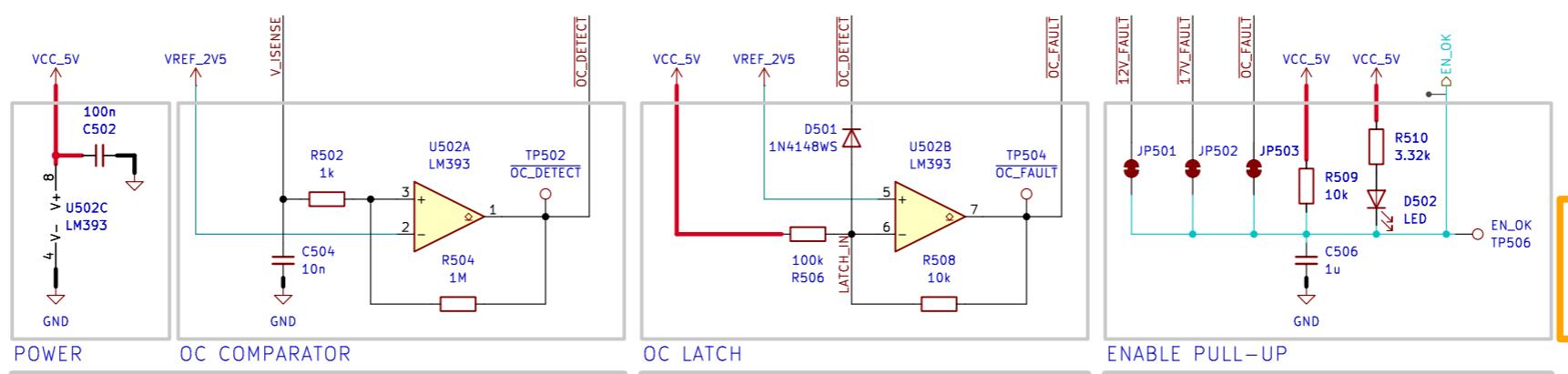
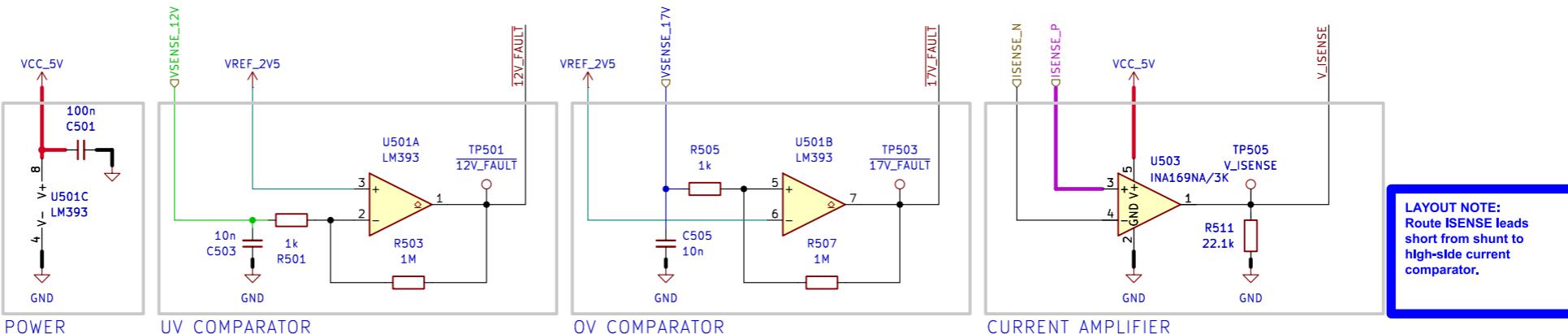
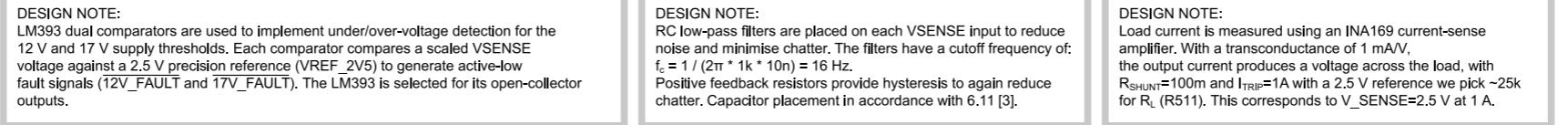
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/ARCHITECTURE/4. POWER/	3eaf265			
FILENAME	VARIANT	CHECKED	REVISION + (Unreleased)	SHEET
Power.kicad_sch				6 OF 10

[7] 5. COMPARATOR

[3] <https://www.ti.com/lit/an/sn0aa35f/sn0aa35f.pdf?ts=1770697404856>



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VARIANT	REVISION + (Unreleased)
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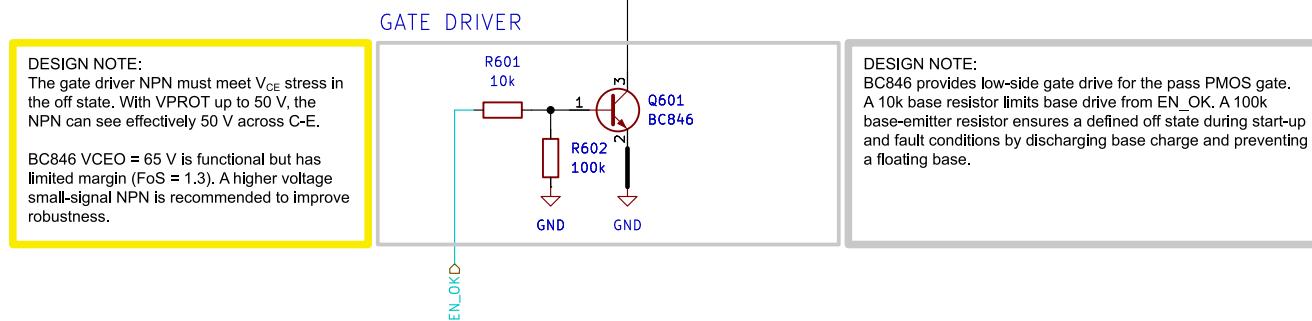
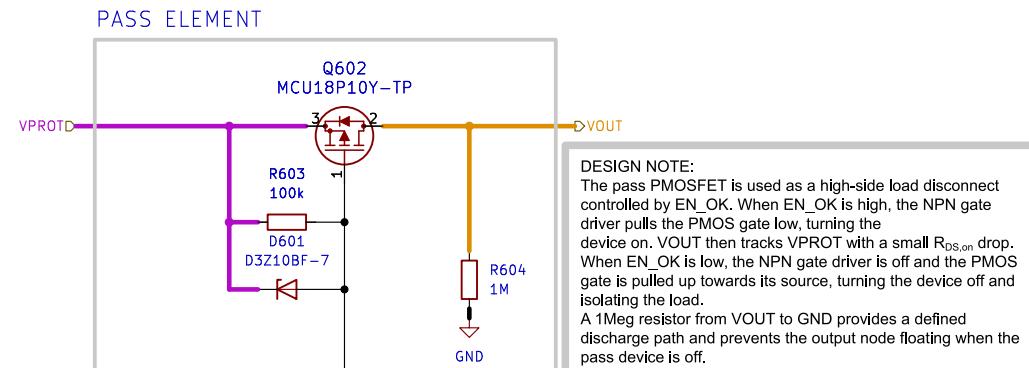


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[8] 6. PASS ELEMENT



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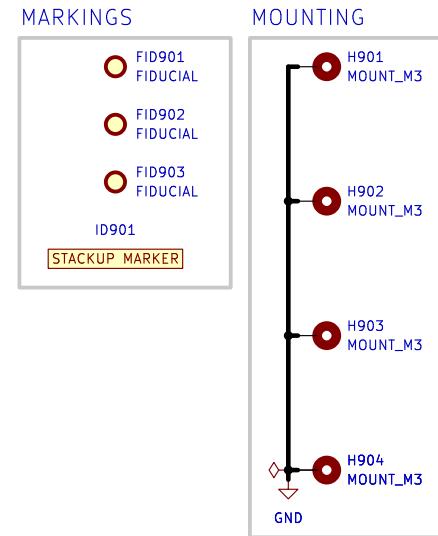
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FILENAME	Pass Element.kicad_sch
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[9] 9. MISCELLANEOUS



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9. MISCELLANEOUS

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FILENAME Miscellaneous.kicad_sch

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[10] REVISION HISTORY

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