

Input Protection

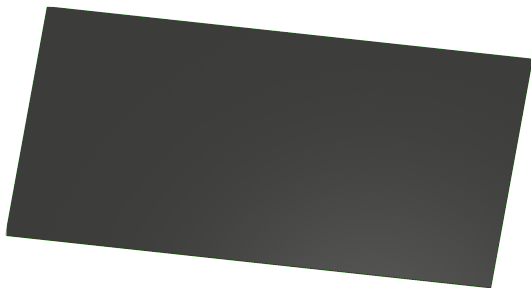
Variant: DRAFT

2026-02-07

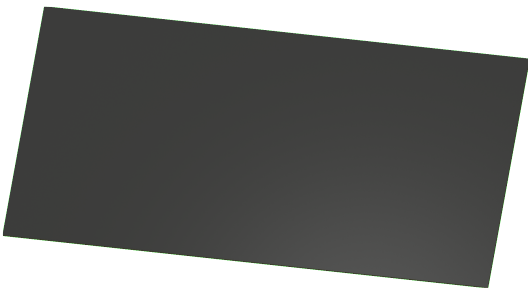
Rev + (Unreleased)

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TOP VIEW



BOTTOM VIEW



NOTES

Comment

Not fitted components are marked as **X**

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There shouldn't be any mistakes. Contact the engineer if you find any.

RELEASED - A board with this schematic has been sent to production.

Date: 07-Feb-2026

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for debug notes.

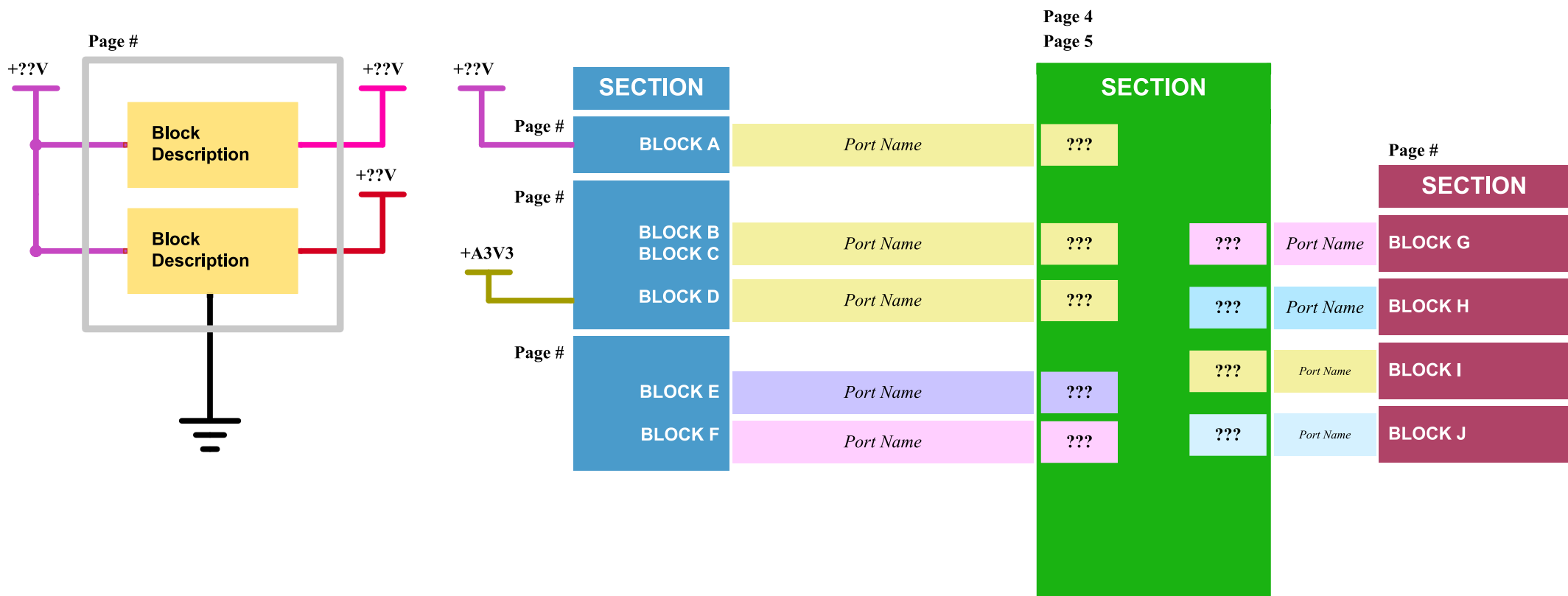
DESIGN NOTE:
Example text for cautionary design notes.

DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

	Comments:	Company: University of Newcastle		Variant: DRAFT	Git Hash: a736dc4
	Sheet Title:	Board Name: Input Protection		Project Name: Assignment 1	
	Sheet Path: /	File Name: Input-Protection.kicad_sch	Designer: R. HICKS	Date: 2025-01-12	Revision: + (Unreleased)
		Reviewer:	Size: A3	Sheet: 1 of 4	

[2] BLOCK DIAGRAM

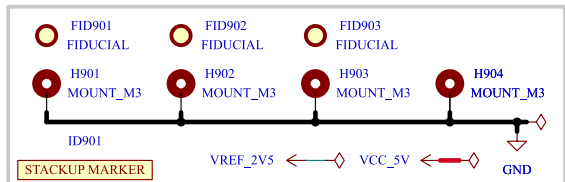
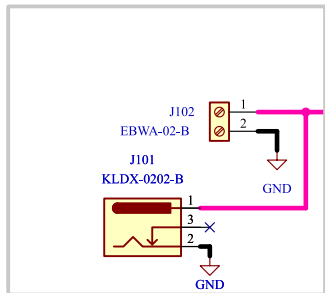


TARGET SPECIFICATIONS:	
INPUT VOLTAGE:	-50 - +50 V
OUTPUT VOLTAGE:	??
Spec 3	??
Spec 4	??

	Comments:		Company: University of Newcastle		Variant: DRAFT	Git Hash: a736dc4
			Board Name: Input Protection		Project Name: Assignment 1	
	Sheet Title: BLOCK DIAGRAM	File Name: Block Diagram.kicad_sch	Designer: R. HICKS	Date: 2025-01-12	Revision: + (Unreleased)	
	Sheet Path: /Block Diagram/		Reviewer:	Size: A3	Sheet: 2 of 4	

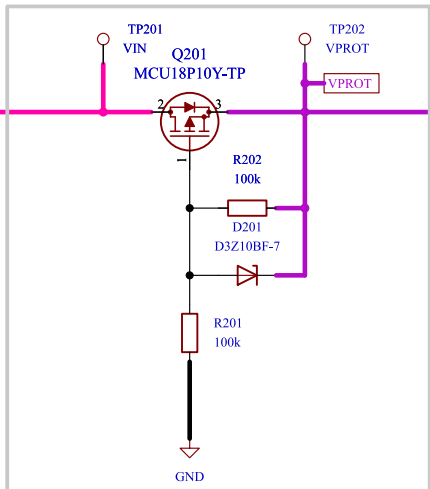
[3] Schematic

1. INTERCONNECTS

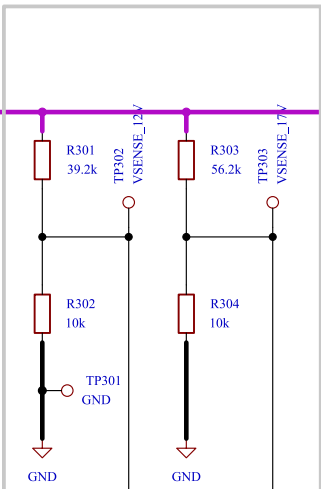


9. ERC & MISC.

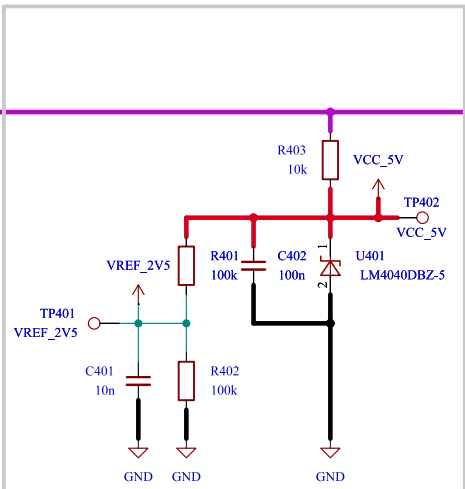
2. REVERSE POLARITY PROTECTION



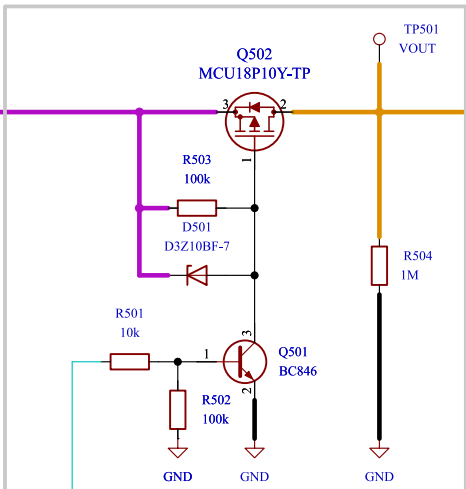
3. VOLTAGE SENSING



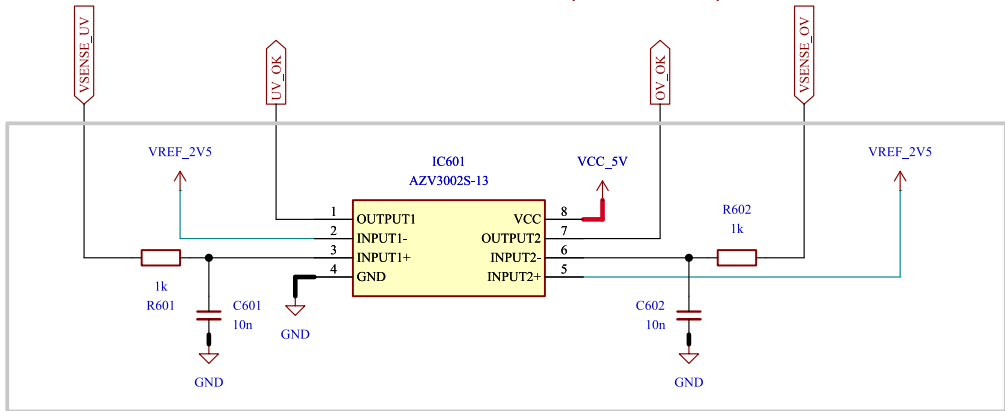
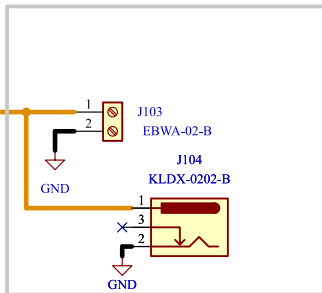
4. 5V & 2V5 VREF



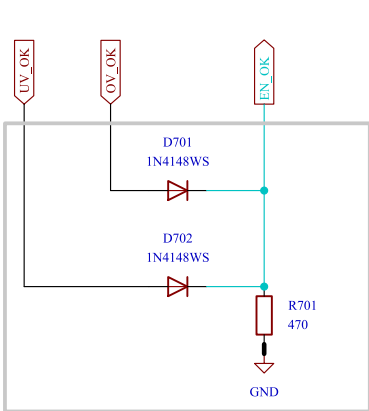
5. PASS ELEMENT



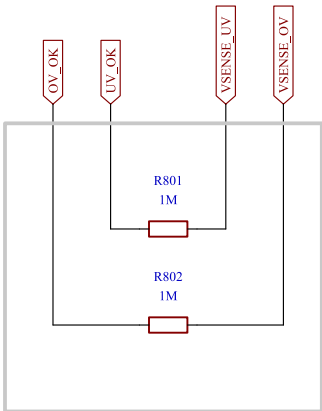
1. INTERCONNECTS (CONT.)



6. OV & UV COMPARATOR



7. SUMMING



8. HYSTERESIS

	Comments:		Company:		Variant:	Git Hash:
			University of Newcastle		DRAFT	a736dc4
			Board Name:		Project Name:	
			Input Protection		Assignment 1	
Sheet Title:	Schematic		File Name:	Schematic.kicad_sch	Designer:	R. HICKS
Sheet Path:	/Schematic/		Reviewer:		Date:	2025-01-12
					Revision:	+
					Size:	A3
					Sheet:	3 of 4

[4] REVISION HISTORY

	Comments:	Company: University of Newcastle		Variant: DRAFT	Git Hash: a736dc4
		Board Name: Input Protection		Project Name: Assignment 1	
	Sheet Title: REVISION HISTORY	File Name: Revision History.kicad_sch	Designer: R. HICKS	Date: 2025-01-12	Revision: + (Unreleased)
	Sheet Path: /Revision History/		Reviewer:	Size: A4	Sheet: 4 of 4