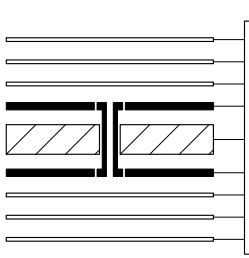
INPUT PROTECTION Fabrication DOCUMENT

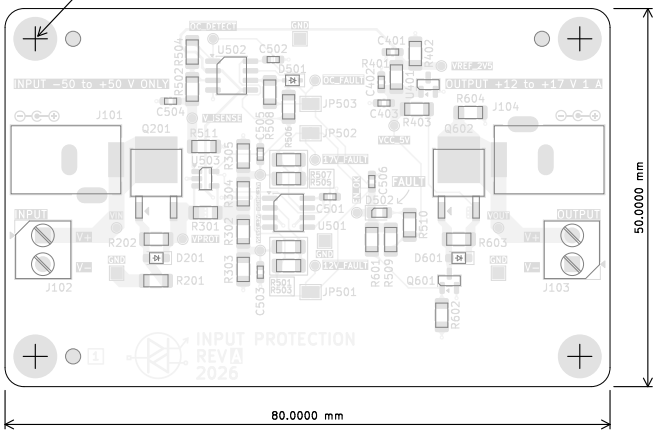
Layer Stack Legend



Material	Layer	Thickness	Dielectric	Type	Gerber
	F.Paste			Paste Mask	
	F.Silkscreen		Direct Printing	Legend	GBR
	F.Mask	0,02mm	Solder Resist	Solder Mask	GBR
Copper	**L1 (Sig, PWR)**	**0.035mm (1.00oz)**		**Signal**	**GBR**
Core		1.48mm	FR4_7628	Dielectric	
Copper	**L2 (Sig, GND)**	**0.035mm (1.00oz)**		**Plane**	**GBR**
	B.Mask	0,02mm	Solder Resist	Solder Mask	GBR
	B.Silkscreen		Direct Printing	Legend	GBR
	B.Paste			Paste Mask	

Total thickness: 1.59mm
Note: external layer thicknesses are specified after plating

Top Fabrication (Scale 1:1)



FABRICATION NOTES (UNLESS OTHERWISE SPECIFIED)

1) FABRICATE PER IPC-6012A CLASS 2.
2) OUTLINE DEFINED IN SEPARATE GERBER FILE WITH "Edge_Cuts.GBR" SUFFIX.
3) SEE SEPARATE DRILL FILES WITH ".DRL" SUFFIX FOR HOLE LOCATIONS.
4) SURFACE FINISH: HAL LEAD-FREE
5) SOLDERMASK ON BOTH SIDES OF THE BOARD SHALL BE LPI, COLOR GREEN.
6) SILK SCREEN LEGEND TO BE APPLIED PER LAYER STACKUP USING WHITE NON-CONDUCTIVE EPOXY INK.
7) VENDOR SHOULD FOLLOW ROHS COMPLIANT PROCESS AND Pb FREE FOR MANUFACTURING
8) PCB MATERIAL REQUIREMENTS:
   A. FLAMMABILITY RATING MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.
   B. Tg 170 C OR EQUIVALENT.
   C. EQUIVALENT MATERIAL SHALL BE RoHS COMPLIANT, HALOGEN FREE AND APPROVED BY RYAN DYNAMICS.
9) DESIGN GEOMETRY MINIMUM FEATURE SIZES:

BOARD SIZE	80.000 × 50.000 mm
BOARD THICKNESS	1.590 mm
TRACE WIDTH	0.200 mm
TRACE TO TRACE	-0.000 mm
MIN. HOLE (PTH)	0.250 mm
MIN. HOLE (NPTH)	N/A mm
ANNULAR RING	0.150 mm
COPPER TO HOLE	0.254 mm
COPPER TO EDGE	0.250 mm
HOLE TO HOLE	0.254 mm

All dimensions are in millimeters unless otherwise specified.

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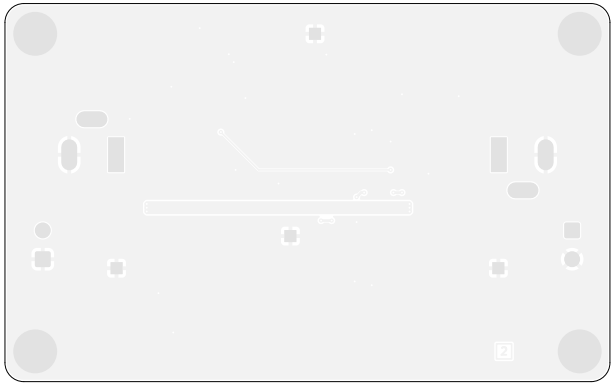
DRN 2024-04-13 R. HICKS	THIS DESIGN AND/OR DRAWING IS THE PROPERTY OF RYAN DYNAMICS AND SHALL NOTBE REPRODUCED WITHOUT AUTHORISATION.		
CHK			
ENG APP	INPUT PROTECTION		
MFR APP			
SHEET PATH	GIT HASH 3eaf265	DRAWING No Fabrication	A4
FILENAME Input-Protection.kicad_pcb	VARIANT CHECKED	REVISION + (Unreleased)	SHEET 1 OF 7

INPUT PROTECTION Fabrication DOCUMENT

Bottom Fabrication (Scale 1:1)



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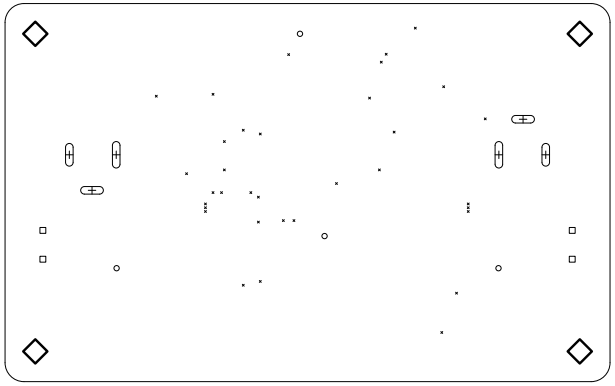
INPUT PROTECTION Fabrication DOCUMENT

Drill Table

Symbol	Count	Hole Size	Plated	Hole Shape	Drill Layer Pair	Hole Type
×	34	0.25mm (9.84mils)	PTH	Round	L1 (Sig, PWR) - L2 (Sig, GND)	Via
○	4	0.70mm (27.56mils)	PTH	Round	L1 (Sig, PWR) - L2 (Sig, GND)	Pad
+	6	1.00mm (39.37mils)	PTH	Slot	L1 (Sig, PWR) - L2 (Sig, GND)	Pad
□	4	1.10mm (43.31mils)	PTH	Round	L1 (Sig, PWR) - L2 (Sig, GND)	Pad
◇	4	3.20mm (125.98mils)	PTH	Round	L1 (Sig, PWR) - L2 (Sig, GND)	Pad
	Total 52					

Drill Drawing L1 – L2 (Scale 1:1)



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DRN 2024-04-13 R. HICKS			
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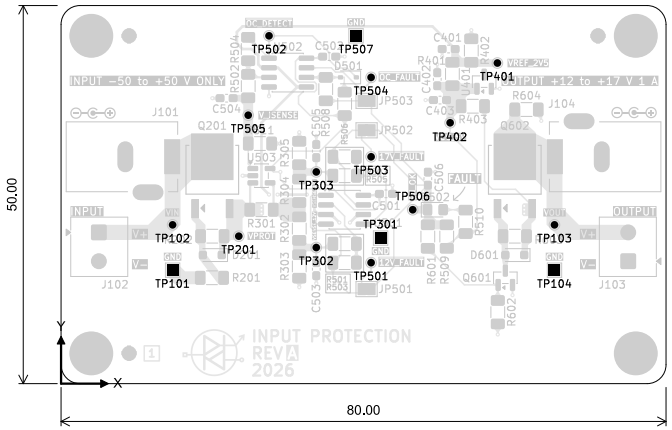
SHEET PATH	GIT HASH 3eaf265	DRAWING No Fabrication	A4
FILENAME Input-Protection.kicad_pcb	VARIANT CHECKED	REVISION + (Unreleased)	SHEET 3 OF 7

INPUT PROTECTION Fabrication DOCUMENT

Top Test Points (Scale 1:1)



Ref.	Net	X [mm]	Y [mm]
TP101	GND	14.75	15.00
TP102	VIN	14.75	21.00
TP103	VOUT	65.25	21.00
TP104	GND	65.25	15.00
TP201	VPROT	23.50	19.50
TP301	GND	42.25	19.25
TP302	VSENSE_12V	33.75	18.00
TP303	VSENSE_17V	33.75	28.00
TP401	VREF_2V5	57.70	42.40
TP402	VCC_5V	51.45	34.50
TP501	12V_FAULT	41.00	16.00
TP502	OC_DETECT	27.50	46.00
TP503	17V_FAULT	41.00	30.00
TP504	OC_FAULT	41.00	40.50
TP505	V_ISENSE	24.75	35.50
TP506	EN_OK	46.50	23.00
TP507	GND	39.00	46.00

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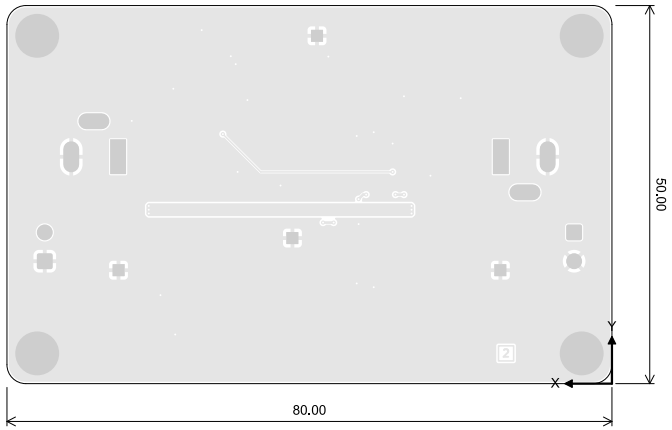
ENG APP	INPUT PROTECTION		
MFR APP			
SHEET PATH	GIT HASH 3eaf265	DRAWING No Fabrication	A4
FILENAME Input-Protection.kicad_pcb	VARIANT CHECKED	REVISION + (Unreleased)	SHEET 4 OF 7

INPUT PROTECTION Fabrication DOCUMENT

Ref.	Net	X [mm]	Y [mm]

Bottom Test Points (Scale 1:1)



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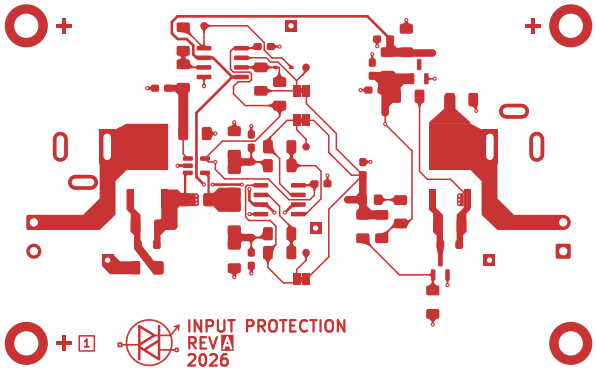
DRN 2024-04-13 R. HICKS			
CHK			
ENG APP	INPUT PROTECTION		
MFR APP			
SHEET PATH	GIT HASH 3eaf265	DRAWING No Fabrication	A4
FILENAME Input-Protection.kicad_pcb	VARIANT CHECKED	REVISION + (Unreleased)	SHEET 5 OF 7

INPUT PROTECTION Fabrication DOCUMENT

L1 (Sig, PWR) (Scale 1:1)



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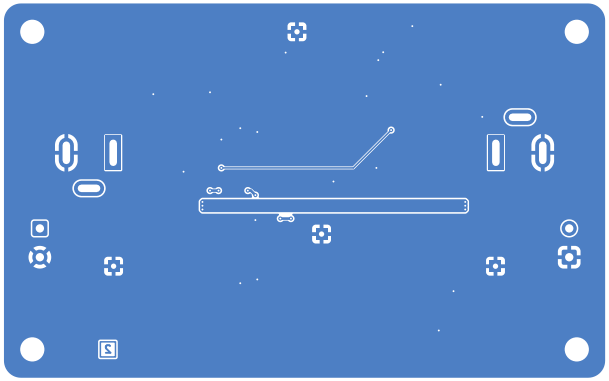
ENG APP	INPUT PROTECTION		
MFR APP			
SHEET PATH	GIT HASH 3eaf265	DRAWING No Fabrication	A4
FILENAME Input-Protection.kicad_pcb	VARIANT CHECKED	REVISION + (Unreleased)	SHEET 6 OF 7

INPUT PROTECTION Fabrication DOCUMENT

L2 (Sig, GND) (Scale 1:1)



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DRN 2024-04-13 R. HICKS			
CHK			
ENG APP	INPUT PROTECTION		
MFR APP			
SHEET PATH	GIT HASH 3eaf265	DRAWING No Fabrication	A4
FILENAME Input-Protection.kicad_pcb	VARIANT CHECKED	REVISION + (Unreleased)	SHEET 7 OF 7