

Input Protection

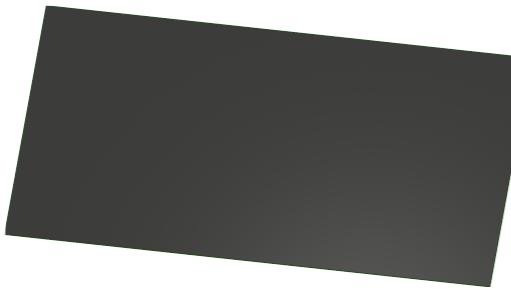
Variant: DRAFT

2026-02-06

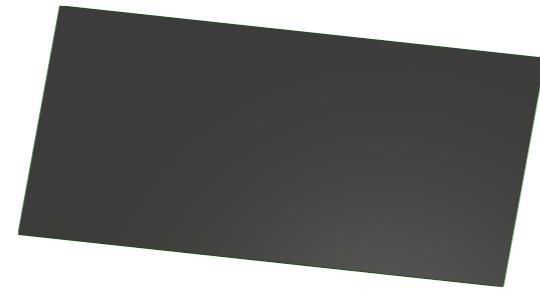
Rev + (Unreleased)

Page	Index	Page	Index	Page	Index	Page	Index
1	Cover Page	11	21	31
2	Block Diagram	12	22	32
3	Schematic	13	23	33
4	Revision History	14	24	34
5	15	25	35
6	16	26	36
7	17	27	37
8	18	28	38
9	19	29	39
10	20	30	40

TOP VIEW



BOTTOM VIEW



NOTES

Comment

Not fitted components are marked as

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There shouldn't be any mistakes. Contact the engineer if you find any.

RELEASED - A board with this schematic has been sent to production.

Date: 06-Feb-2026

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for debug notes.

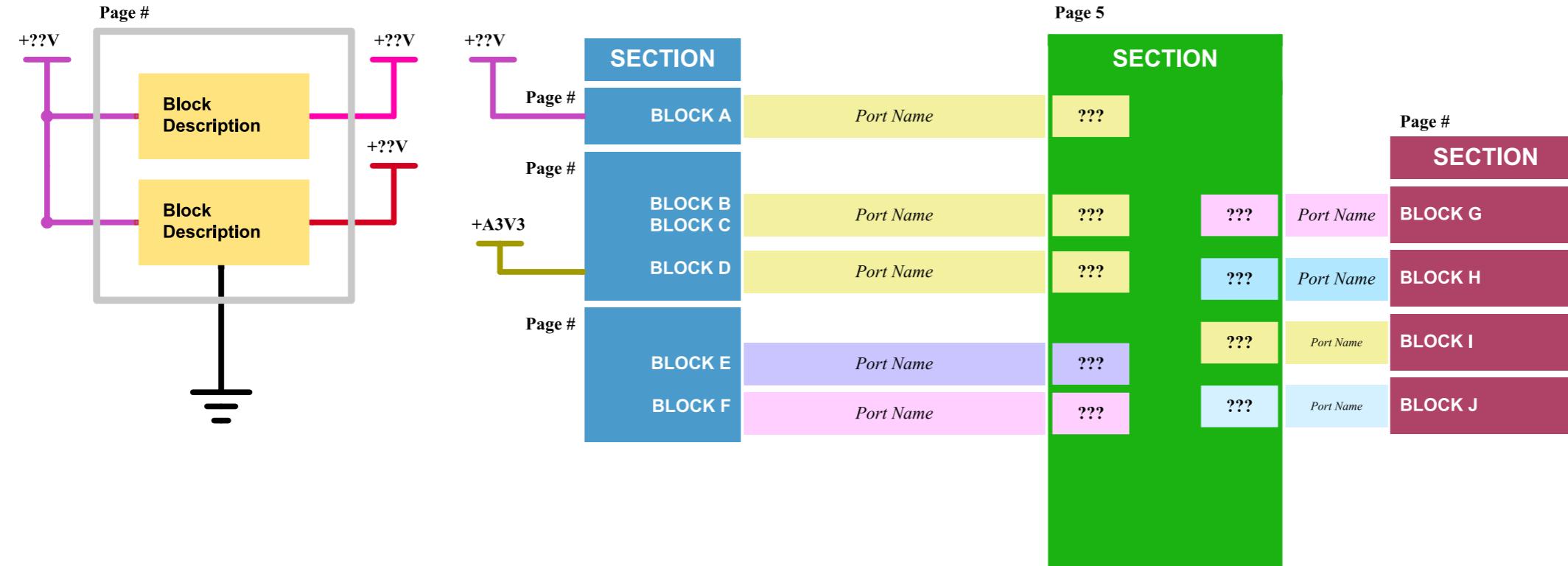
DESIGN NOTE:
Example text for cautionary design notes.

DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

	Comments:	Company: University of Newcastle	Variant: DRAFT	Git Hash: a736dc4
	Board Name: Input Protection	Project Name: Assignment 1		
	Sheet Title: /	File Name: Input-Protection.kicad_sch	Designer: R. HICKS	Date: 2025-01-12 Revision: + (Unreleased)
	Sheet Path: /	Reviewer:	Size: A3	Sheet: 1 of 4

[2] Block Diagram



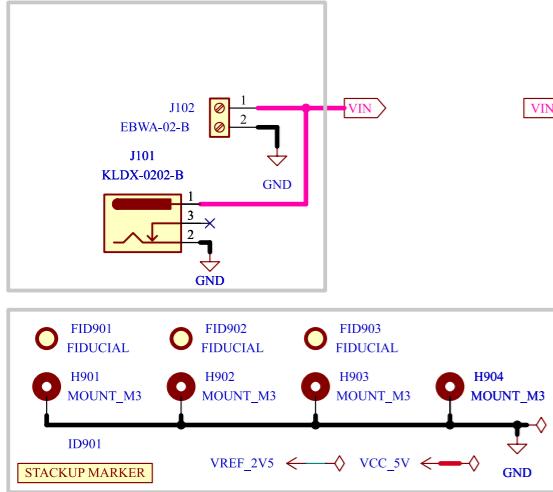
Target specifications:

Input voltage:	?? - ?? V
Spec 2	??
Spec 3	??
Spec 4	??

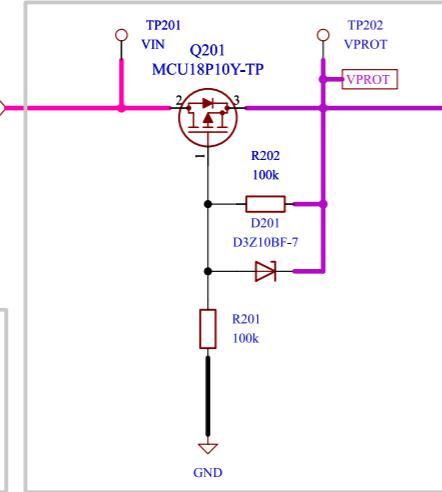
	Comments:	Company: University of Newcastle	Variant: DRAFT	Git Hash: a736dc4
	Board Name: Input Protection	Project Name: Assignment 1		
	Sheet Title: Block Diagram	File Name: Block Diagram.kicad_sch	Designer: R. HICKS	Date: 2025-01-12 + (Unreleased)
	Sheet Path: /Block Diagram/	Reviewer:	Size: A3	Sheet: 2 of 4

[3] Schematic

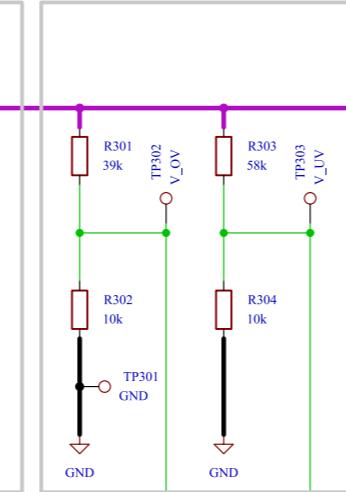
1. INTERCONNECTS



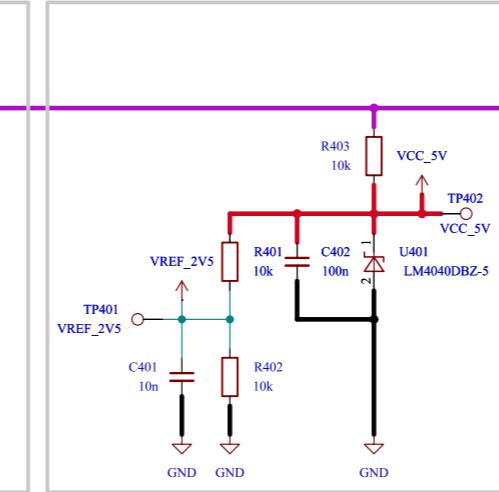
2. REVERSE POLARITY PROTECTION



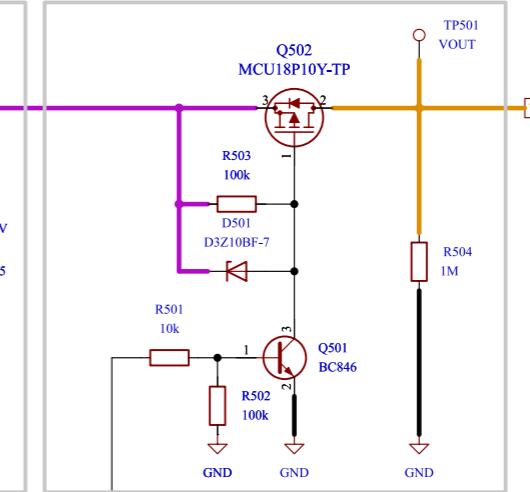
3. VOLTAGE SENSING



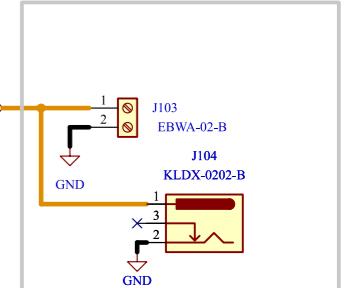
4. 5V & 2V5 VREF



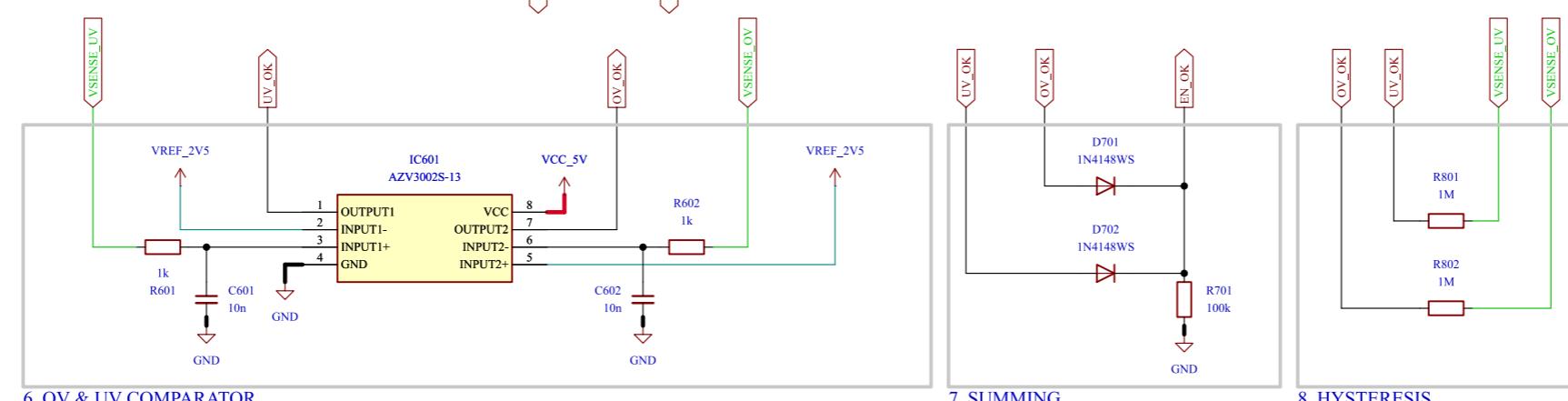
5. PASS ELEMENT



1. INTERCONNECTS (CONT.)



9. ERC & MISC.



Comments: Input Protection	Company: University of Newcastle	Variant: DRAFT	Git Hash: a736dc4
	Board Name: Assignment 1	Project Name: Assignment 1	
Sheet Title: Schematic	File Name: Schematic.kicad_sch	Designer: R. HICKS	Date: 2025-01-12 + (Unreleased)
Sheet Path: /Schematic/	Reviewer:	Size: A3	Sheet: 3 of 4

[4] Revision History

	Comments:	Company: University of Newcastle	Variant: DRAFT	Git Hash: a736dc4
		Board Name: Input Protection	Project Name: Assignment 1	
	Sheet Title: Revision History	File Name: Revision History.kicad_sch	Designer: R. HICKS	Date: 2025-01-12 Revision: + (Unreleased)
	Sheet Path: /Revision History/		Reviewer:	Size: A4 Sheet: 4 of 4