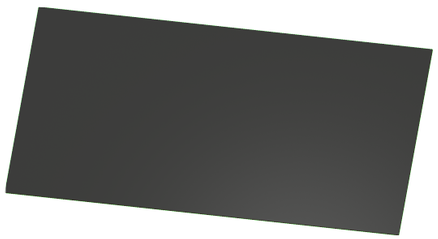
Input Protection

Variant: DRAFT

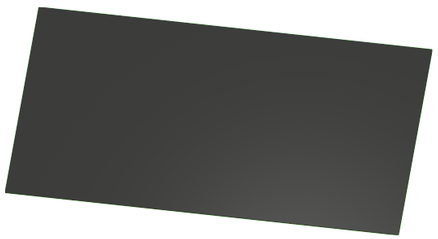
2026-02-07

Rev + (Unreleased)

TOP VIEW



BOTTOM VIEW



NOTES

Comment

Not fitted components are marked as ✗

DRAFT - Very early stage of schematic, ignore details.
PRELIMINARY - Close to final schematic.
CHECKED - There shouldn't be any mistakes. Contact the engineer if you find any.
RELEASED - A board with this schematic has been sent to production.

Date: 07-Feb-2026

DESIGN CONSIDERATIONS

DESIGN NOTE: Example text for informational design notes.

DESIGN NOTE: Example text for debug notes.

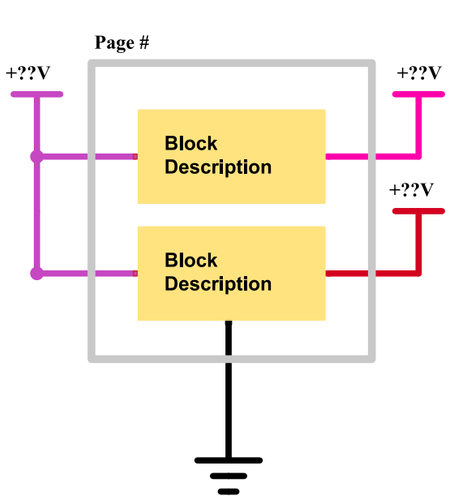
DESIGN NOTE: Example text for cautionary design notes.

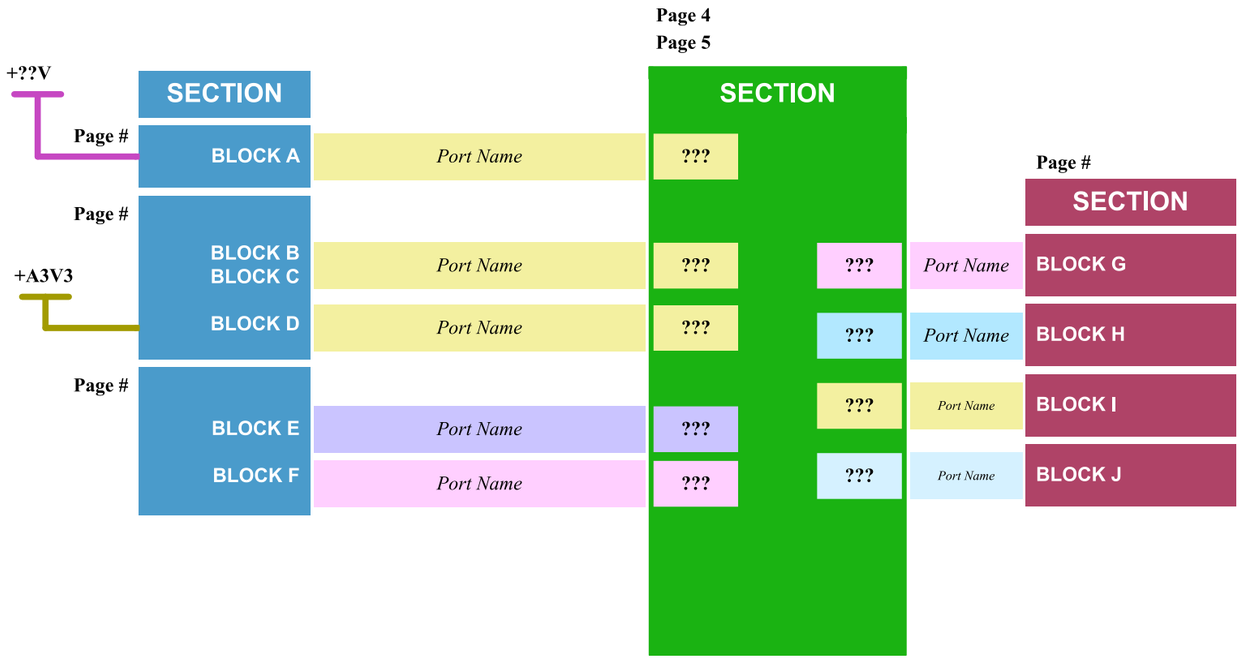
DESIGN NOTE: Example text for critical design notes.

LAYOUT NOTE: Example text for critical layout guidelines.

Comments:	Company: University of Newcastle		Variant: DRAFT	Git Hash: aea0273
	Board Name: **Input Protection**		Project Name: **Assignment 1**	
Sheet Title:	File Name: Input-Protection.kicad_sch	Designer: R. HICKS	Date: 2025-01-12	Revision: + (Unreleased)
Sheet Path: /		Reviewer:	Size: **A3**	Sheet: **1** of **4**

[2] BLOCK DIAGRAM





TARGET SPECIFICATIONS:

INPUT VOLTAGE:	-50 - +50 V
OUTPUT VOLTAGE:	??
Spec 3	??
Spec 4	??

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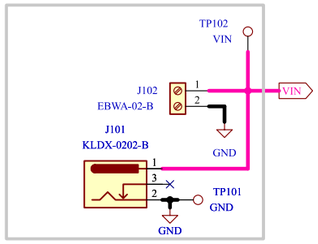
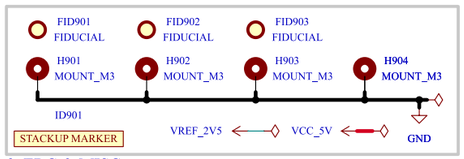
Sheet Title: BLOCK DIAGRAM	File Name: Block Diagram.kicad_sch	Designer: R. HICKS	Date: 2025-01-12	Revision: + (Unreleased)
Sheet Path: /Block Diagram/		Reviewer:	Size: **A3**	Sheet: **2** of **4**

[3] SCHEMATIC

1. INTERCONNECTS



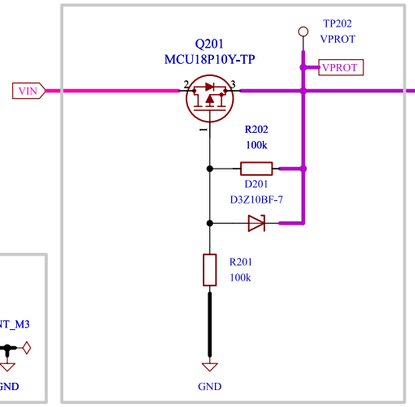


9. ERC & MISC.

DESIGN NOTE:
This PMOSFET is acting as an ideal diode [1].

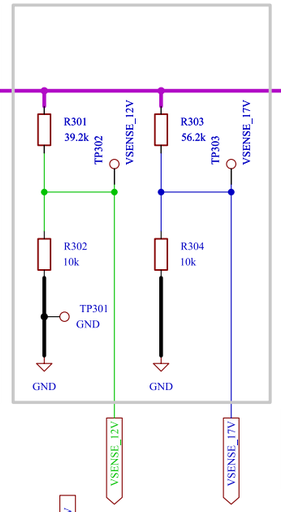
10V zener from Gate to Source to limit VGS <= 10V under all VIN and transient conditions to protect PMOSFET. 100K Gate to Source resistor to not allow floating Gate. 100K Gate pulldown resistor so Gate is off and not affected by leakage or capacitive coupling when VIN removed or reversed.

2. REVERSE POLARITY PROTECTION



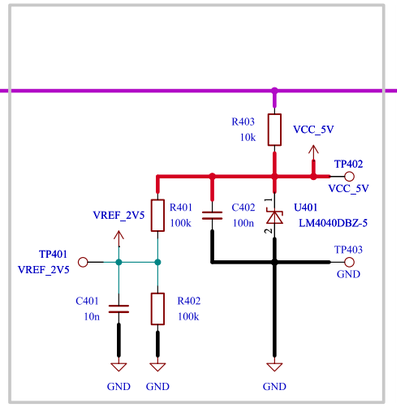
DESIGN NOTE:
VSENSE=VPROT*RBOT/(RTOP+RBOT)
We are comparing with 2V5 VREF,
VTRIP=2.5*(RTOP+RBOT)/RBOT.
We'll pick RBOT=10k for stiffness which leaves:
RTOP = 2000 * (2*VTRIP-5).
For 12V, RTOP=38K. For 17V, RTOP=58K.

3. VOLTAGE SENSING



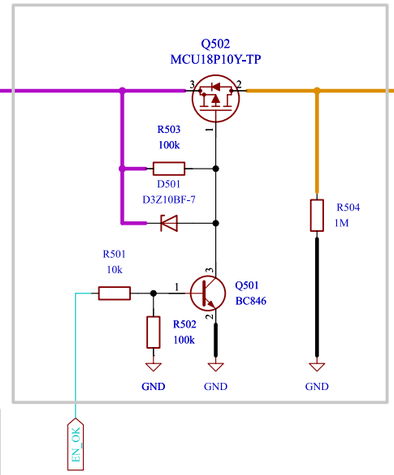
DESIGN NOTE:
Per TI [2] choose Rs such that IRMIN<IR<IRMAX
(IRMAX=15mA), accounting for VIN range and load.
With VIN_MIN=12V, VIN_MAX=50V, VOUT=5 V,
IRMIN=75µA and ILOAD_MAX=I(2.5 V divider)+I(EN_OK pull-up)+Iq(AZV3002)=250µA+50µA+9µA,
Rs_MAX=(VIN_MIN−VOUT)/(ILOAD_MAX+IRMIN)=18K
Rs_MIN=(VIN_MAX−VOUT)/IRMAX=3K. Rs=10K is selected to guarantee regulation at 12V while limiting shunt current at 50V.

4. VCC_5V & VREF_2V5



DESIGN NOTE:
VREF_2V5 is generated from VCC_5V with a 100K/100K divider. A 10nF capacitor from VREF_2V5 to GND provides low-pass filtering f_c=1/(2π*50K*10n)=318Hz.

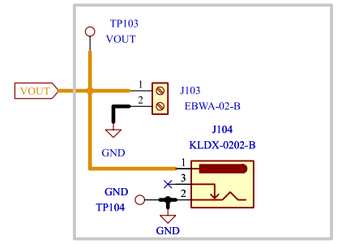
5. PASS ELEMENT



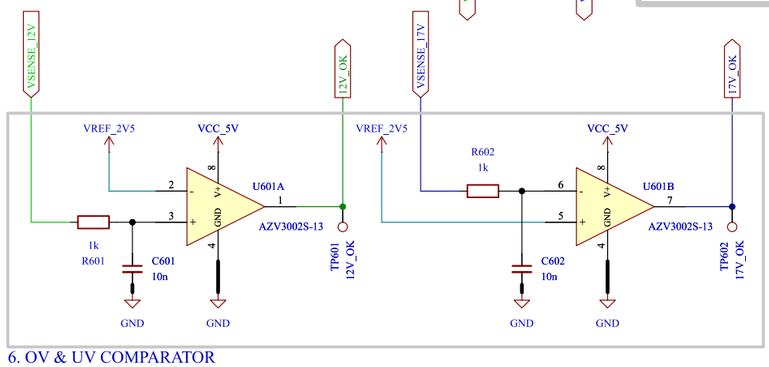
DESIGN NOTE:
The pass PMOSFET is used as a high-side load disconnect controlled by the window comparator logic.
When EN_OK is high, the gate is pulled low via the NPN driver, turning the device on and allowing VOUT to track VPROT with a small RDS(on) drop.
When EN_OK is low, the gate is released and pulled toward the source, fully turning the device off and isolating the load.
A 1Meg output resistor to ground prevents floating output with no load.

DESIGN NOTE:
BC846 provides low-side gate drive for the pass PMOS. 10K base resistor limits base current from EN_OK, 100K base-emitter pull-down ensures defined OFF state during startup and fault conditions.

1. INTERCONNECTS (CONT.)

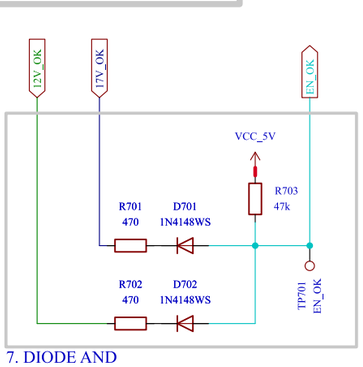


6. OV & UV COMPARATOR



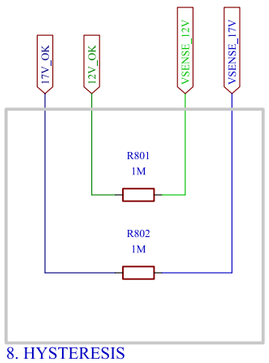
DESIGN NOTE:

7. DIODE AND



DESIGN NOTE:

8. HYSTERESIS



DESIGN NOTE:

[1] https://www.ti.com/lit/an/slvae57b/slvae57b.pdf?ts=1770319054914

[2] https://www.ti.com/lit/ds/symlink/lm4040-n.pdf?ts=1752678691365

Comments:	Company: **University of Newcastle**		Variant: DRAFT	Git Hash: aea0273
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Sheet Title: SCHEMATIC	File Name: Schematic.kicad_sch	Designer: R. HICKS	Date: 2025-01-12	Revision: + (Unreleased)
Sheet Path: /Schematic/		Reviewer:	Size: **A3**	Sheet: **3** of **4**

[4] REVISION HISTORY

	Comments:	Company: University of Newcastle		Variant: DRAFT	Git Hash: aea0273
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	Sheet Title: REVISION HISTORY	File Name: Revision History.kicad_sch	Designer: R. HICKS	Date: 2025-01-12	Revision: + (Unreleased)
	Sheet Path: /Revision History/		Reviewer:	Size: **A4**	Sheet: **4** of **4**