

INPUT PROTECTION

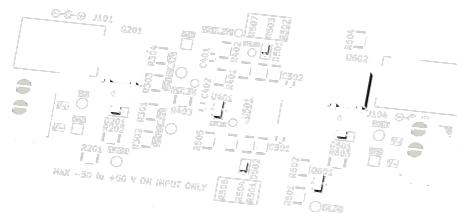
Variant: PRELIMINARY

2026-02-09

Rev + (Unreleased)

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TOP VIEW



BOTTOM VIEW

NOTES

Comment

Not fitted components are marked as

DRAFT – Very early stage of schematic, ignore details.

PRELIMINARY – Close to final schematic.

CHECKED – There shouldn't be any mistakes. Contact the engineer if found.

RELEASED – A board with this schematic has been sent to production.

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for debug notes.

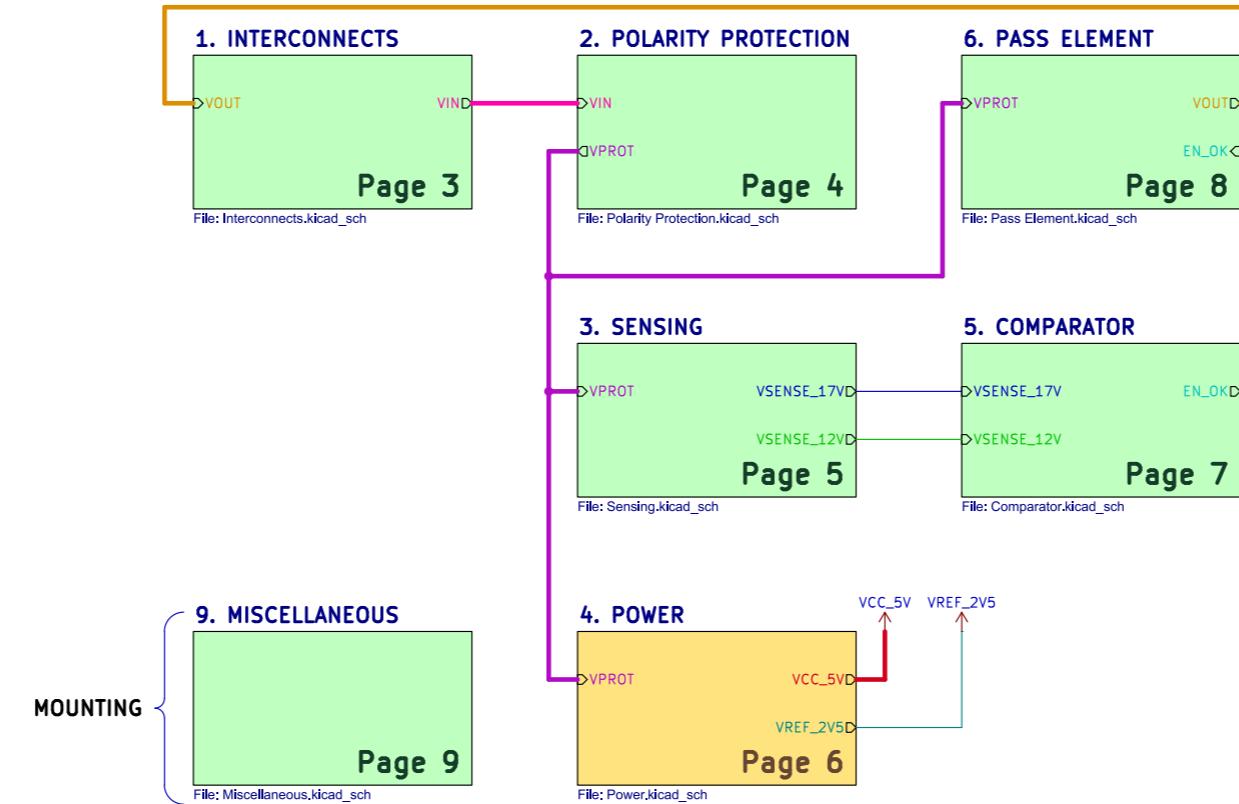
DESIGN NOTE:
Example text for cautionary design notes.

DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

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ENG APP			
MFR APP			
SHEET PATH	GIT HASH	DRAWING No	
/	3eaf265		
FILENAME	Input-Protection.kicad_sch	VARIANT	PRELIMINARY
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[2] ARCHITECTURE



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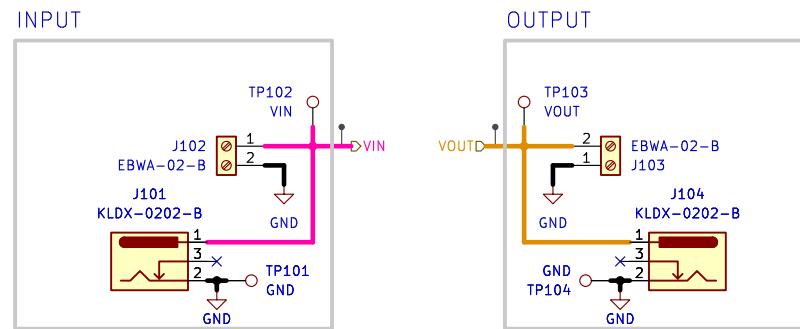
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[3] 1. INTERCONNECTS



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1. INTERCONNECTS

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FILENAME Interconnects.kicad_sch

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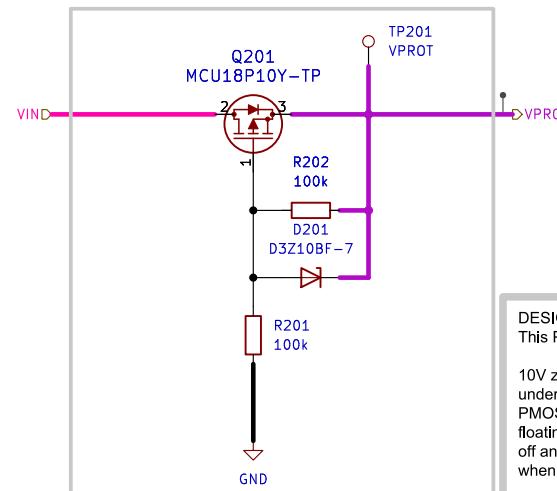
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[4] 2. POLARITY PROTECTION



DESIGN NOTE:
This PMOSFET is acting as an ideal diode [1].

10V zener from Gate to Source to limit $V_{GS} \leq 10V$ under all VIN and transient conditions to protect PMOSFET. 100k Gate to Source resistor to not allow floating Gate. 100k Gate pulldown resistor so Gate is off and not affected by leakage or capacitive coupling when VIN removed or reversed.

[1] <https://www.ti.com/lit/an/slvae57b/slvae57b.pdf?ts=1770319054914>

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3ea12265 POLARITY PROTECTION

FILENAME Polarity Protection.kicad_sch

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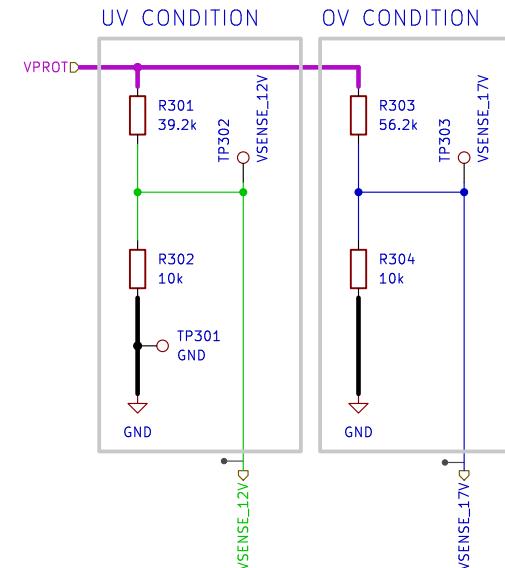
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[5] 3. SENSING



DESIGN NOTE:
 $VSENSE = VPROTD \cdot RBOT / (RTOP + RBOT)$
 We are comparing with 2V5 VREF,
 $VTRIP = 2.5 \cdot (RTOP + RBOT) / RBOT$.
 We'll pick $RBOT = 10k$ for stiffness which leaves:
 $RTOP = 2000 \cdot (2 \cdot VTRIP - 5)$.
 For 12V, $RTOP = 38K$. For 17V, $RTOP = 58K$.

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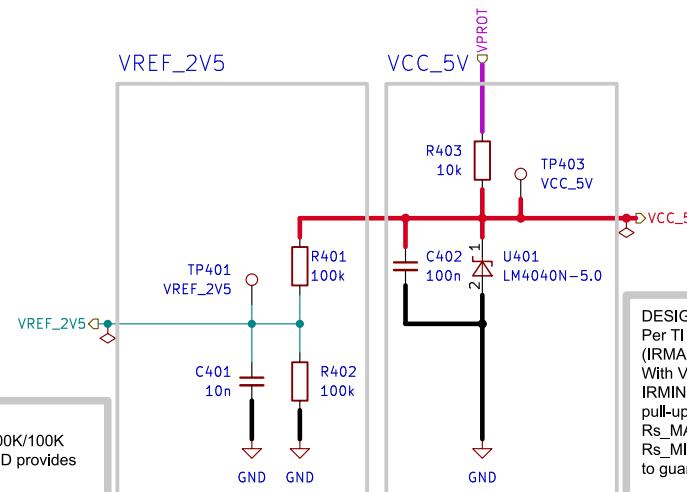
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[6] 4. POWER



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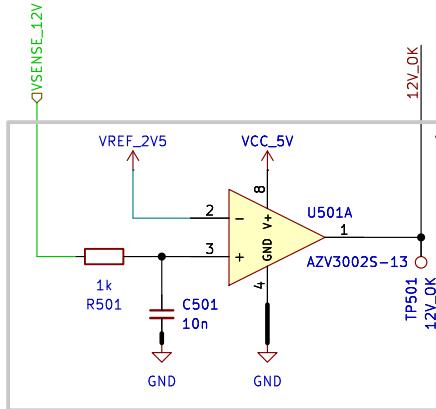
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[7] 5. COMPARATOR



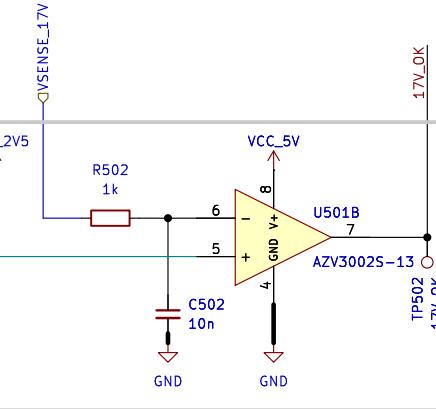
OV & UV COMPARATOR

DESIGN NOTE:

The AZV3002S-13 dual comparator is used to implement the 12-17 V window detector. Each comparator compares a scaled VPROT sense voltage (VSENSE) against VREF_2V5 to generate 12V_OK and 17V_OK signals. The device is selected for its low supply current (10uA worst) and rail-to-rail input.

DESIGN NOTE:

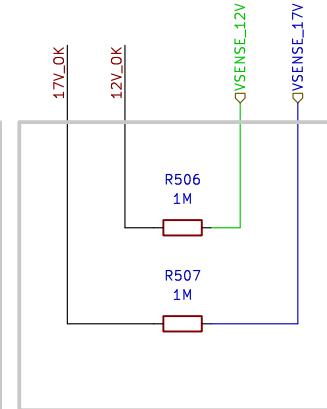
A simple low pass filter is placed on the VSENSE inputs of the comparators to smooth transitions and reduce chatter near the transition points. $f_c = 1/(2\pi \cdot 1k \cdot 10n) = 16Hz$.



DIODE AND

DESIGN NOTE:

EN_OK is generated using diode logic AND combining the 12V_OK and 17V_OK. A pull-up resistor biases EN_OK high, while either comparator output can clamp the node low through its diode, ensuring the pass MOSFET is enabled only when both voltage conditions are satisfied. Series resistors limit output interaction and improve stability with push-pull comparator outputs.



HYSTERESIS

DESIGN NOTE:

1M feedback resistor from comparator output to sense input provides external hysteresis to prevent chatter near the 12 V and 17 V thresholds. With divider $RTH = RTOP || RBOT = 8K$ and a 5 V output swing, hysteresis at VSENSE is about $\Delta VSENSE = 5 * RTH / RHY = 40mV$, or $\sim 0.2-0.3 V$ seen at VPROT.

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/ARCHITECTURE/5. COMPARATOR/

FILENAME Comparator.kicad_sch

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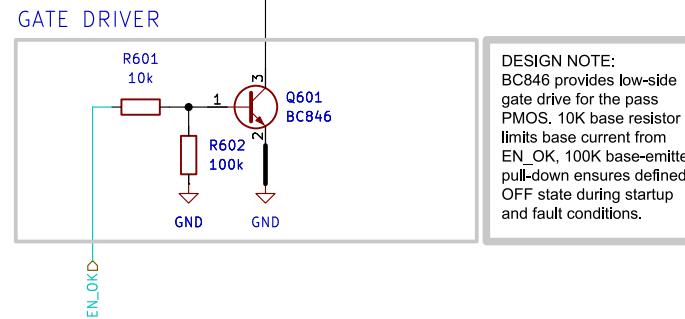
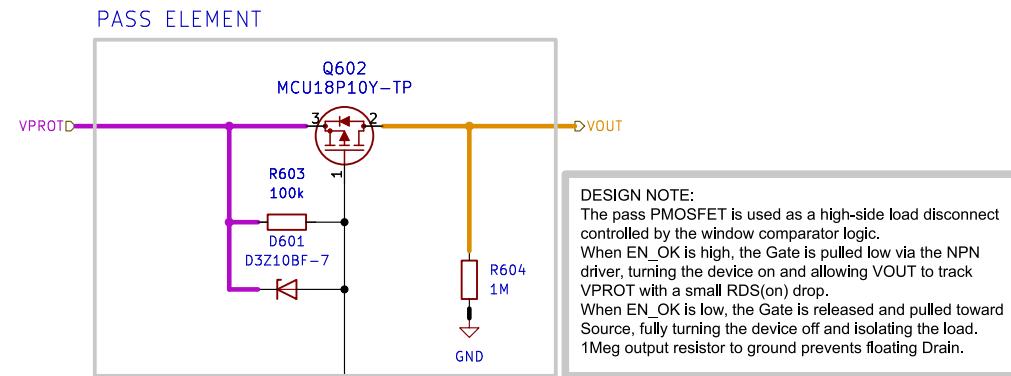
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[8] 6. PASS ELEMENT



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6. PASS ELEMENT

/ARCHITECTURE/6. PASS ELEMENT/

FILENAME Pass_Element.kicad_sch

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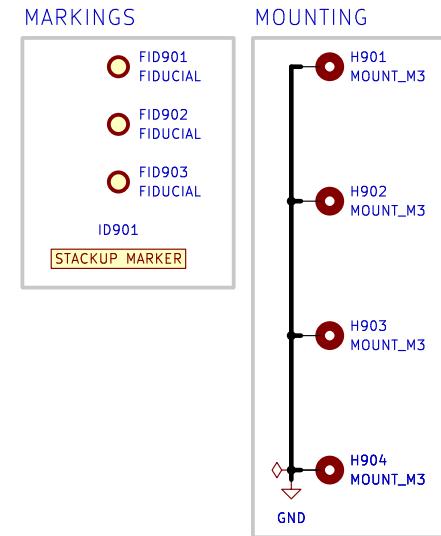
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[9] 9. MISCELLANEOUS



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FILENAME Miscellaneous.kicad_sch

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[10] REVISION HISTORY

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