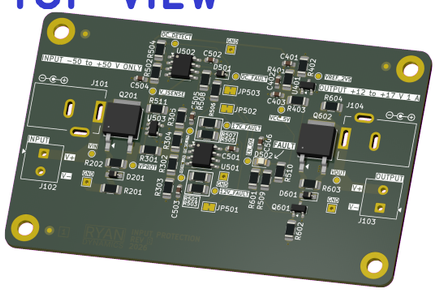
INPUT PROTECTION

VARIANT: RELEASED

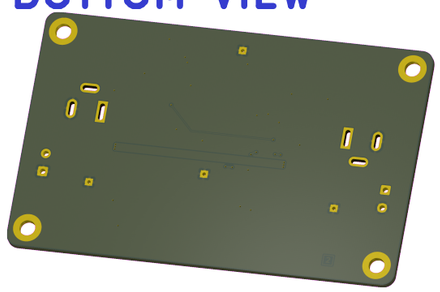
2026-02-18

REV 1.1.0

TOP VIEW



BOTTOM VIEW



NOTES

COMMENT

NOT FITTED COMPONENTS MARKED AS X

DRAFT – EARLY STAGE SCHEMATIC CAPTURE
PRELIMINARY – LATE STAGE SCHEMATIC CAPTURE
CHECKED – PCB LAYOUT CHECKED, CONTACT ENGINEER IF MISTAKE FOUND
RELEASED – READY FOR PRODUCTION

DESIGN CONSIDERATIONS

DESIGN NOTE: Example text for informational design notes.

DESIGN NOTE: Example text for debug notes.

DESIGN NOTE: Example text for cautionary design notes.

DESIGN NOTE: Example text for critical design notes.

LAYOUT NOTE: Example text for critical layout guidelines.

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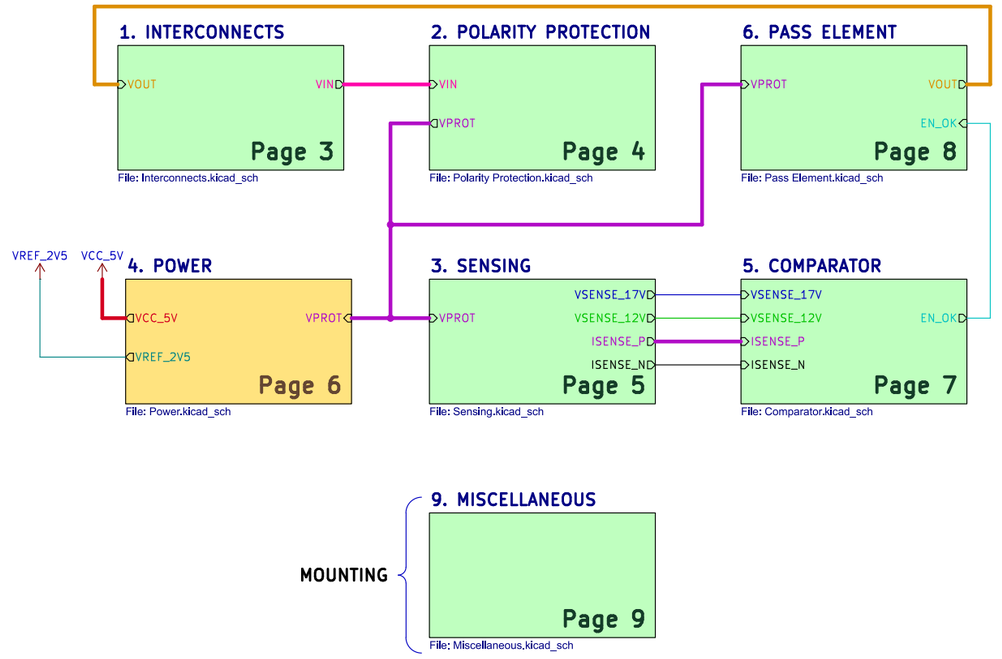
CHK			
ENG APP	INPUT PROTECTION		
MFR APP			
SHEET PATH /	GIT HASH 0313524	DRAWING No	A3
FILENAME Input-Protection.kicad_sch	VARIANT RELEASED	REVISION 1.1.0	SHEET 1 OF 10

[2] ARCHITECTURE



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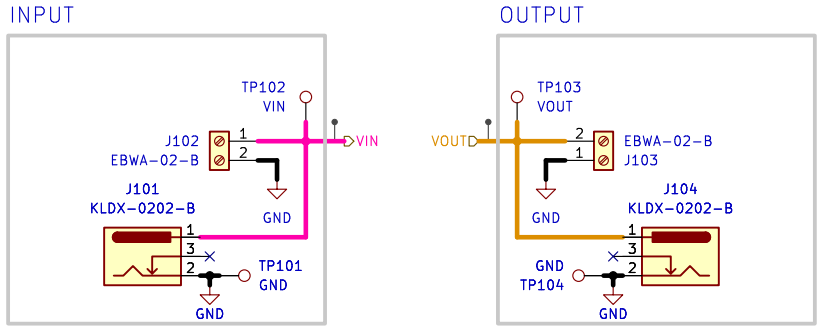
SHEET PATH /ARCHITECTURE/	GIT HASH 0313524	DRAWING No ARCHITECTURE	A3
FILENAME Project Architecture.kicad_sch	VARIANT RELEASED	REVISION 1.1.0 / SHEET 2 OF 10	

[3] 1. INTERCONNECTS



LAYOUT NOTE:
Large traces for VIN and VOUT, with 1oz copper a track width of >0.8mm is required to handle 2A of current with a FoS=2.

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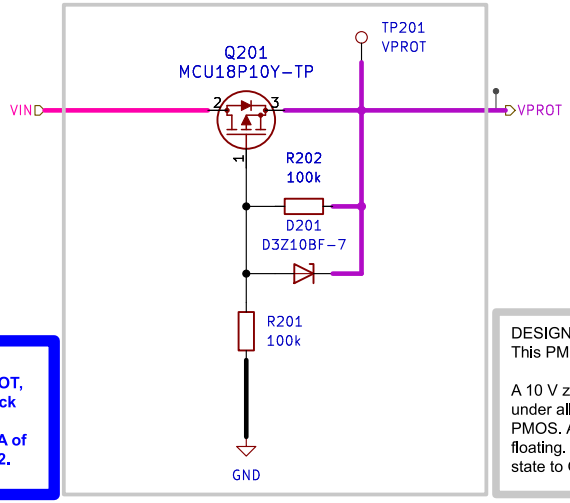
SHEET PATH /ARCHITECTURE/1. INTERCONNECTS/	GIT HASH 0313524	DRAWING No 1. INTERCONNECTS	A4
FILENAME Interconnects.kicad_sch	VARIANT RELEASED	REVISION 1.1.0	SHEET 3 OF 10

[4] 2. POLARITY PROTECTION



LAYOUT NOTE:
Large traces for VPROT, with 1oz copper a track width of >0.8 mm is required to handle 2 A of current with a FoS = 2.

DESIGN NOTE:
This PMOS is acting as an ideal diode [1].

A 10 V zener from gate to source limits V_{GS} <= 10 V under all VIN and transient conditions to protect the PMOS. A 100k gate to source resistor stops the gate floating. A 100k gate pulldown resistor sets default state to OFF when no voltage at VIN is present.

[1] https://www.ti.com/lit/an/slvae57b/slvae57b.pdf?ts=1770319054914

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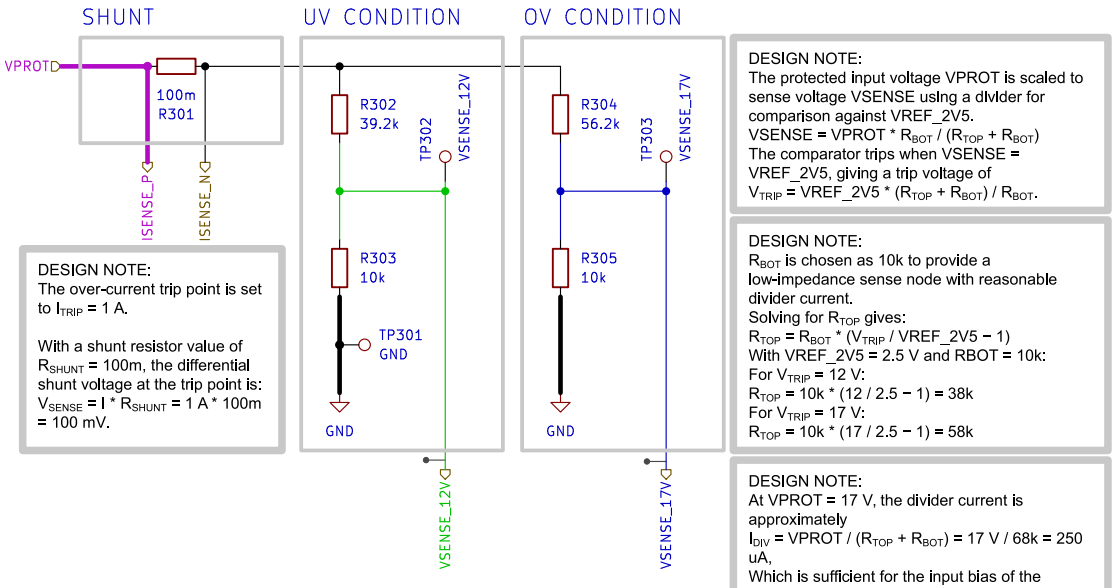
ENG APP	INPUT PROTECTION		
MFR APP			
SHEET PATH /ARCHITECTURE/2. POLARITY PROTECTION/	GIT HASH 0313524	DRAWING No POLARITY PROTECTION	A4
FILENAME Polarity Protection.kicad_sch	VARIANT RELEASED	REVISION 1.1.0	SHEET 4 OF 10

[5] 3. SENSING



DESIGN NOTE:
The over-current trip point is set to I_{TRIP} = 1 A.

With a shunt resistor value of R_{SHUNT} = 100m, the differential shunt voltage at the trip point is: $V_{SENSE} = I * R_{SHUNT}$ = 1 A * 100m = 100 mV.

DESIGN NOTE:
The protected input voltage VPROT is scaled to sense voltage VSENSE using a divider for comparison against VREF_2V5.
VSENSE = VPROT * R_{BOT} / (R_{TOP} + R_{BOT})
The comparator trips when VSENSE = VREF_2V5, giving a trip voltage of
V_{TRIP} = VREF_2V5 * (R_{TOP} + R_{BOT}) / R_{BOT}.

DESIGN NOTE:
R_{BOT} is chosen as 10k to provide a low-impedance sense node with reasonable divider current.
Solving for R_{TOP} gives:
R_{TOP} = R_{BOT} * (V_{TRIP} / VREF_2V5 − 1)
With VREF_2V5 = 2.5 V and RBOT = 10k:
For V_{TRIP} = 12 V:
R_{TOP} = 10k * (12 / 2.5 − 1) = 38k
For V_{TRIP} = 17 V:
R_{TOP} = 10k * (17 / 2.5 − 1) = 58k

DESIGN NOTE:
At VPROT = 17 V, the divider current is approximately
I_{DIV} = VPROT / (R_{TOP} + R_{BOT}) = 17 V / 68k = 250 uA,
Which is sufficient for the input bias of the comparators.

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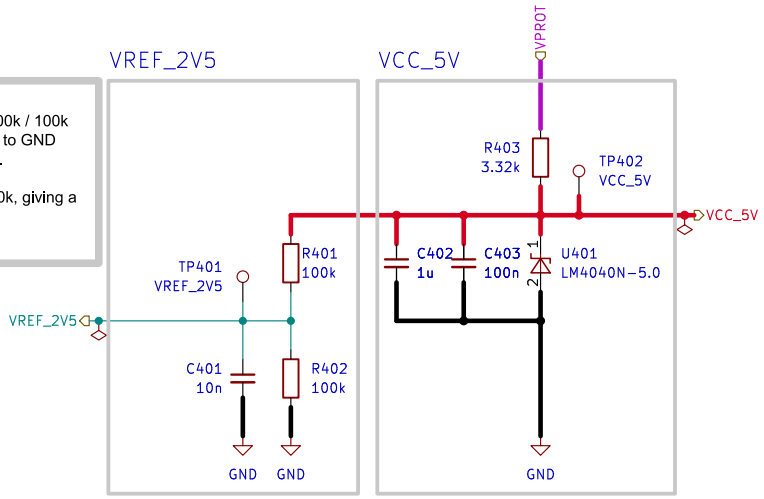
ENG APP	INPUT PROTECTION		
MFR APP			
SHEET PATH /ARCHITECTURE/3. SENSING/	GIT HASH 0313524	DRAWING No 3. SENSING	A4
FILENAME Sensing.kicad_sch	VARIANT RELEASED	REVISION 1.1.0	SHEET 5 OF 10

[6] 4. POWER

DESIGN NOTE:
VREF_2V5 is generated from VCC_5V using a 100k / 100k resistive divider. A 10n capacitor from VREF_2V5 to GND provides low-pass filtering to reduce supply noise.

The effective source resistance of the divider is 50k, giving a cutoff frequency of:
$f_c = 1 / (2\pi * 50k * 10n) = 318$ Hz.



DESIGN NOTE:
Per TI [2], choose the series resistor R_S such that $I_{RMIN} < I_R < I_{RMAX}$ across the full input range, while supplying the worst-case load current from VCC_5V.
Assume:
$V_{IN,MIN} = 12$ V, $V_{IN,MAX} = 50$ V, $V_{OUT} = 5$ V
$I_{RMAX} = 15$ mA, $I_{RMIN} = 75$ uA
Worst-case VCC_5V load current with EN_OK high is estimated as:
$I_{LOAD,MAX} = I_{DIV,2V5} + I_{Q,LM393} + I_{Q,INA169} + I_{B,NPN}$
where:
$I_{DIV,2V5} = 5$ V / (100k + 100k) = 25 uA
$I_{Q,LM393} = 2 * 600$ µA = 1.2 mA (two LM393 packages)
$I_{Q,INA169} = 125$ uA
$I_{B,NPN} = (5$ V − 0.7 V) / 10k = 430 uA
Note:
The fault LED current is drawn only when EN_OK is low and is therefore not included in the EN_OK-high load budget.
Thus:
$I_{LOAD,MAX} = 25$ uA + 1.2 mA + 125 uA + 430 uA = 1.78 mA
This gives:
$R_{S,MAX} = (V_{IN,MIN} - V_{OUT}) / (I_{LOAD,MAX} + I_{RMIN}) = 7$ V / (1.78 mA + 0.075 mA) = 3.8k
$R_{S,MIN} = (V_{IN,MAX} - V_{OUT}) / I_{RMAX} = 45$ V / 15 mA = 3k
R_S (R403) is selected as 3.32k to ensure regulation at $V_{IN,MIN}$ while limiting shunt current at $V_{IN,MAX}$.

[2] https://www.ti.com/lit/ds/symlink/lm4040-n.pdf?ts=1752678691365

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CHK			
ENG APP	INPUT PROTECTION		
MFR APP			
SHEET PATH /ARCHITECTURE/4. POWER/	GIT HASH 0313524	DRAWING No 4. POWER	A4
FILENAME Power.kicad_sch	VARIANT RELEASED	REVISION 1.1.0	SHEET 6 OF 10

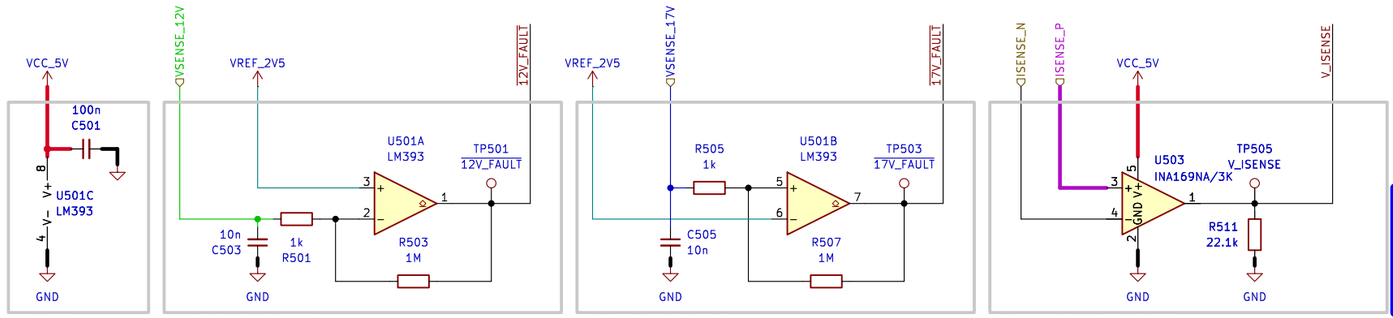
[7] 5. COMPARATOR

[3] https://www.ti.com/lit/an/snoaa35f/snoaa35f.pdf?ts=1770697404856

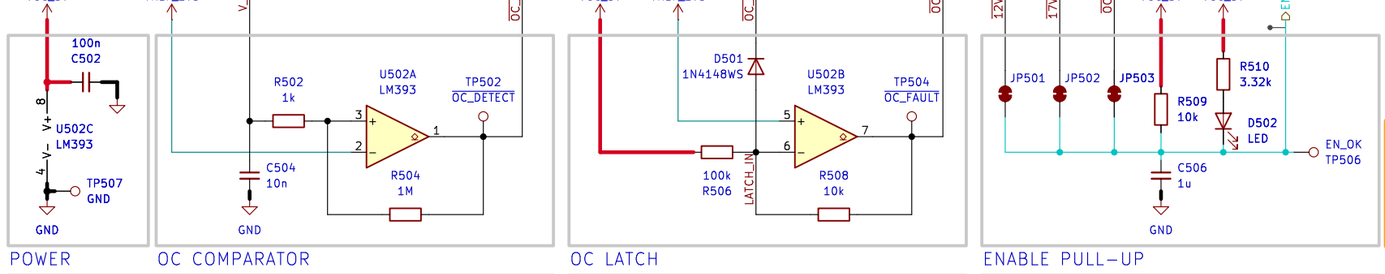
DESIGN NOTE:
LM393 dual comparators are used to implement under/over-voltage detection for the 12 V and 17 V supply thresholds. Each comparator compares a scaled VSENSE voltage against a 2.5 V precision reference (VREF_2V5) to generate active-low fault signals (12V_FAULT and 17V_FAULT). The LM393 is selected for its open-collector outputs.

DESIGN NOTE:
RC low-pass filters are placed on each VSENSE input to reduce noise and minimise chatter. The filters have a cutoff frequency of: $f_c = 1 / (2\pi * 1k * 10n) = 16$ Hz.
Positive feedback resistors provide hysteresis to again reduce chatter. Capacitor placement in accordance with 6.11 [3].

DESIGN NOTE:
Load current is measured using an INA169 current-sense amplifier. With a transconductance of 1 mA/V, the output current produces a voltage across the load, with R_{SHUNT}=100m and I_{TRIP}=1A with a 2.5 V reference we pick ~25k for R_L (R511). This corresponds to V_SENSE=2.5 V at 1 A.



LAYOUT NOTE:
Route ISENSE leads short from shunt to high-side current comparator.



DESIGN NOTE:
Solder bridges are provided to isolate different fault signals, cut the trace and re-solder to reconnect.

DESIGN NOTE:
A second LM393 comparator monitors the V_ISENSE signal from the current-sense amplifier and compares it against the 2.5 V reference to detect over-current conditions. When the sensed current exceeds the programmed threshold, the comparator output asserts an active-low over-current fault signal (OC_FAULT).

DESIGN NOTE:
The spare LM393 comparator is configured as a latch. This prevents "hiccups". OC_DETECT is reverse bias diode-coupled into the latch input. Once an over-current condition occurs, the latch forces OC_FAULT low and maintains the fault state until power is removed.

DESIGN NOTE:
All active-low fault signals (12V_FAULT, 17V_FAULT, and OC_LATCH) are combined using wired-AND logic enabled by the open-collector comparator outputs. A single pull-up resistor biases EN_OK high during normal operation. Assertion of any fault pulls EN_OK low, disabling the pass MOSFET.

PROJECT: ASSIGNMENT 1	Ryan Dynamics		
DRN: 2025-01-12 R. HICKS			
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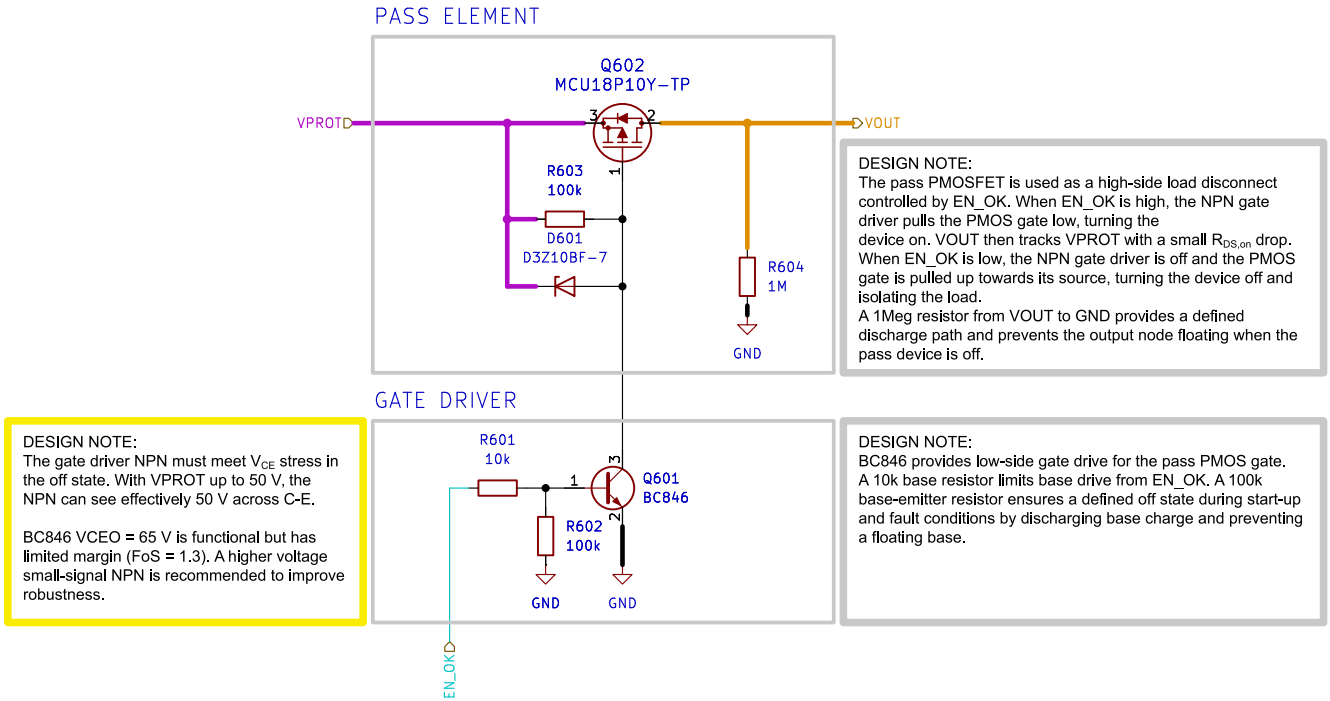
ENG APP	INPUT PROTECTION		
MFR APP			
SHEET PATH: /ARCHITECTURE/5. COMPARATOR/	GIT HASH: 0313524	DRAWING No: 5. COMPARATOR	A3
FILENAME: Comparator.kicad_sch	VARIANT: RELEASED	REVISION: 1.1.0	SHEET: 7 OF 10

[8] 6. PASS ELEMENT



DESIGN NOTE:
The pass PMOSFET is used as a high-side load disconnect controlled by EN_OK. When EN_OK is high, the NPN gate driver pulls the PMOS gate low, turning the device on. VOUT then tracks VPROT with a small $R_{DS,on}$ drop. When EN_OK is low, the NPN gate driver is off and the PMOS gate is pulled up towards its source, turning the device off and isolating the load.
A 1Meg resistor from VOUT to GND provides a defined discharge path and prevents the output node floating when the pass device is off.

DESIGN NOTE:
The gate driver NPN must meet V_{CE} stress in the off state. With VPROT up to 50 V, the NPN can see effectively 50 V across C-E.

BC846 VCEO = 65 V is functional but has limited margin (FoS = 1.3). A higher voltage small-signal NPN is recommended to improve robustness.

DESIGN NOTE:
BC846 provides low-side gate drive for the pass PMOS gate. A 10k base resistor limits base drive from EN_OK. A 100k base-emitter resistor ensures a defined off state during start-up and fault conditions by discharging base charge and preventing a floating base.

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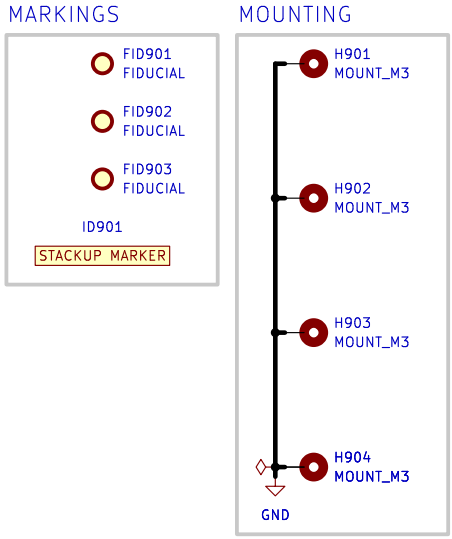
MFR APP	
SHEET PATH /ARCHITECTURE/6. PASS ELEMENT/	GIT HASH 0313524
FILENAME Pass Element.kicad_sch	VARIANT RELEASED
DRAWING No 6. PASS ELEMENT	REVISION 1.1.0
SHEET 8 OF 10	A4

[9] 9. MISCELLANEOUS



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ENG APP	INPUT PROTECTION		
MFR APP			
SHEET PATH /ARCHITECTURE/9. MISCELLANEOUS/	GIT HASH 0313524	DRAWING No 9. MISCELLANEOUS	A4
FILENAME Miscellaneous.kicad_sch	VARIANT RELEASED	REVISION 1.1.0	SHEET 9 OF 10

[10] REVISION HISTORY

Version 1.0.0 – 2026-02-11

Fixed

- N/A

Added

- Schematic capture and layout of a −50 to +50 V input +12 to +17 V output 1A protection PCBA

Changed

- N/A

Removed

- N/A

Version 1.1.0 – 2026-02-18

Fixed

- Tidied up some routing issues

Added

- N/A

Changed

- Changed fiducials to be circular
- Changed info block

Removed

- N/A

Version 1.1.0 – 2026-02-18

Fixed

- Tidied up some routing issues

Added

- N/A

Changed

- Changed fiducials to be circular
- Changed info block

Removed

- N/A

PROJECT ASSIGNMENT 1	Ryan Dynamics		
DRN 2025-01-12 R. HICKS			
CHK			
ENG APP	INPUT PROTECTION		
MFR APP			
SHEET PATH /REVISION HISTORY/	GIT HASH 0313524	DRAWING No REVISION HISTORY	A4
FILENAME Revision History.kicad_sch	VARIANT RELEASED	REVISION 1.1.0	SHEET 10 OF 10