

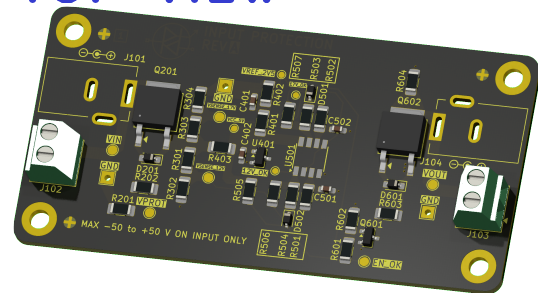
INPUT PROTECTION

Variant: PRELIMINARY

2026-02-09
Rev + (Unreleased)

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TOP VIEW



BOTTOM VIEW



NOTES

Comment

Not fitted components are marked as **X**

- DRAFT – Very early stage of schematic, ignore details.
- PRELIMINARY – Close to final schematic.
- CHECKED – There shouldn't be any mistakes. Contact the engineer if found.
- RELEASED – A board with this schematic has been sent to production.

DESIGN CONSIDERATIONS


DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for debug notes.

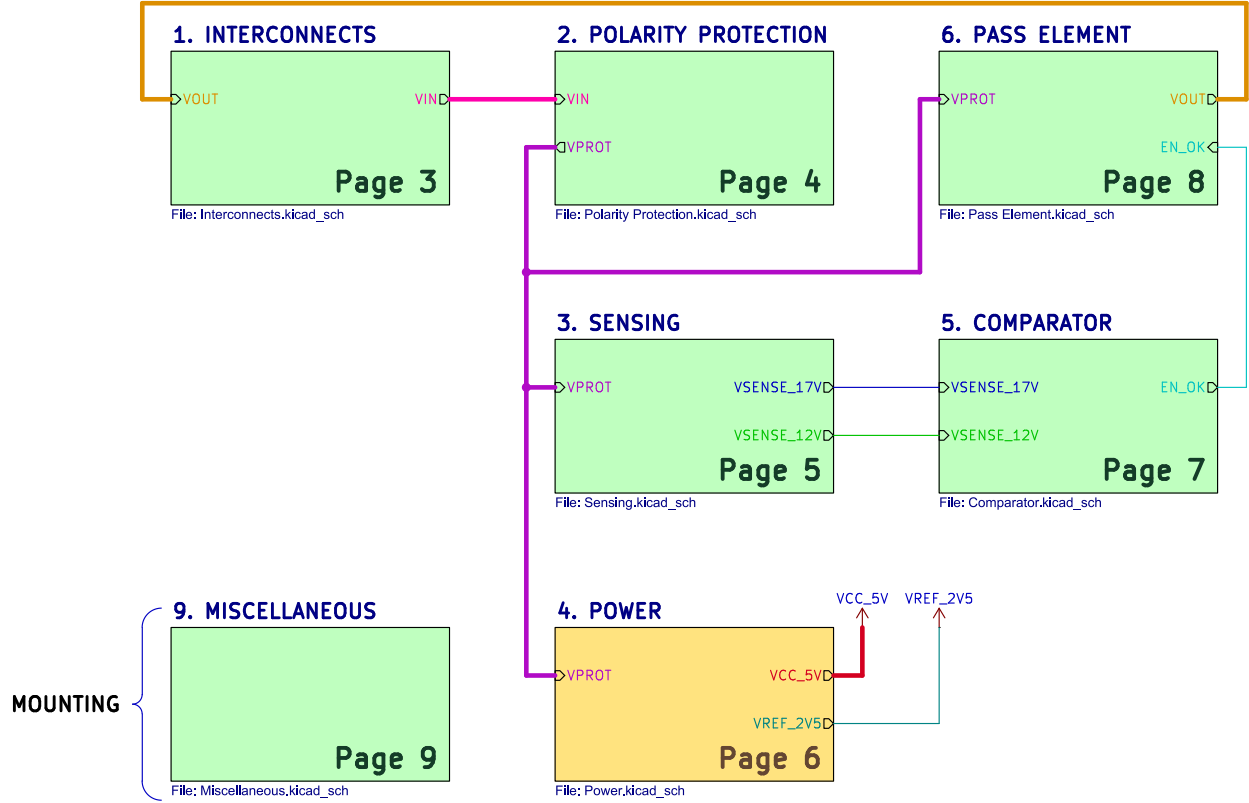
DESIGN NOTE:
Example text for cautionary design notes.


DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

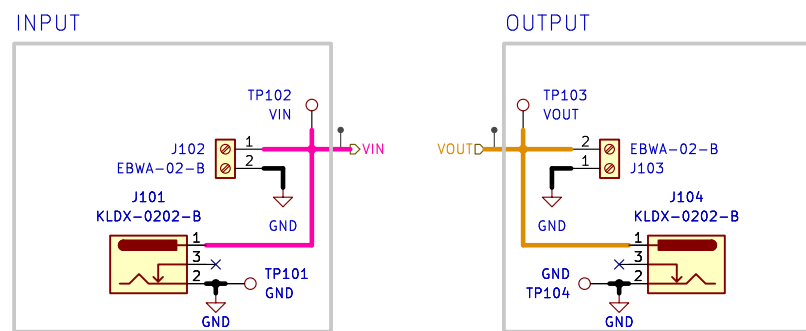
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DRN 2025-01-12 R. HICKS			
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MFR APP			
SHEET PATH	GIT HASH 3eaf265	DRAWING No	A3
FILENAME Input-Protection.kicad_sch	VARIANT PRELIMINARY	REVISION + (Unreleased) SHEET	
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[2] ARCHITECTURE



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SHEET PATH /ARCHITECTURE/	GIT HASH 3eaf265	DRAWING No ARCHITECTURE	A3
FILENAME Project Architecture.kicad_sch	VARIANT PRELIMINARY	REVISION + (Unreleased) SHEET 2 OF 10	

[3] 1. INTERCONNECTS



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1. INTERCONNECTS

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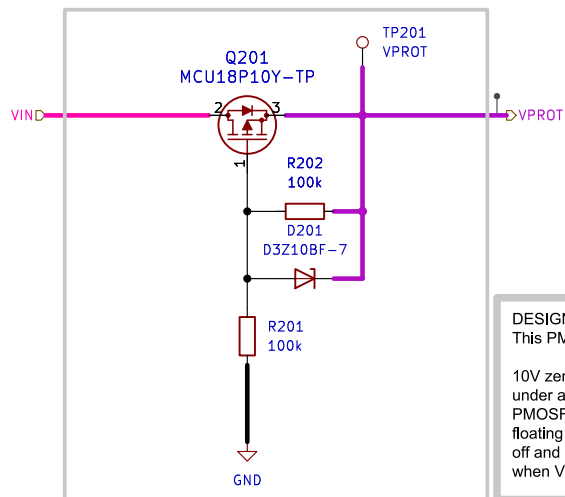
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[4] 2. POLARITY PROTECTION



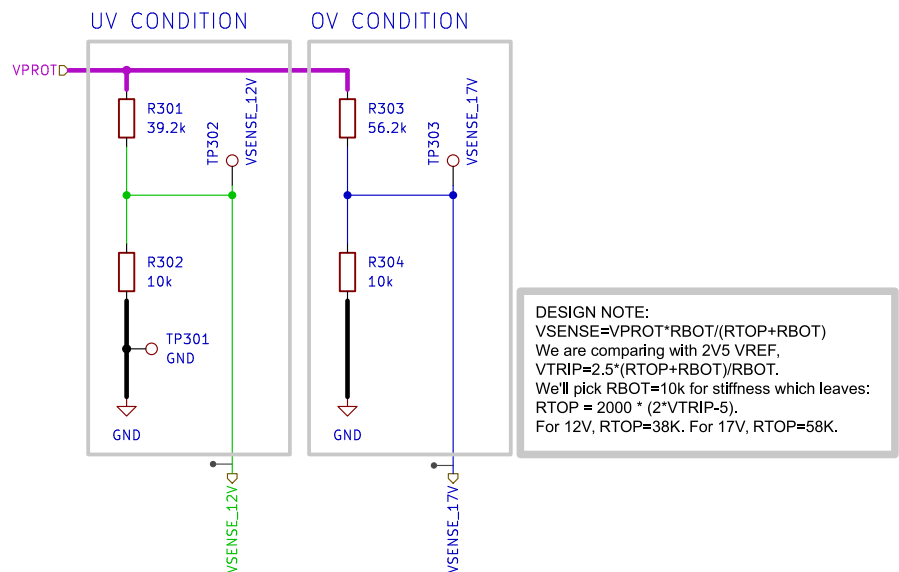
DESIGN NOTE:
This PMOSFET is acting as an ideal diode [1].

10V zener from Gate to Source to limit VGS \leq 10V under all VIN and transient conditions to protect PMOSFET. 100K Gate to Source resistor to not allow floating Gate. 100K Gate pulldown resistor so Gate is off and not affected by leakage or capacitive coupling when VIN removed or reversed.


[1] <https://www.ti.com/lit/an/slvae57b/slvae57b.pdf?ts=1770319054914>

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/ARCHITECTURE/2. POLARITY PROTECTION/	3ea12265	POLARITY PROTECTION	
FILENAME Polarity Protection.kicad_sch	VARIANT PRELIMINARY	REVISION + (Unreleased)	SHEET 4 OF 10

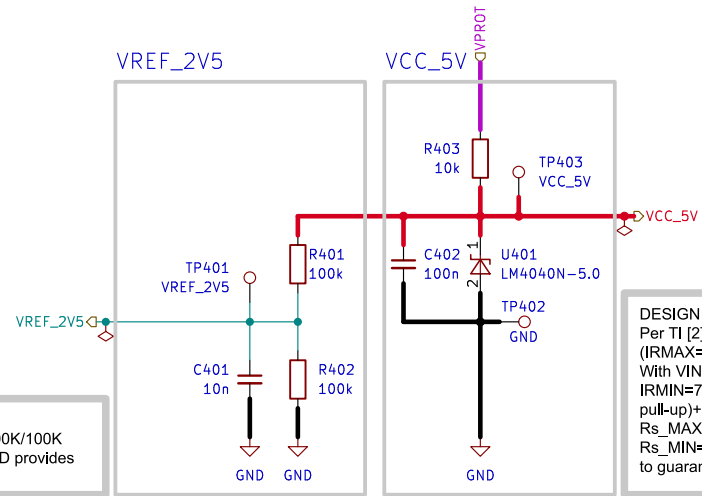
[5] 3. SENSING



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FILENAME	Sensing.kicad_sch

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[6] 4. POWER



DESIGN NOTE:
VREF_2V5 is generated from VCC_5V with a 100K/100K divider. A 10nF capacitor from VREF_2V5 to GND provides low-pass filtering $f_c = 1/(2\pi \cdot 50K \cdot 10n) = 318Hz$.

DESIGN NOTE:
Per TI [2] choose R_s such that $IR_{MIN} < IR < IR_{MAX}$ ($IR_{MAX} = 15mA$), accounting for VIN range and load. With $VIN_{MIN} = 12V$, $VIN_{MAX} = 50V$, $VOUT = 5V$, $IR_{MIN} = 75\mu A$ and $I_{LOAD_MAX} = I(2.5V \text{ divider}) + I(EN_OK \text{ pull-up}) + I_q(AZV3002) \approx 250\mu A + 50\mu A + 9\mu A$, $R_{s_MAX} = (VIN_{MIN} - VOUT)/(I_{LOAD_MAX} + IR_{MIN}) \approx 18K$, $R_{s_MIN} = (VIN_{MAX} - VOUT)/IR_{MAX} = 3K$. $R_s = 10K$ is selected to guarantee regulation at 12V & limit shunt current at 50V.

[2] <https://www.ti.com/lit/ds/symlink/lm4040-n.pdf?ts=1752678691365>

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/ARCHITECTURE/4. POWER/

FILENAME Power.kicad_sch



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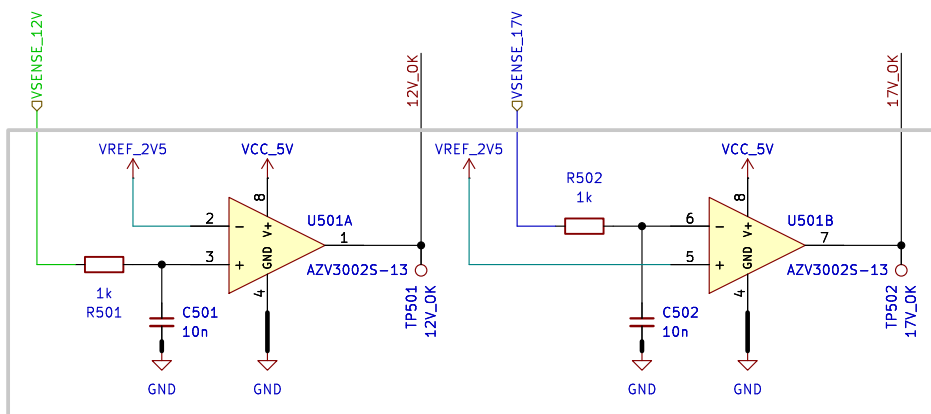
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[7] 5. COMPARATOR



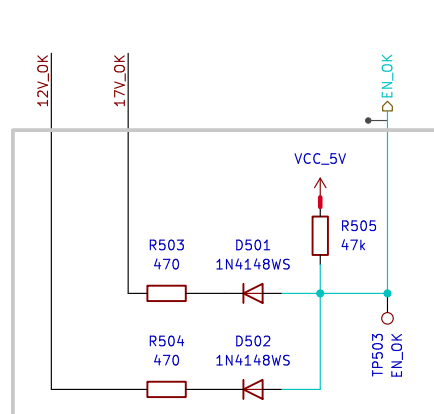
0V & UV COMPARATOR

DESIGN NOTE:

The AZV3002S-13 dual comparator is used to implement the 12-17 V window detector. Each comparator compares a scaled VPROT sense voltage (VSENSE) against VREF_2V5 to generate 12V_OK and 17V_OK signals. The device is selected for its low supply current (10uA worst) and rail-to-rail input.

DESIGN NOTE:

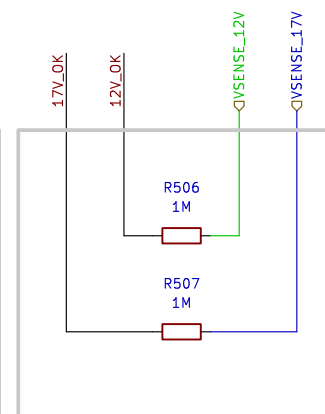
A simple low pass filter is placed on the VSENSE inputs of the comparators to smooth transitions and reduce chatter near the transition points. $f_c = 1 / (2\pi * 1K * 10n) = 16Hz$.



DIODE AND

DESIGN NOTE:

EN_OK is generated using diode logic AND combining the 12V_OK and 17V_OK. A pull-up resistor biases EN_OK high, while either comparator output can clamp the node low through its diode, ensuring the pass MOSFET is enabled only when both voltage conditions are satisfied. Series resistors limit output interaction and improve stability with push-pull comparator outputs.



HYSTERESIS

DESIGN NOTE:

1M feedback resistor from comparator output to sense input provides external hysteresis to prevent chatter near the 12 V and 17 V thresholds. With divider $R_{TH} = R_{TOP} || R_{BOT} \approx 8K$ and a 5 V output swing, hysteresis at VSENSE is about $\Delta V_{SENSE} \approx 5 * R_{TH} / R_{HYS} \approx 40mV$, or $\sim 0.2-0.3$ V seen at VPROT.

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/ARCHITECTURE/5. COMPARATOR/

FILENAME Comparator.kicad_sch



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5. COMPARATOR

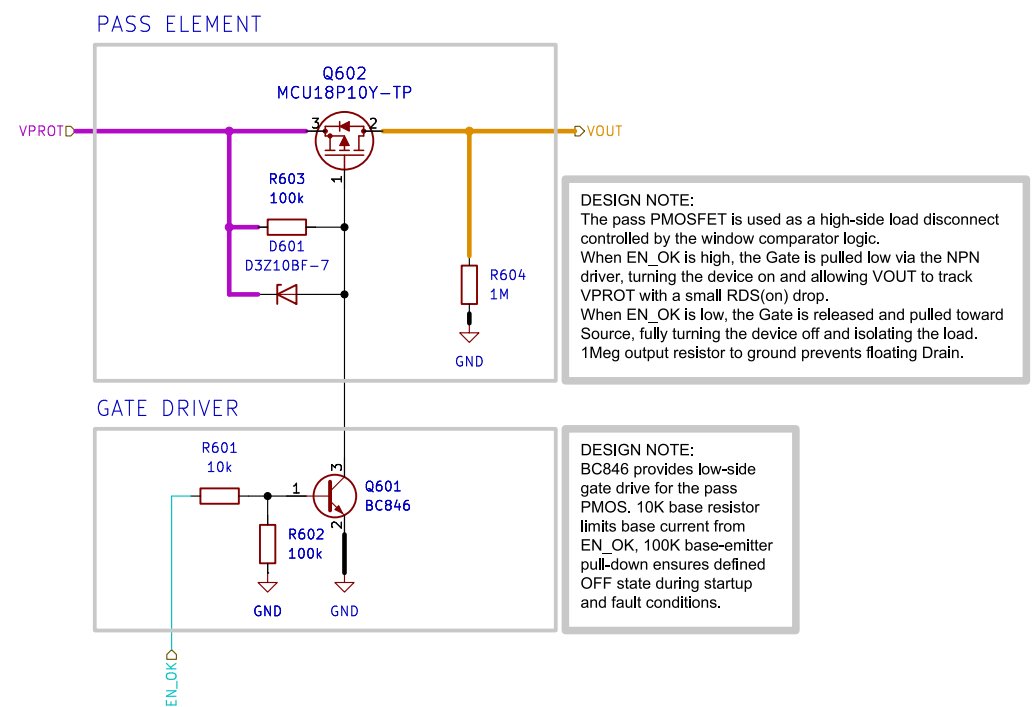
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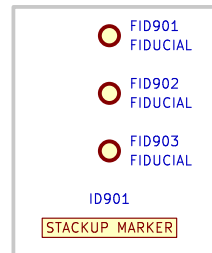
[8] 6. PASS ELEMENT



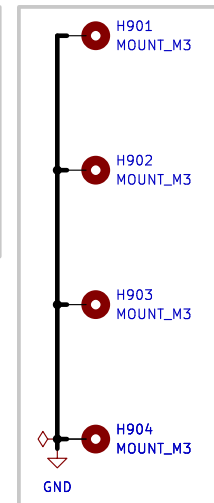
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/ARCHITECTURE/6. PASS ELEMENT/	3eaf265	6. PASS ELEMENT	
FILENAME Pass Element.kicad_sch	VARIANT PRELIMINARY	REVISION + (Unreleased)	SHEET 8 OF 10


[9] 9. MISCELLANEOUS

MARKINGS



MOUNTING



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3eaf265		9. MISCELLANEOUS		
FILENAME Miscellaneous.kicad_sch		VARIANT PRELIMINARY	REVISION + (Unreleased)	

[10] REVISION HISTORY

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