

INPUT PROTECTION

Variant: CHECKED

2026-02-10
Rev + (Unreleased)

Page	Index	Page	Index	Page	Index	Page	Index
1	Cover Page	11		21		31	
2	ARCHITECTURE	12		22		32	
3	1. INTERCONNECTS	13		23		33	
4	2. POLARITY PROTECTION	14		24		34	
5	3. SENSING	15		25		35	
6	4. POWER	16		26		36	
7	5. COMPARATOR	17		27		37	
8	6. PASS ELEMENT	18		28		38	
9	9. MISCELLANEOUS	19		29		39	
10	REVISION HISTORY	20		30		40	

TOP VIEW

BOTTOM VIEW

NOTES

Comment

Not fitted components are marked as **X**

- DRAFT** – Very early stage of schematic, ignore details.
PRELIMINARY – Close to final schematic.
CHECKED – There shouldn't be any mistakes. Contact the engineer if found.
RELEASED – A board with this schematic has been sent to production.

DESIGN CONSIDERATIONS


DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for debug notes.

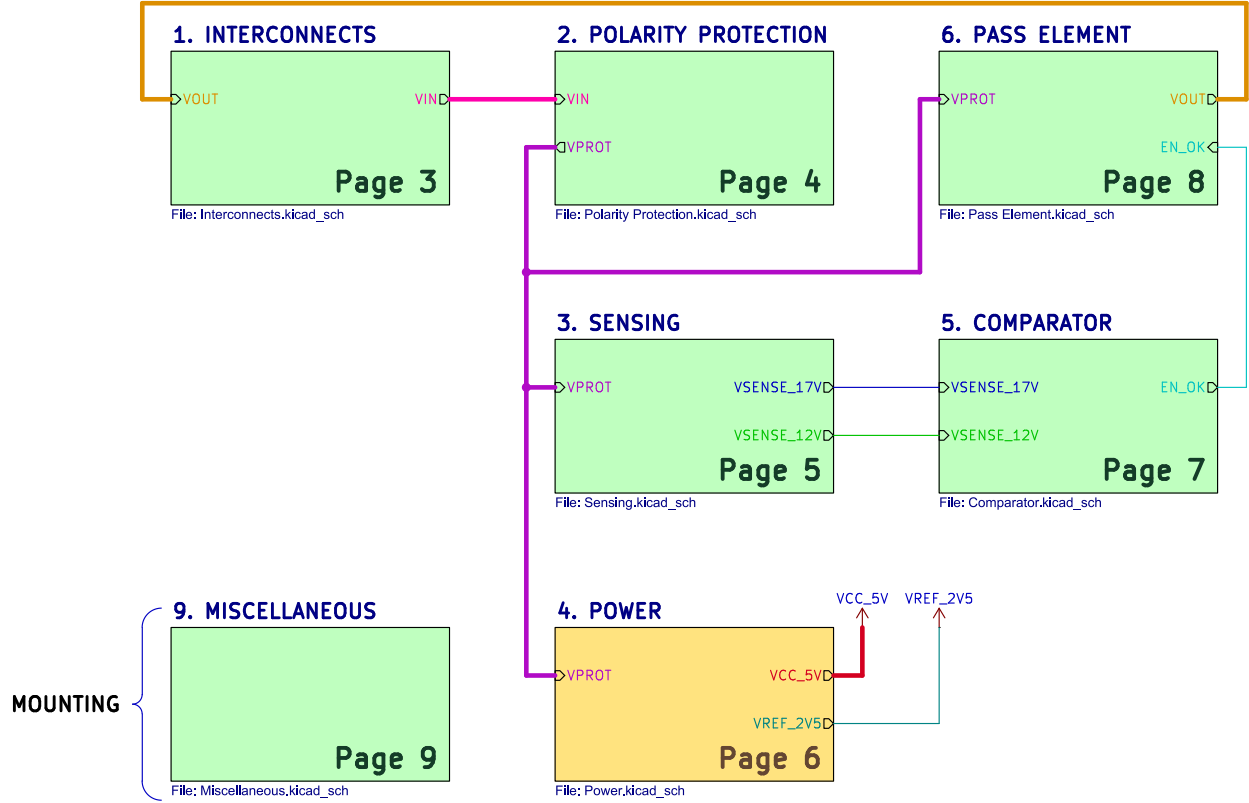
DESIGN NOTE:
Example text for cautionary design notes.


DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

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CHK			
ENG APP	INPUT PROTECTION		
MFR APP			
SHEET PATH	GIT HASH 3eaf265	DRAWING No	A3
FILENAME Input-Protection.kicad_sch	VARIANT CHECKED	REVISION + (Unreleased) SHEET	
		1 OF 10	

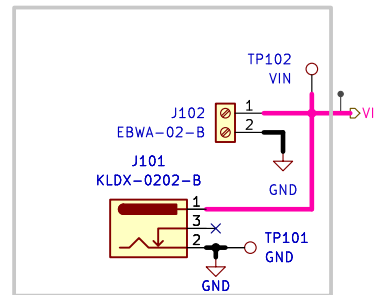
[2] ARCHITECTURE



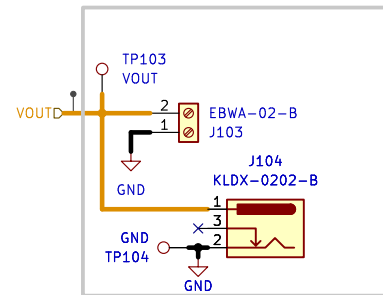
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SHEET PATH /ARCHITECTURE/	GIT HASH 3eaf265	DRAWING No ARCHITECTURE	A3
FILENAME Project Architecture.kicad_sch	VARIANT CHECKED	REVISION + (Unreleased) SHEET 2 OF 10	

[3] 1. INTERCONNECTS

INPUT



OUTPUT



LAYOUT NOTE:
Large traces for VIN and VOUT, with 1oz copper a track width of >0.8mm is required to handle 2A of current with a FoS=2.

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/ARCHITECTURE/1. INTERCONNECTS/

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1. INTERCONNECTS

A4

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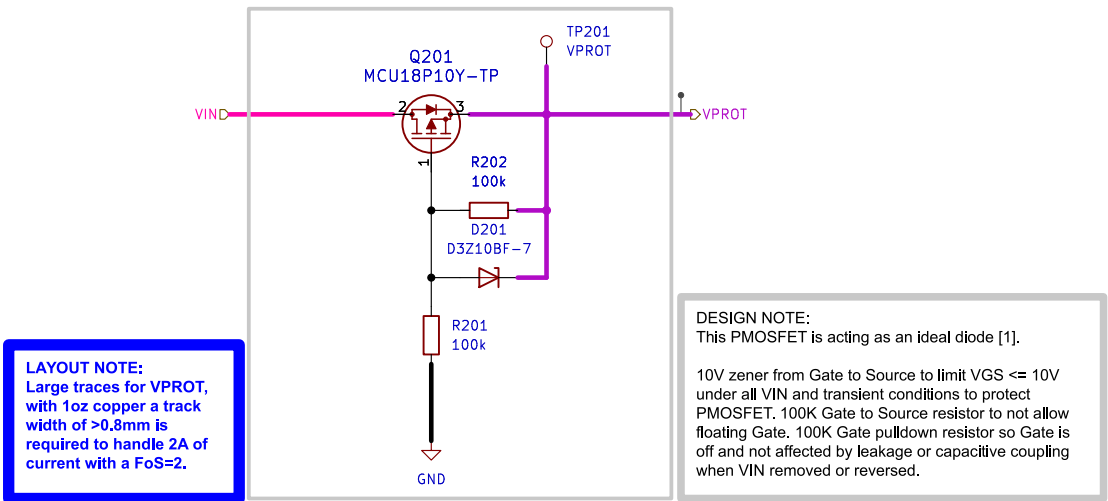
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3 OF 10

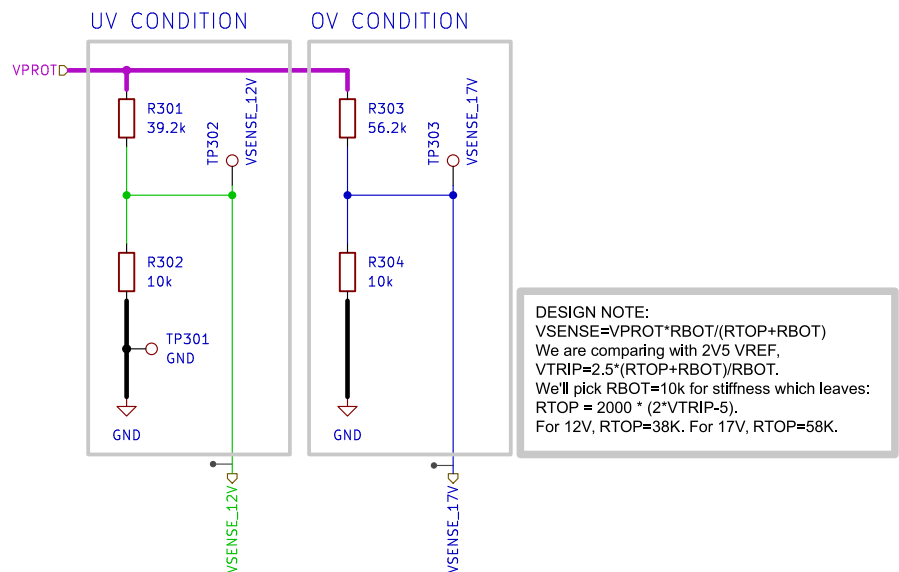
[4] 2. POLARITY PROTECTION




[1] <https://www.ti.com/lit/an/slvae57b/slvae57b.pdf?ts=1770319054914>

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MFR APP			
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/ARCHITECTURE/2. POLARITY PROTECTION/		GIT HASH 3ea12265	DRAWING No POLARITY PROTECTION
FILENAME Polarity Protection.kicad_sch	VARIANT	CHECKED	REVISION + (Unreleased) SHEET 4 OF 10

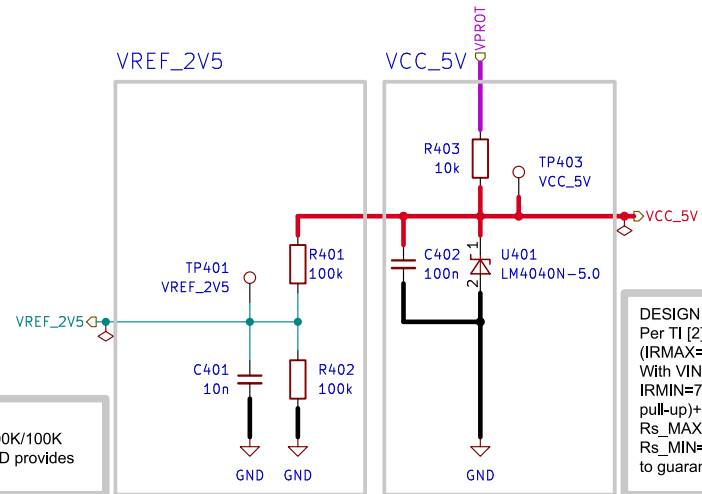
[5] 3. SENSING



PROJECT	ASSIGNMENT 1
DRN	2025-01-12 R. HICKS
CHK	
ENG APP	
MFR APP	
SHEET PATH	/ARCHITECTURE/3. SENSING/
FILENAME	Sensing.kicad_sch

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GIT HASH	DRAWING No	A4
3eaf265	3. SENSING	
VARIANT	CHECKED	REVISION + (Unreleased) SHEET
		5 OF 10

[6] 4. POWER



DESIGN NOTE:
VREF_2V5 is generated from VCC_5V with a 100K/100K divider. A 10nF capacitor from VREF_2V5 to GND provides low-pass filtering $f_c = 1/(2\pi \cdot 50K \cdot 10n) = 318Hz$.

DESIGN NOTE:
Per TI [2] choose R_s such that $IR_{MIN} < IR < IR_{MAX}$ ($IR_{MAX} = 15mA$), accounting for VIN range and load. With $V_{IN_MIN} = 12V$, $V_{IN_MAX} = 50V$, $V_{OUT} = 5V$, $IR_{MIN} = 75\mu A$ and $I_{LOAD_MAX} = I(2.5V \text{ divider}) + I(EN_OK \text{ pull-up}) + I_q(AZV3002) \approx 250\mu A + 50\mu A + 9\mu A$, $R_{s_MAX} = (V_{IN_MIN} - V_{OUT}) / (I_{LOAD_MAX} + IR_{MIN}) \approx 18K$, $R_{s_MIN} = (V_{IN_MAX} - V_{OUT}) / IR_{MAX} = 3K$. $R_s = 10K$ is selected to guarantee regulation at 12V & limit shunt current at 50V.

[2] <https://www.ti.com/lit/ds/symlink/lm4040-n.pdf?ts=1752678691365>

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/ARCHITECTURE/4. POWER/

FILENAME Power.kicad_sch



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4. POWER

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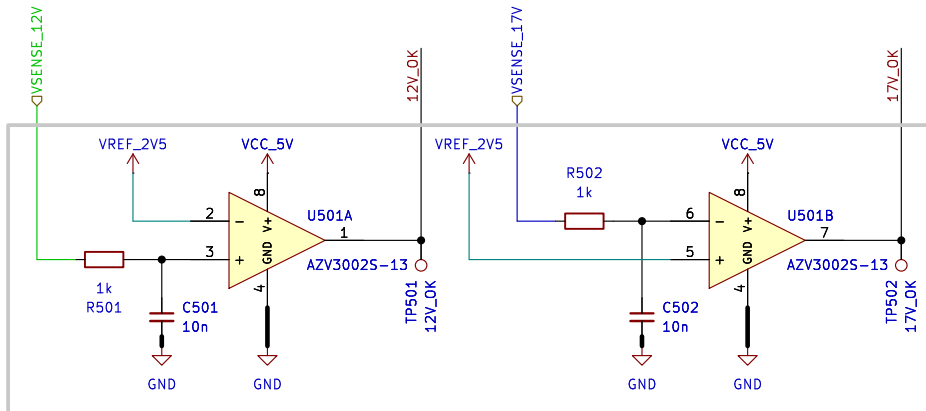
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REVISION + (Unreleased)

SHEET

6 OF 10

[7] 5. COMPARATOR



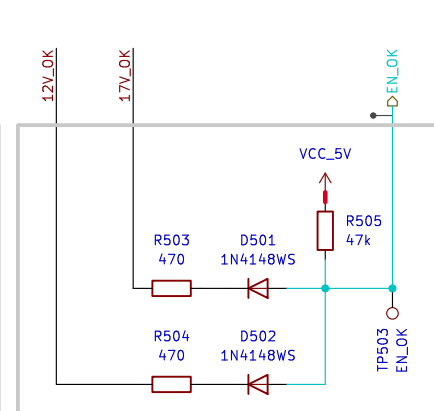
0V & UV COMPARATOR

DESIGN NOTE:

The AZV3002S-13 dual comparator is used to implement the 12-17 V window detector. Each comparator compares a scaled VPROT sense voltage (VSENSE) against VREF_2V5 to generate 12V_OK and 17V_OK signals. The device is selected for its low supply current (10uA worst) and rail-to-rail input.

DESIGN NOTE:

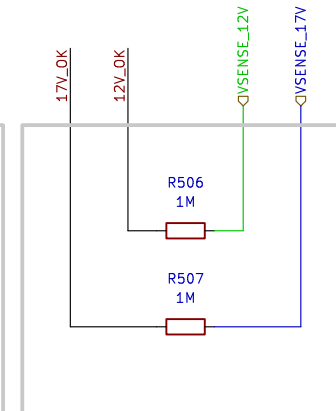
A simple low pass filter is placed on the VSENSE inputs of the comparators to smooth transitions and reduce chatter near the transition points. $f_c = 1 / (2\pi * 1K * 10n) = 16Hz$.



DIODE AND

DESIGN NOTE:

EN_OK is generated using diode logic AND combining the 12V_OK and 17V_OK. A pull-up resistor biases EN_OK high, while either comparator output can clamp the node low through its diode, ensuring the pass MOSFET is enabled only when both voltage conditions are satisfied. Series resistors limit output interaction and improve stability with push-pull comparator outputs.



HYSTERESIS

DESIGN NOTE:

1M feedback resistor from comparator output to sense input provides external hysteresis to prevent chatter near the 12 V and 17 V thresholds. With divider $R_{TH} = R_{TOP} || R_{BOT} \approx 8K$ and a 5 V output swing, hysteresis at VSENSE is about $\Delta V_{SENSE} \approx 5 * R_{TH} / R_{HYS} \approx 40mV$, or $\sim 0.2-0.3$ V seen at VPROT.

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ENG APP

MFR APP

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/ARCHITECTURE/5. COMPARATOR/

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Comparator.kicad_sch



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5. COMPARATOR

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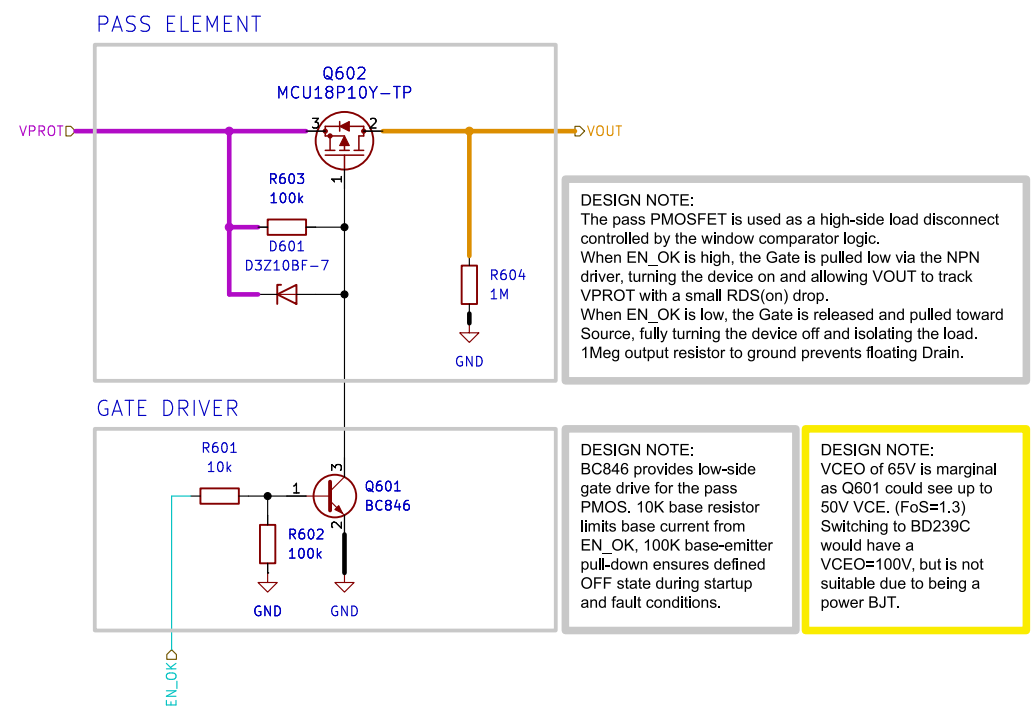
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SHEET

7 OF 10

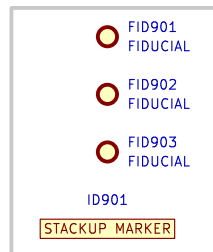
[8] 6. PASS ELEMENT



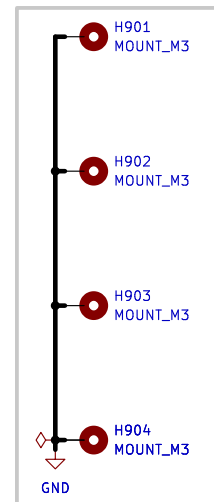
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MFR APP			
SHEET PATH	GIT HASH	DRAWING No	A4
/ARCHITECTURE/6. PASS ELEMENT/	3eaf265	6. PASS ELEMENT	
FILENAME Pass Element.kicad_sch	VARIANT CHECKED	REVISION + (Unreleased)	SHEET 8 OF 10

[9] 9. MISCELLANEOUS

MARKINGS



MOUNTING



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ASSIGNMENT 1

DRN
2025-01-12 R. HICKS

CHK

ENG APP

MFR APP

SHEET PATH

/ARCHITECTURE/9. MISCELLANEOUS/

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DRAWING No

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SHEET

9 OF 10

[10] REVISION HISTORY

PROJECT	ASSIGNMENT 1
DRN	2025-01-12 R. HICKS
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SHEET PATH	/REVISION HISTORY/
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3eaf265			
VARIANT	CHECKED	REVISION + (Unreleased)	SHEET
			10 OF 10