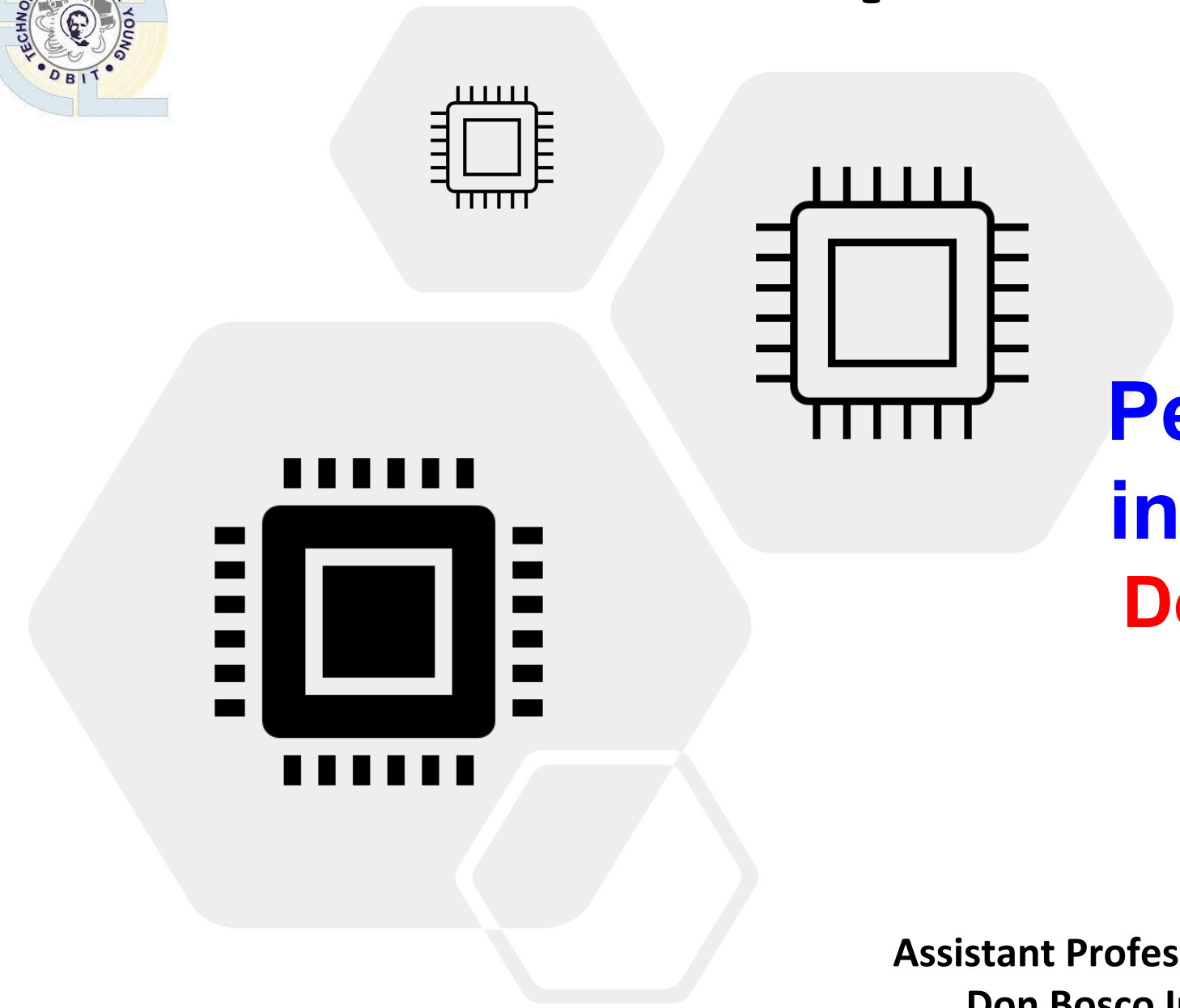
Microprocessor



Peripherals and their interfacing with 8086

Decoding and Mapping Techniques

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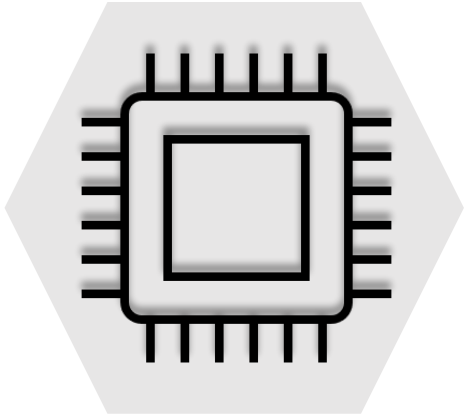
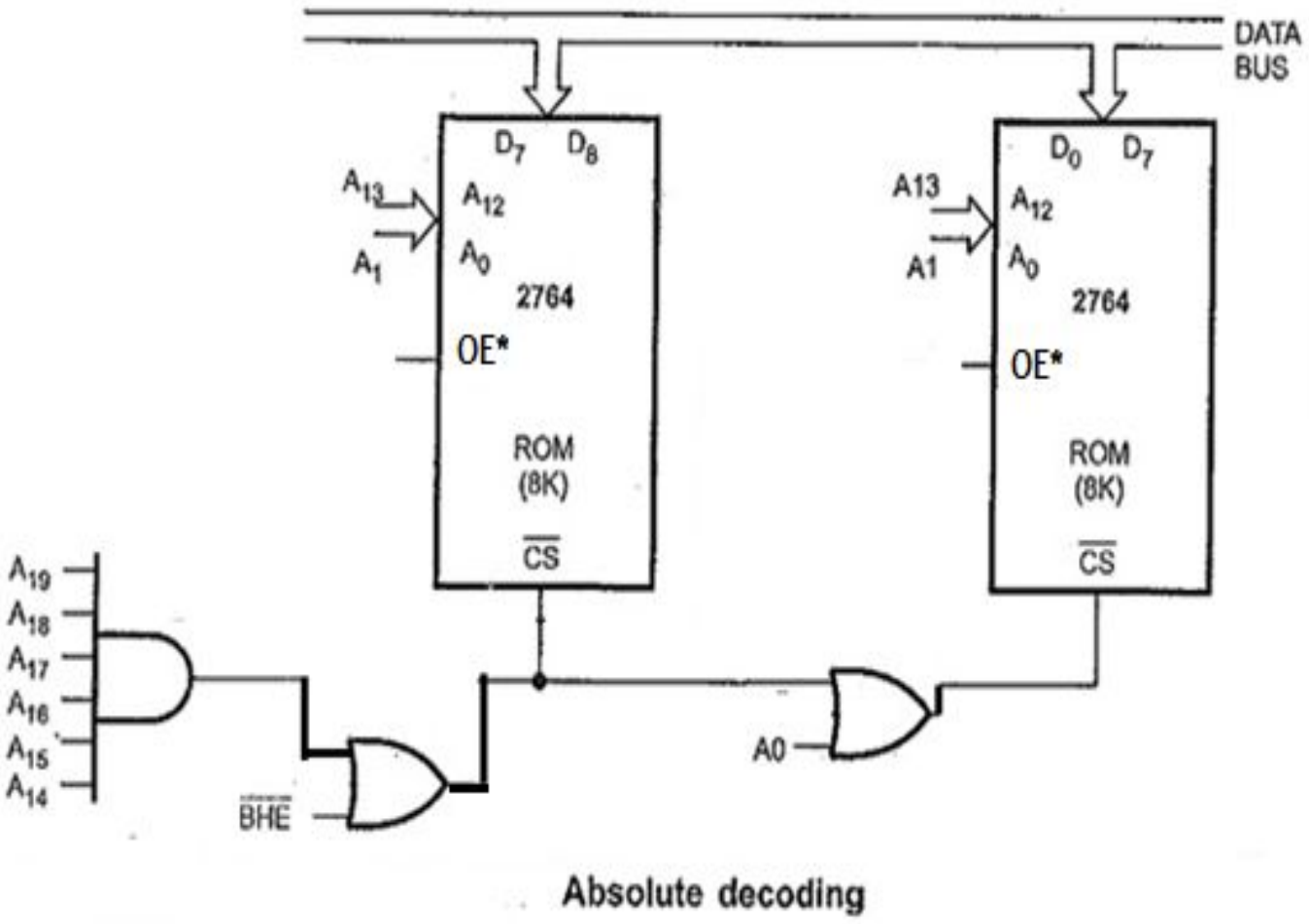
Topics to be discussed



- Decoding Techniques: Absolute and Linear
- Mapping Techniques:I/O mapped I/O and Memory mapped I/O

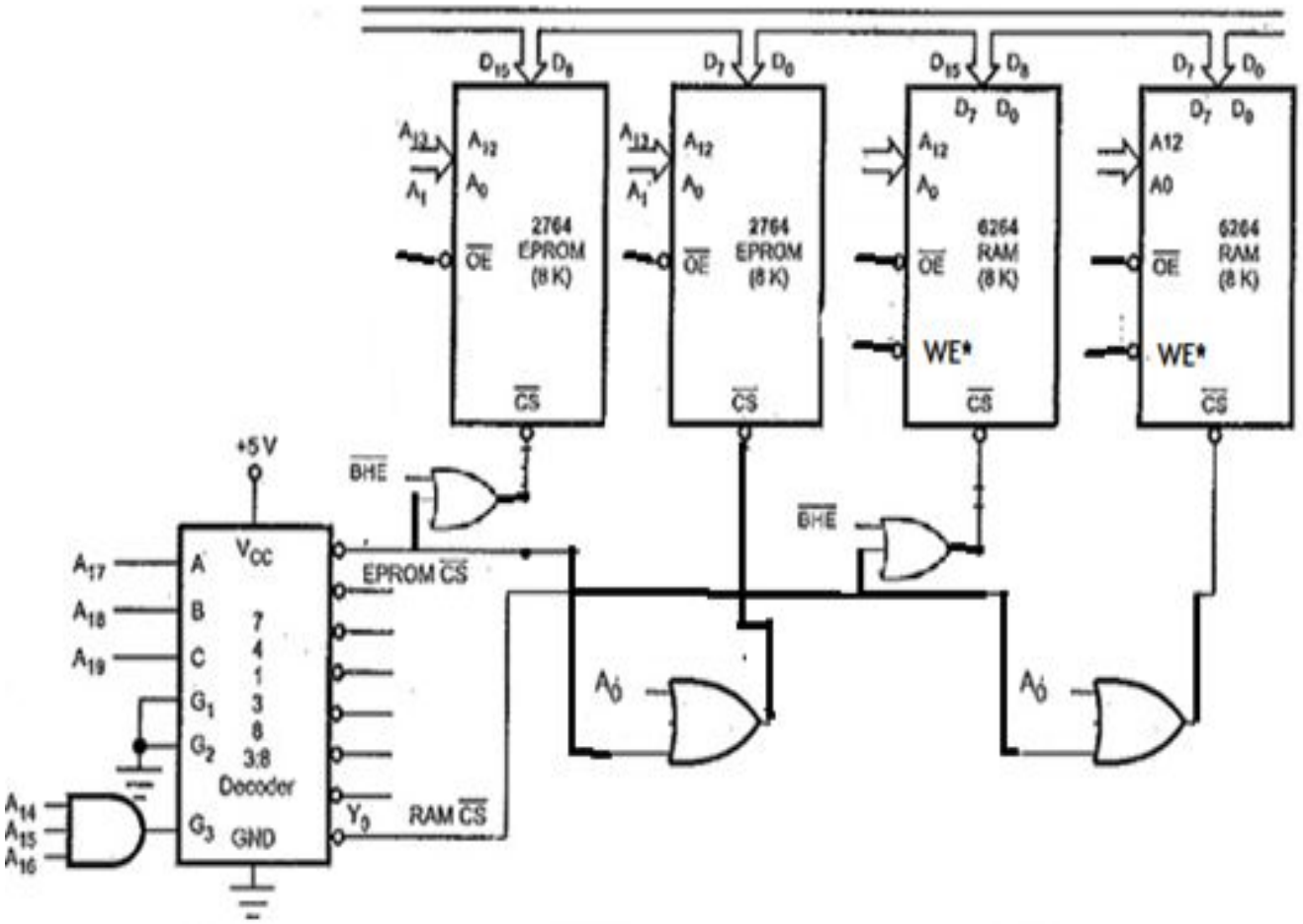
Absolute decoding (Full Decoding)



Absolute decoding

- The memory chip is selected only for the specified logic level on the address lines; no other logic levels can select the chip.
- First we interface the required address lines directly to the chips
- All remaining address lines are used to generate an unique chip select signal
- Normally used in large, memory systems.

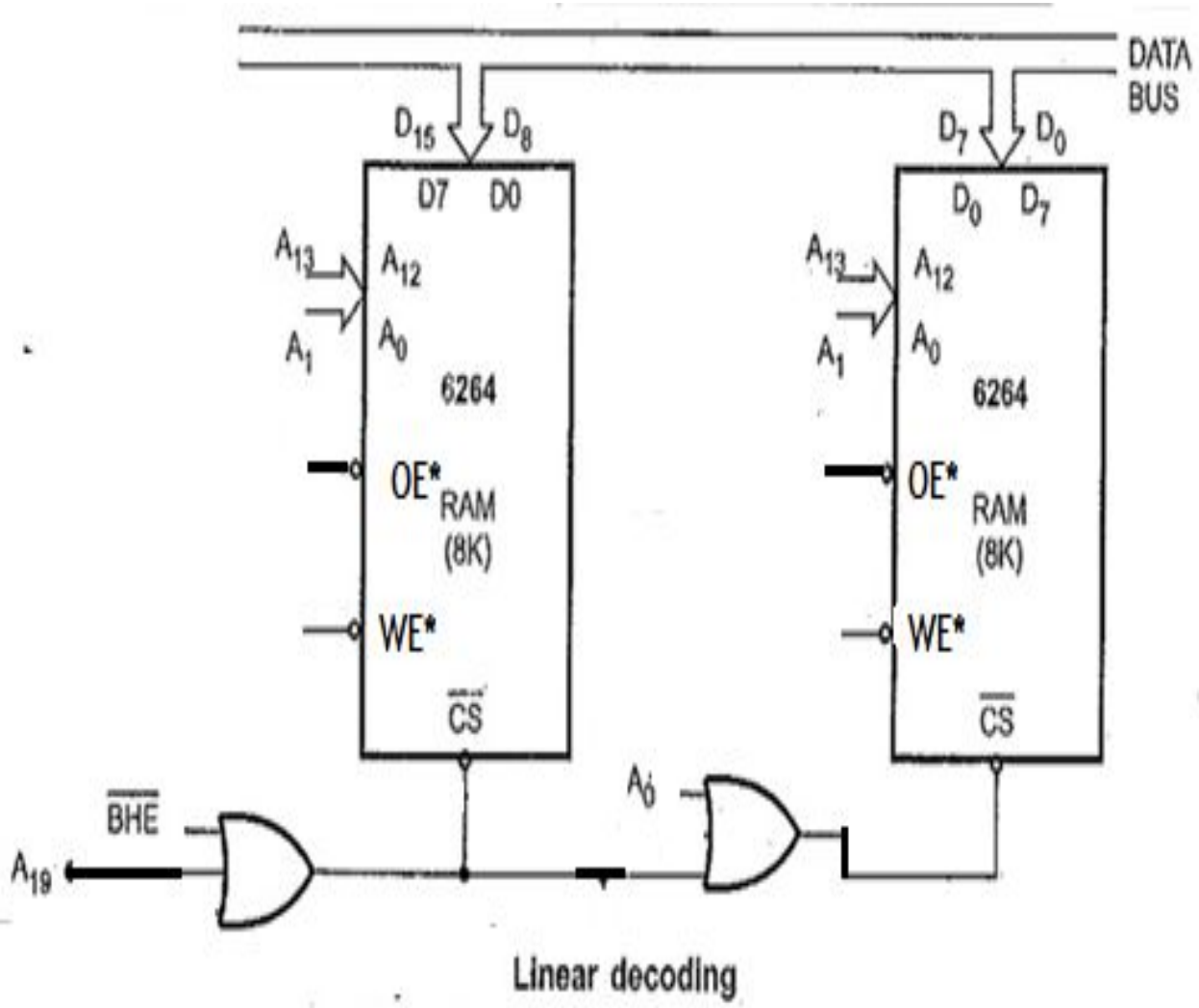
Block decoding (Special Case of full decoding)



Block decoding

- In a microcomputer system the memory array often consists of several blocks of memory chips.
- Each block of memory requires decoding circuit.
- To avoid separate decoding for each memory block special decoder IC is used to generate chip select signal for each block.

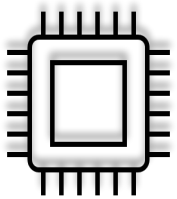
Linear decoding (Partial decoding)



Linear decoding

- In small systems, hardware for the decoding logic can be eliminated, by using only required number of addressing lines (not all). Other lines are simply ignored.
- Ex:The status of A_{14} to A_{18} does not affect the chip selection logic. This gives you multiple addresses (shadow addresses).
- Reduces the cost , but it has drawback of multiple addresses.

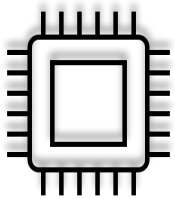
IMPORTANT POINTS TO REMEMBER FOR I/O DESIGNING



- Normally I/O devices are mapped using I/O mapped I/O which means I/O devices are given I/O addresses
- Here I/O addresses can be either 8-bit or 16 bit.
- If the question says direct addressing mode or fixed port addressing, then use an 8-bit address like 80H (A7-A0).
- If the question says indirect addressing or variable port addressing , then use 16-bit address like 0080H (A15-A0).
- If nothing is mentioned, use indirect addressing or variable port addressing
- If memory mapped I/O is asked (Very rare), then remember the following changes

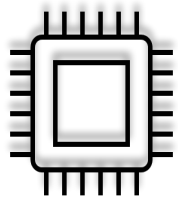
1. Give the I/O device a 20-bit unused memory address like 80000H (A19-A0)
2. Connect MEMR* and MEMW* signals to the I/O device instead of the usual IOR* and IOW* signals

Mapping Techniques

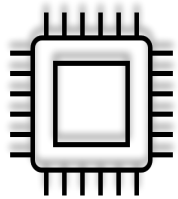


I/O MAPPED I/O	MEMORY MAPPED I/O
I/O device is treated as an I/O device and hence given an I/O address.	I/O device is treated like a memory device and hence given a memory address.
I/O device has an 8 or 16 bit I/O address.	I/O device has a 20 bit Memory address.
I/O device is given IOR* and IOW* control signals	I/O device is given MEMR* and MEMW* control signals
Decoding is easier due to lesser address lines	Decoding is more complex due to more address lines

Mapping Techniques



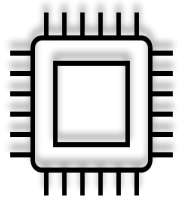
I/O MAPPED I/O	MEMORY MAPPED I/O
Decoding is cheaper	Decoding is more expensive
Works faster due to less delays	More gates add more delays hence slower
Allows max 2^{16} = 65536 I/O devices	Allows many more I/O devices as I/O addresses are now 20 bits.
I/O devices can only be accessed by IN and OUT instructions.	I/O devices can now be accessed using any memory instruction.
ONLY AL/ AX registers can be used to transfer data with the I/O device.	Any register can be used to transfer data with the I/O device.
Popular technique in Microprocessors	Popular technique in Microcontrollers.



You have completed this topic, you should be able to:

Explain operating modes of 8255?

References Used



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