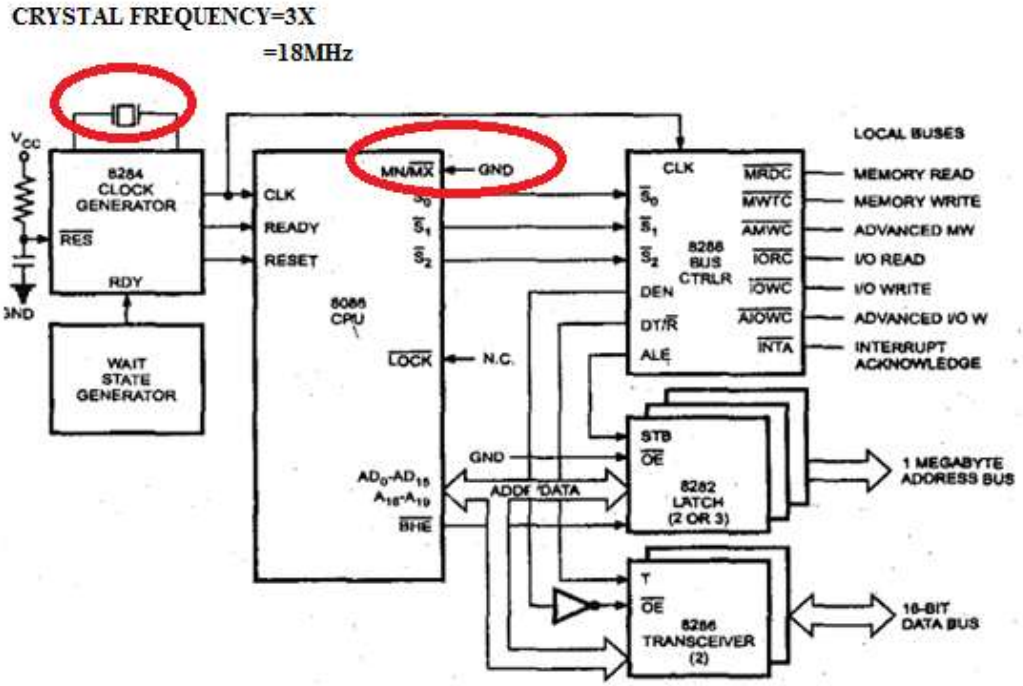
Designing Examples

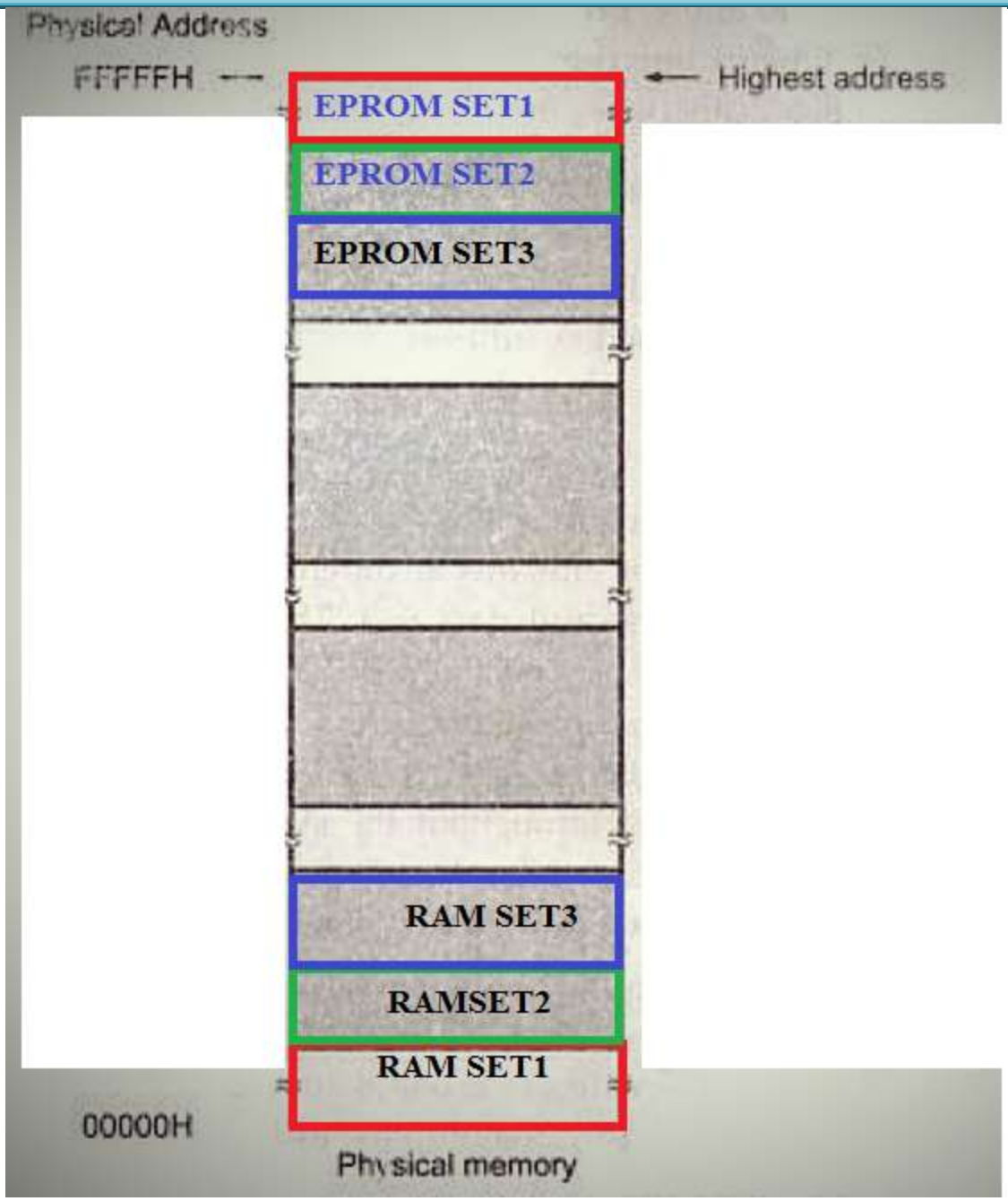
Design an 8086 based Maximum Mode system working at 6 MHz having the following:
32KB EPROM using 16KB chips,
128KB RAM using 32KB chips,
Two 16-bit input and two 16-bit output ports all interrupt driven

Note:
** Every designing problem has three components:
1) Mode of Operation of 8086 processor: Minimum mode or Maximum mode
2) Memory Interfacing: Using ROM and RAM chips (we will construct a Memory Map and interfacing diagram)
3) I/O Interfacing: Using 8255 ICs (we will construct an I/O Map and interfacing diagram)

Solution:
1) Mode of Operation:
Show 8086 max. mode configuration with a crystal of 18 MHz.



Note for variations:
1) If crystal frequency is specified, then show that value directly over crystal; but if operating frequency is specified then crystal frequency=3* operating frequency.
2) If mode of operation not specified then draw minimum mode configuration.
3) Important points in the diagram are: Crystal frequency and MN/MX* pin status.
4) Instead of minimum mode or maximum mode ,interfacing of any chip (IC-8259,IC-8253,IC-8257 can be asked)



2) Memory Calculations:
EPROM:
Required size = 32 KB, Available size = 16 KB
No. of chips required = Required size / Available size =2 chips.
No. of sets required= No. of chips required/ No. of banks= 2/2=1
Set size= Available Chip size x no .of banks= 16 x 2= 32 KB=32 x 1KB= $2^5 \times 2^{10} = 2^{15}$

A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0				**7**				**F**				**F**				**F**			

Ending Address=FFFFFH
Starting address of EPROM is calculated as:
=Ending Address – Set size
=F F F F F H- 7 F F F H=F8000H

Chip	Address	Even Bank	Odd Bank
EPROM Set 1	Starting Address	F8000H	F8001H
	Ending Address	FFFFEH	FFFFFH

No. of address lines required for interfacing is dependent on size of a single available EPROM chip
= 16 KB
= 16 x 1KB = $2^4 \times 2^{10}$
= 2^{14}
= 14 address lines= (A 14 … A1)…note A0 is reserved for banking….IMPORTANT during interfacing

RAM:
Required size = 128 KB, Available size = 32 KB
No. of chips required = Required size / Available size = 4 chips.
No. of sets required= No. of chips required/ No. of banks= 4/2=2
Set size= Available Chip size x no .of banks= 32 x 2= 64 KB=64 x 1KB= $2^6 \times 2^{10} = 2^{16}$

A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0				F				F				F				F			

Starting address of RAM Set1=00000H
Ending address of RAM Set1 is calculated as:
=Starting Address + Set size
=00000 H +0 F F F F H
=0FFFFH

Starting address of RAM Set2= Ending address of RAM Set1+1=10000H
Ending address of RAM Set2 is calculated as:
=Starting Address + Set size
=10000 H +0 F F F F H
=1FFFFH

Chip	Address	Even Bank	Odd Bank
RAM Set 1	Starting Address	00000H	00001H
	Ending Address	0FFFEH	0FFFFH
RAM Set 2	Starting Address	10000H	10001H
	Ending Address	1FFFEH	1FFFFH

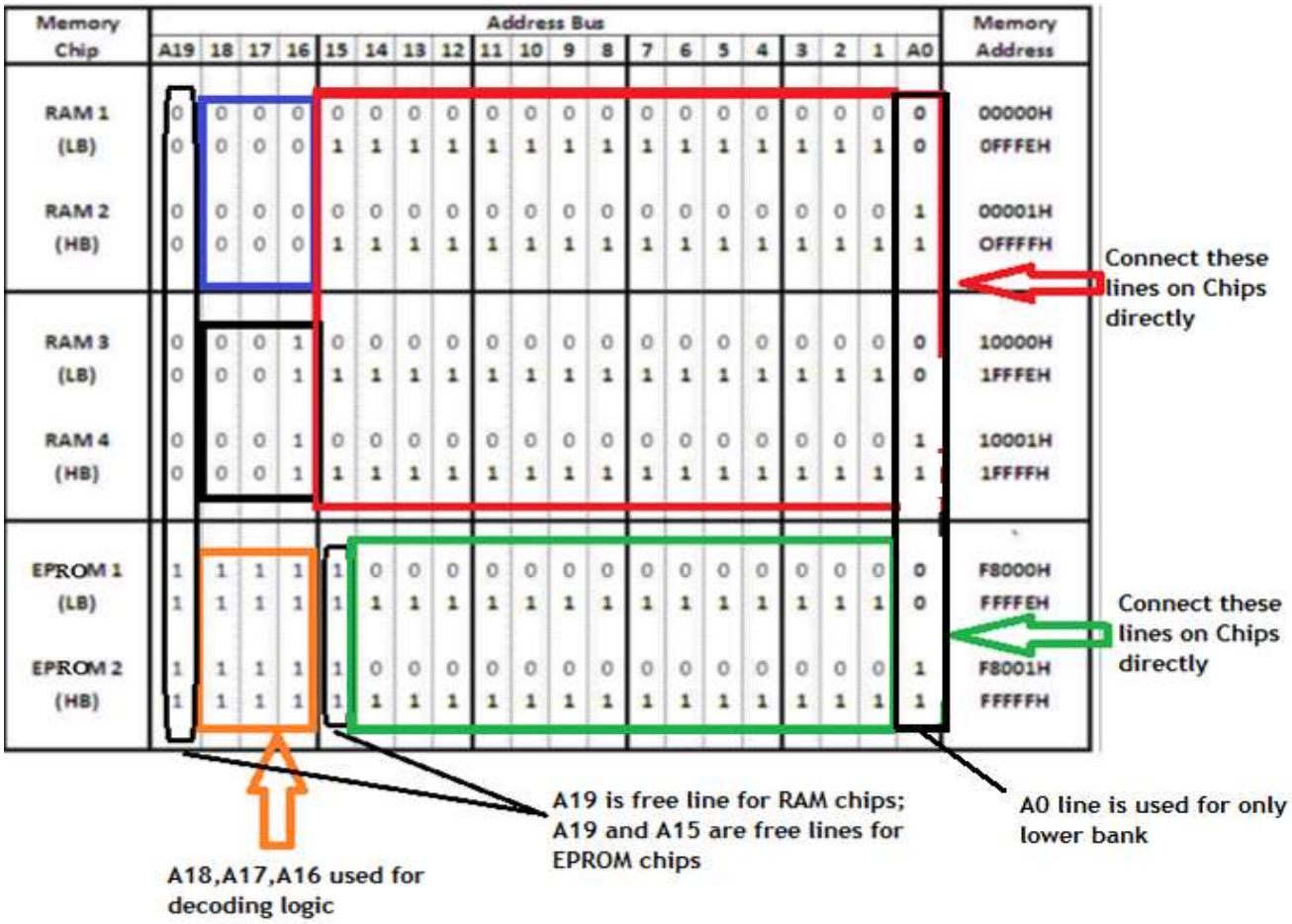
No. of address lines required for interfacing is dependent on size of a single available RAM chip
= 32 KB
= 32 x 1 KB = $2^5 \times 2^{10}$
= 2^{15}
= 15 address lines
= (A15 … A1)…. note A0 is reserved for banking….IMPORTANT during interfacing

MEMORY MAP

Let's construct first the memory map

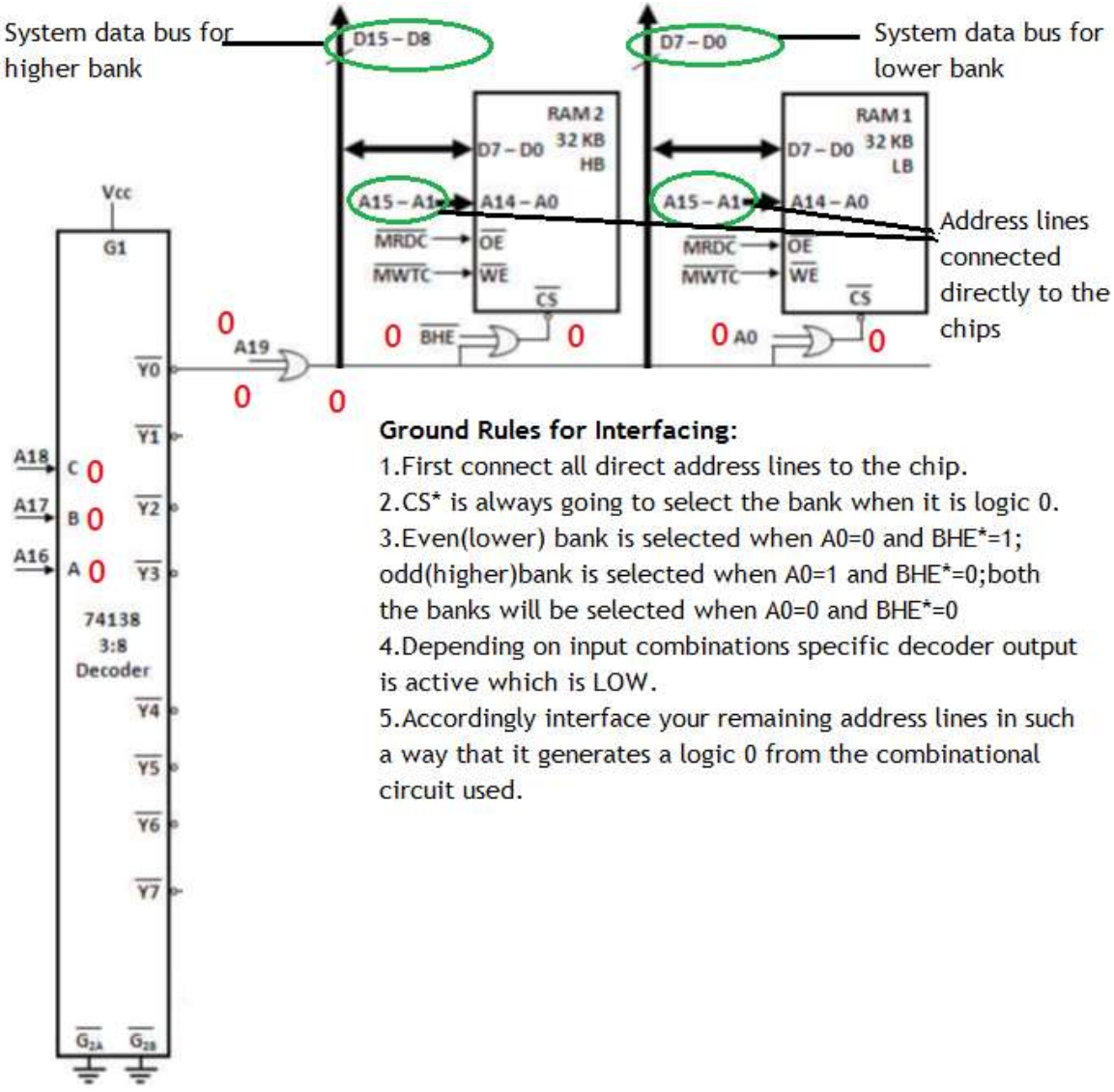
Memory Chip	Address Bus																				Memory Address
	A19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	A0	
RAM 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00000H
(LB)	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0FFFEH
RAM 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	00001H
(HB)	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0FFFFH
RAM 3	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	10000H
(LB)	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1FFFEH
RAM 4	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	10001H
(HB)	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1FFFFH
EPROM 1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	F8000H
(LB)	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	FFFFEH
EPROM 2	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	F8001H
(HB)	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFFFH

Interpreting Memory Map for Memory Interfacing:



Memory Interfacing:
Step1: Interfacing RAM set1

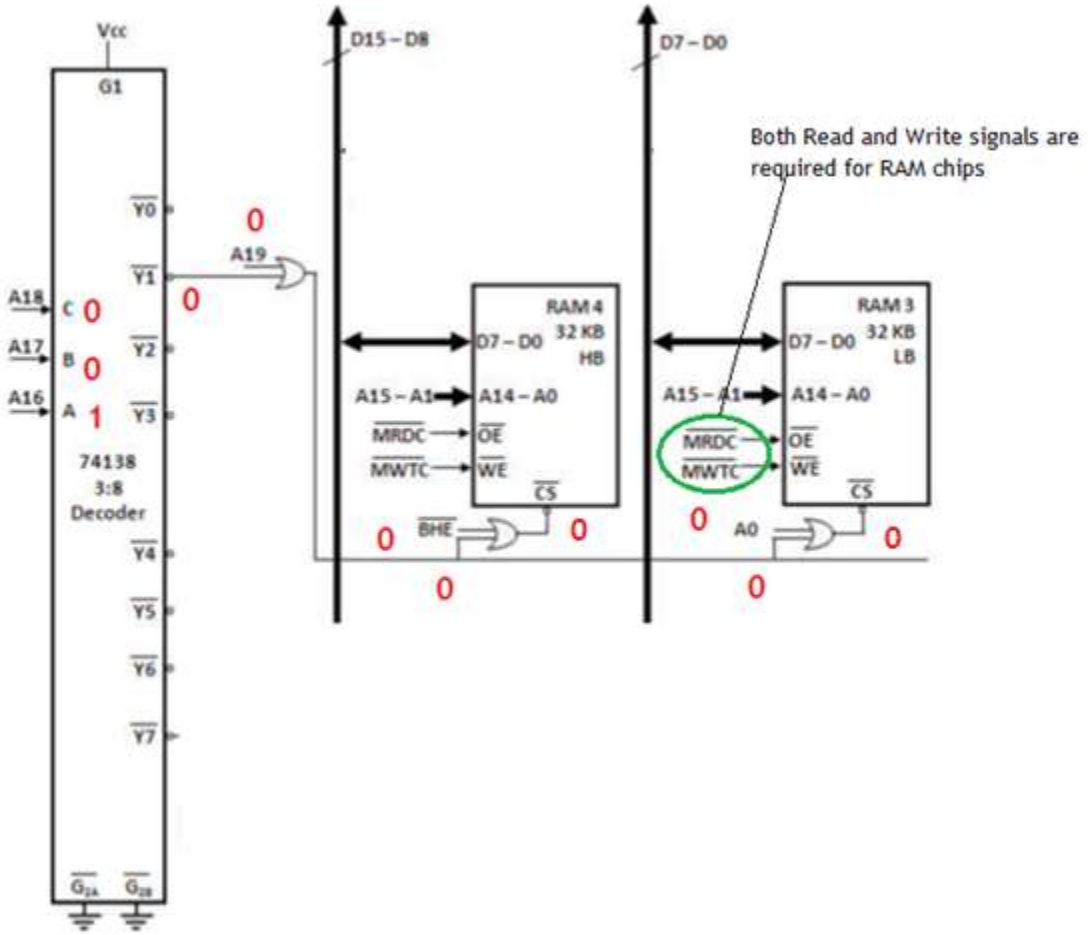
Memory Chip	A19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	A0	Memory Address
RAM 1 (LB)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00000H
	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0FFFEH
RAM 2 (HB)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	00001H
	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0FFFFH



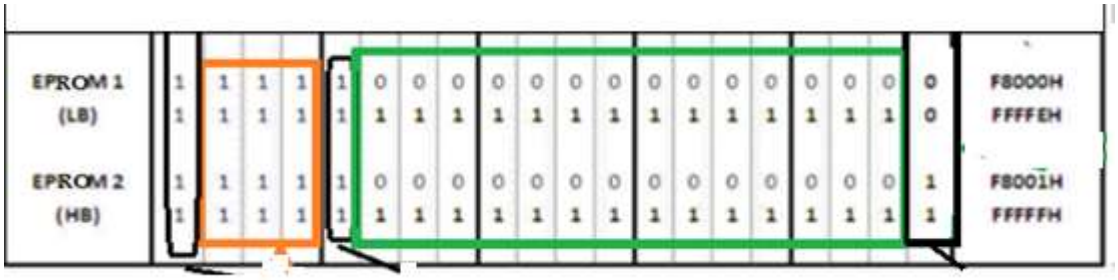
Ground Rules for Interfacing:

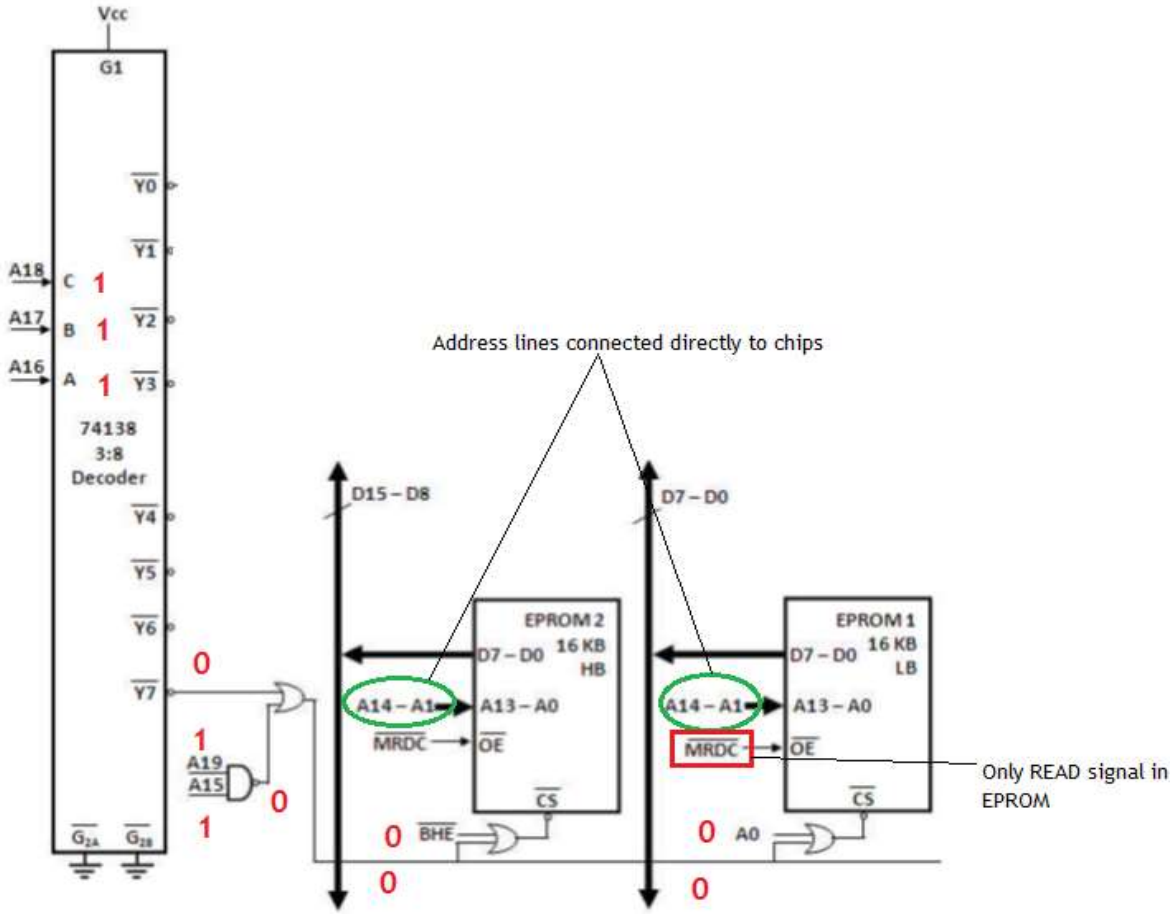
1. First connect all direct address lines to the chip.
2. CS* is always going to select the bank when it is logic 0.
3. Even(lower) bank is selected when A0=0 and BHE*=1; odd(higher)bank is selected when A0=1 and BHE*=0;both the banks will be selected when A0=0 and BHE*=0
4. Depending on input combinations specific decoder output is active which is LOW.
5. Accordingly interface your remaining address lines in such a way that it generates a logic 0 from the combinational circuit used.

Step2: Interfacing RAM set2



Step 3: Interfacing EPROM set1





Note for variations:

1) If application memory is mentioned it means RAM chips and if monitor programming memory mentioned it means EPROM chips.

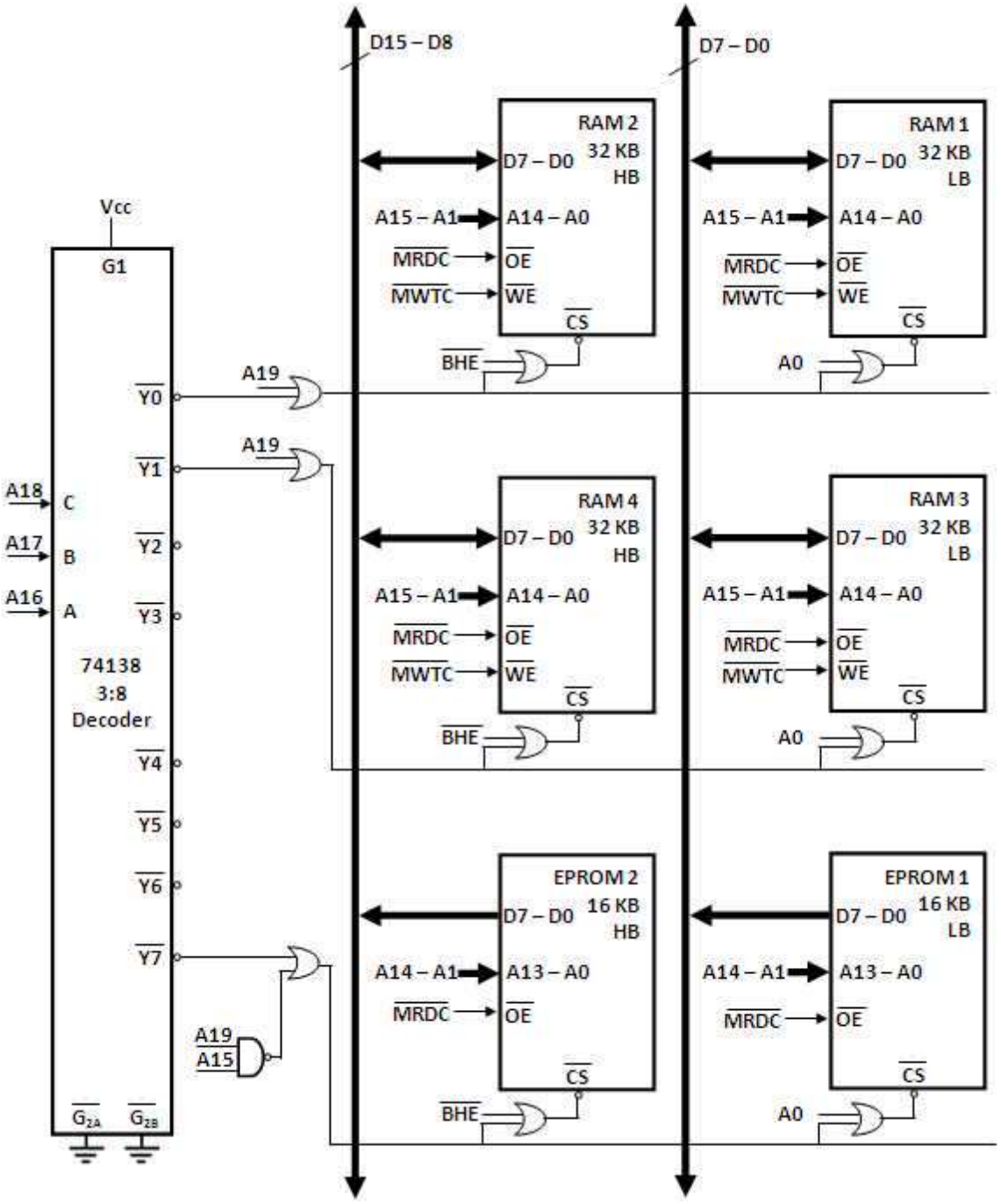
2)Generally we use absolute (full) decoding technique (especially block) for memory interfacing.

3) Instead of the required size sometimes you have IC numbers given ,we need to know their size.

Chips	IC Number	Memory Size(Available Size)
EPROM	2716	2K x 8
	2732	4K x 8
	2764	8K x 8
	27128	16K x 8
	27256	32K x 8
	27512	64K x 8
RAM	6116	2K x 8
	6264	8K x 8
	62256	32K x 8

4) Depending on the address lines used, sometimes we need to use either 2:4 decoder(IC-74139) or3:8 decoder(IC 74138) or 4:16 decoder(74154)
5) Specifications of these decoders are as follows:
2:4 decoder (IC-74139): It has 2 inputs and 4 active low outputs. It has one active low G pin.
3:8 decoder (IC 74138): It has 3 inputs and 8 active low outputs. It has one active high G_1 pin and two active low G_{2A} and G_{2B} pin.
4:16 decoder (74154): It has 4 inputs and 16 active low outputs. It has two active low G_1 and G_2 pin.

Complete Interfacing Diagram (You need to draw this final diagram)



IMPORTANT POINTS TO REMEMBER FOR I/O DESIGNING

- Normally I/O devices are mapped using **I/O mapped I/O** which means I/O devices are given I/O addresses
- Here I/O addresses can be either 8-bit or 16 bit.
- If the question says **direct addressing mode or fixed port addressing**, then use an 8-bit address like 80H (A7-A0).
- If the question says **indirect addressing or variable port addressing**, then use 16-bit address like 0080H (A15-A0).
- If nothing is mentioned, use **indirect addressing or variable port addressing**.
- If memory mapped I/O is asked (Very rare), then remember the following changes
    1. Give the I/O device a 20-bit unused memory address like 80000H (A19-A0)
    2. Connect MEMR* and MEMW* signals to the I/O device instead of the usual IOR* and IOW* signals

I/O Map:

I/O Port	Address Bus																I/O Address
	A15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	A0	
8255 LB																	
Port A	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0060H
Port B	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0062H
Port C	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0064H
C Word	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0066H
8255 HB																	
Port A	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0061H
Port B	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0063H
Port C	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0065H
C Word	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	0067H
8255 LB																	
Port A	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0080H
Port B	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0082H
Port C	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0084H
C Word	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0086H
8255 HB																	
Port A	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0081H
Port B	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0083H
Port C	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	1	0085H
C Word	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0087H

Interpreting I/O map for I/O interfacing via 8255IC.

I/O Port	Address Bus A15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	A0	I/O Address
8255 LB																	
Port A	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0060H
Port B	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0062H
Port C	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0064H
C Word	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0066H
8255 HB																	
Port A	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0061H
Port B	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0063H
Port C	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0065H
C Word	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	0067H
8255 LB																	
Port A	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0080H
Port B	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0082H
Port C	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0084H
C Word	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0086H
8255 HB																	
Port A	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0081H
Port B	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0083H
Port C	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	1	0085H
C Word	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0087H

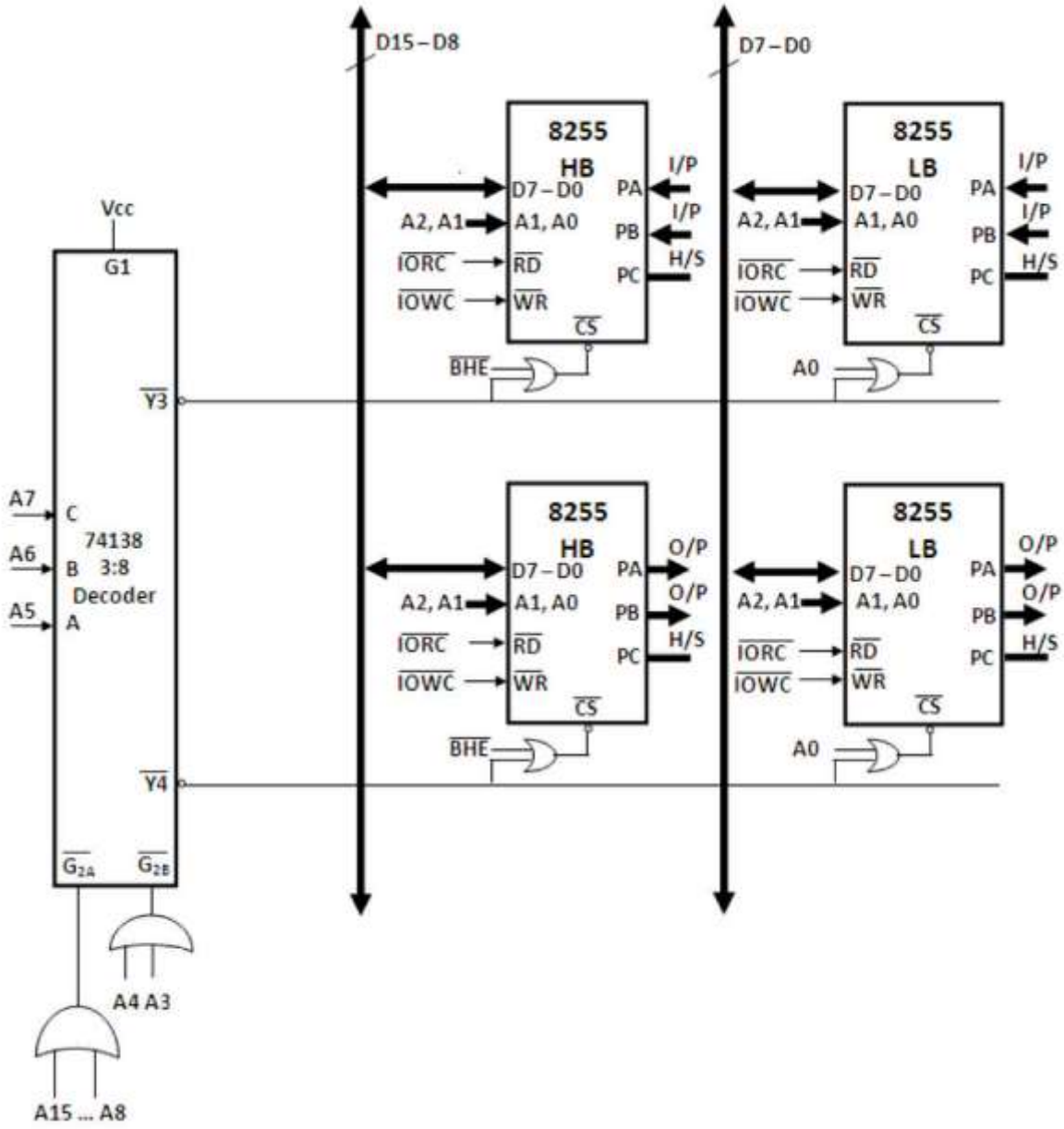
Lines A3 -A4 and A8-A15....are all free lines can be utilized in combinational circuit

Used for decoding; output will be on Y3* and Y4*

A0 always reserved for banking

A1 and A2 of processor are connected to A0 and A1 of 8255 and are used for selection of port A,B,C or CWR

Complete Interfacing Diagram (You need to draw this final diagram)



Possible Variations in I/O mapping:

Port Size, quantity and configuration
Two 16-bit input and two 16-bit output ports (Number of 8255 IC's required =4)
One 16-bit input and one 16-bit output port(Number of 8255 IC's required =2)
Two 8-bit input and two 8-bit output ports(Number of 8255 IC's required =2)
One 8-bit input and One 8-bit output port(Number of 8255 IC's required =1)

Practise Question:
Design an 8086 based system working at 7 MHz having the following:
128KB EPROM using 32KB chips,
32KB RAM using 8KB chips,
Two 8-bit input and two 8-bit output ports all interrupt driven

Solution:
Memory Calculations:
EPROM:
Required size = 128 KB, Available size = 32 KB
No. of chips required = Required size / Available size =4 chips.
No. of sets required= No. of chips required/ No. of banks= 4/2=2
Set size= Available Chip size x no .of banks= 32 x 2= 64 KB=64 x 1KB= $2^6 \times 2^{10} = 2^{16}$

A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0				F				F				F				F			

Ending Address of EPROM set1=FFFFFH
Starting address of EPROM set1 is calculated as:
=Ending Address – Set size
=F F F F F H- F F F F F H=F0000H

Ending Address of EPROM set2= Starting address of EPROM set1 -1=F0000H-1=EFFFFH
Starting address of EPROM set2 is calculated as:
=Ending Address – Set size
=E F F F F H- F F F F F H=E0000H

Chip	Address	Even Bank	Odd Bank
EPROM Set 1	Starting Address	F0000H	F0001H
	Ending Address	FFFFEH	FFFFFH
EPROM Set 2	Starting Address	E0000H	E0001H
	Ending Address	EFFFEH	EFFFFH

No. of address lines required for interfacing is dependent on size of a single available EPROM chip = 32 KB
= 32 x 1KB = $2^5 \times 2^{10}$
= 2^{15}
= 15 address lines= (A 15 … A1)…note A0 is reserved for banking….IMPORTANT during interfacing

RAM:
Required size = 32 KB, Available size = 8 KB
No. of chips required = Required size / Available size = 4 chips.
No. of sets required= No. of chips required/ No. of banks= 4/2=2
Set size= Available Chip size x no .of banks= 8 x 2= 16 KB=16 x 1KB= $2^4 \times 2^{10} = 2^{14}$

A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0				3				F				F				F			

Starting address of RAM Set1=00000H
Ending address of RAM Set1 is calculated as:
=Starting Address + Set size
=00000 H +0 3 F F F H
=03FFFH

Starting address of RAM Set2= Ending address of RAM Set1+1=04000H

Ending address of RAM Set2 is calculated as:
=Starting Address + Set size
=04000 H +0 3 F F F H
=**07FFFH**

Chip	Address	Even Bank	Odd Bank
RAM Set 1	Starting Address	00000H	00001H
	Ending Address	03FFEH	03FFFH
RAM Set 2	Starting Address	04000H	04001H
	Ending Address	07FFEH	07FFFH

No. of address lines required for interfacing is dependent on size of a single available RAM chip
= 8 KB
= 8 x 1 KB = $2^3 \times 2^{10}$
= 2^{13}
= 13 address lines
= (A13 … A1)…. note A0 is reserved for banking….IMPORTANT during interfacing

Draw the memory map further for this question and also interfacing diagram.