MP Assignment 2

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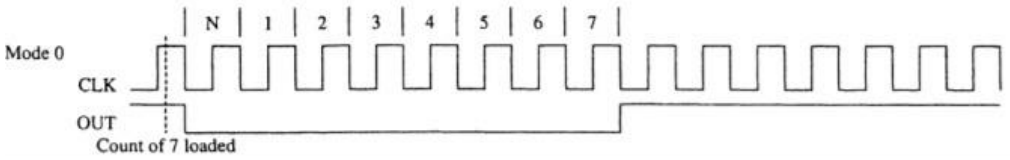
Q1. Explain operating modes of 8253 IC.

8253/54 can be operated in 6 different modes. Following are the operating modes:

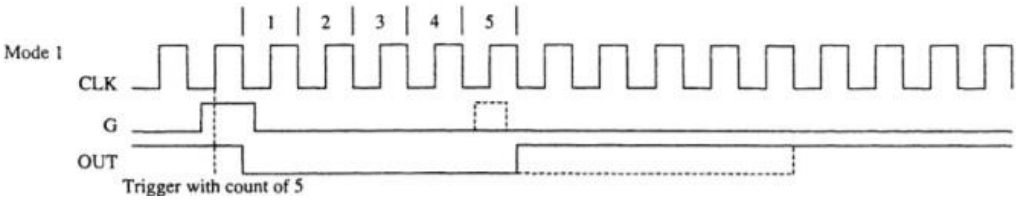
Mode 0 ─ Interrupt on Terminal Count

- It is used to generate an interrupt to the microprocessor after a certain interval.
- Initially the output is low after the mode is set. The output remains LOW after the count value is loaded into the counter.
- The process of decrementing the counter continues till the terminal count is reached, i.e., the count become zero and the output goes HIGH and will remain high until it reloads a new count.
- The GATE signal is high for normal counting. When GATE goes low, counting is terminated and the current count is latched till the GATE goes high again.



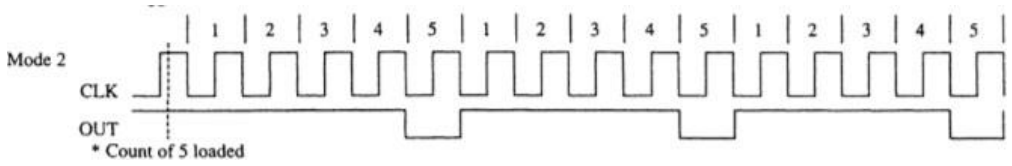
Mode 1 – Programmable One Shot

- It can be used as a mono stable multi-vibrator.
- The gate input is used as a trigger input in this mode.
- The output remains high until the count is loaded and a trigger is applied.



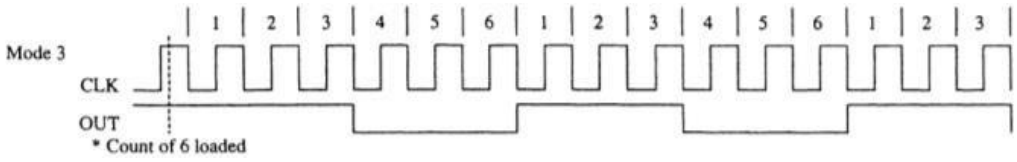
Mode 2 – Rate Generator

- The output is normally high after initialization.
- Whenever the count becomes zero, another low pulse is generated at the output and the counter will be reloaded.



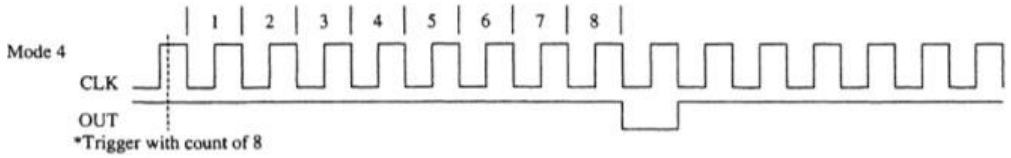
Mode 3 – Square Wave Generator

- This mode is similar to Mode 2 except the output remains low for half of the timer period and high for the other half of the period.



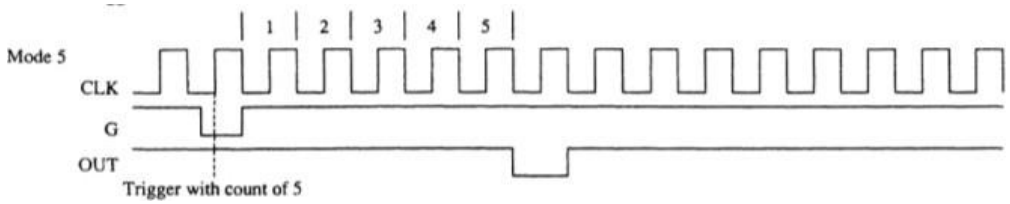
Mode 4 − Software Triggered Mode

- In this mode, the output will remain high until the timer has counted to zero, at which point the output will pulse low and then go high again.
- The count is latched when the GATE signal goes LOW.
- On the terminal count, the output goes low for one clock cycle then goes HIGH. This low pulse can be used as a strobe.



Mode 5 – Hardware Triggered Mode

- This mode generates a strobe in response to an externally generated signal.
- This mode is similar to mode 4 except that the counting is initiated by a signal at the gate input, which means it is hardware triggered instead of software triggered.
- After it is initialized, the output goes high.
- When the terminal count is reached, the output goes low for one clock cycle.



Q2. Design 8086 based system for following specifications:

i) 8086 in minimum mode with clock frequency 5MHz.

ii) 128 KB EPROM using 32KB*8 chips

iii) 32 KB RAM using 16KB*8 chips

Q2) Design 8086 based system for following specifications:
i) 8086 in minimum mode with clock frequency 5MHz
ii) 128 Kb EPROM using 32Kb * 8 chips
iii) 32 Kb RAM using 16 Kb * 8 chips.

Ans →

1) Mode of operation
minimum mode
crystal frequency = 3 × clock frequency
= 3 × 5
= 15 MHz

2) Memory calculation
EPROM
Required size = 128 Kb
Available size = 32 Kb
No. of chips req = Req size / Available size
= 128 / 32 = 4 chips
No. of sets req = No. of chips req / No. of banks
= 4 / 2 = 2 sets
set size = Available size × no. of banks
= 32 × 2 = 64 Kb
= 64 × 1 Kb
= $2^6 \times 2^{10}$
= 2^{16} memory locations for EPROM.

16 address lines preserved for EPROM ($A_0 - A_{15}$)

$A_0 - A_{15} \rightarrow 1$	0000	1111	1111	1111	1111
$A_{16} - A_{19} \rightarrow 0$	0	F	F	F	F

OFFFF H ⟶ max size of set

Set 1 Ending address = FFFFF H

Set 1 Starting address = Ending address - set size
= FFFFF H - OFFFF H
= F0000 H

Set 2 Ending address = Starting address of set 1 - 1
= F0000 H - 1 = EFFFF H

Set 2 Starting address = Ending address - set size
= EFFFFH - OFFFF H
= E0000 H

Chip	Address	Even bank	Odd bank
EPROM set 1	Starting	F0000H	F0001 H
	Ending	FFFFE H	FFFFF H
EPROM set 2	starting	E0000 H	E0001 H
	Ending	EFFFE H	EFFFF H

No. of address lines required for interfacing
= Available size of EPROM
= 32 Kb
= $2^5 \times 2^{10}$ Kb
= 2^{15} = 15 address lines (A_1 - A_{15})

A_0 reserved for banking.

(processor) A_1 - A_{15} ↔ A_0 - A_{14} (EPROM)

RAM :-

Required size = 32 Kb
Available size = 16 Kb
No. of chips req = Req size / Avail size
= 32 / 16 = 2 chips
No. of sets req = Avail chip size / no. of banks.
~~= 2×2 = 4~~ = 2/2 = 1

set size = Available chip size x no. of banks.

= 16 x 2 = 32 Kb

= $2^5 \times 2^{10}$

= 2^{15}

$A_0 - A_{14} \rightarrow 1$	0000	0111	1111	1111	1111
$A_{15} - A_{19} \rightarrow 0$	0	7	F	F	F

Maximum set size = 07FFFH

Starting address of RAM set 1 = 00000 H

Ending address = starting address + set size

= 00000 H + 07FFF H

= 07FFF H

Chip	Address	Even bank	Odd bank
RAM	Starting	00000H	00001 H
	Ending	~~0F~~ 07FFEH	07FFF H

No. of address lines required for interfacing

= size of available RAM

= 16 KB

= $2^4 \times 2^{10}$

= 2^{14} = 14 address lines ($A_1 - A_{14}$)

A_0 reserved for banking

processor ($A_1 - A_{14}$) $\longleftrightarrow$ ($A_0 - A_{13}$) RAM

Memory map :-

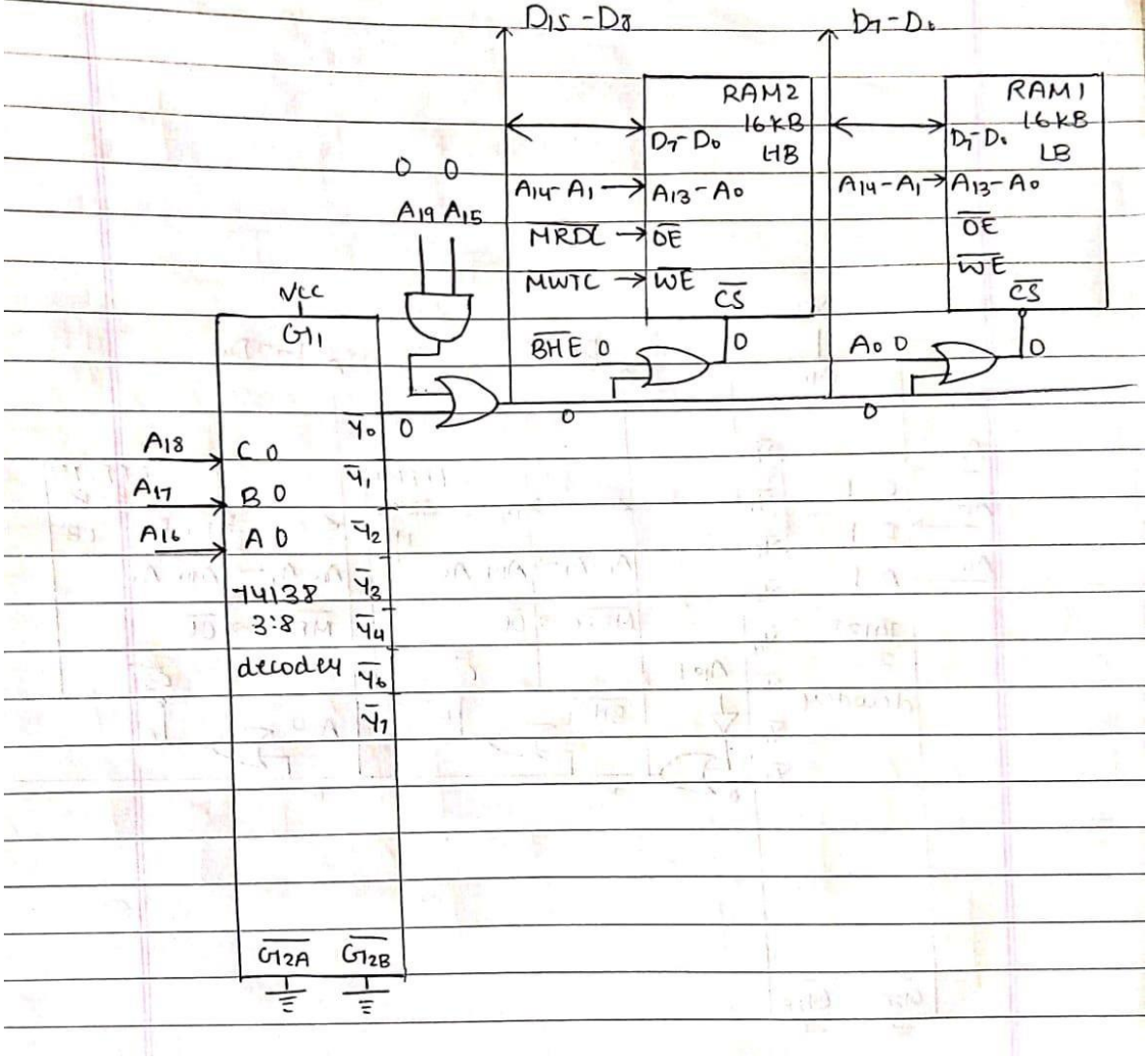
Memory chip	Address Bus					Memory Address
RAM 1	0000	0000	0000	0000	0000	00000 H
(LB)	0000	0111	1111	1111	1111	07FFE H
RAM 2	0000	0000	0000	0000	0000	00001 H
(HB)	0000	0111	1111	1111	1111	07FFF H
EPROM 1	1111	0000	0000	0000	0000	F0000 H
(LB)	1111	1111	1111	1111	1110	FFFFE H
EPROM 2	1111	0000	0000	0000	0001	F0001 H
(HB)	1111	1111	1111	1111	1111	FFFFF H
EPROM 3	1110	0000	0000	0000	0000	E0000 H
(LB)	1110	1111	1111	1111	1110	EFFFE H
EPROM 4	1110	0000	0000	0000	0001	E0001 H
(HB)	1110	1111	1111	1111	1111	EFFFF H

A_0 -> Banking

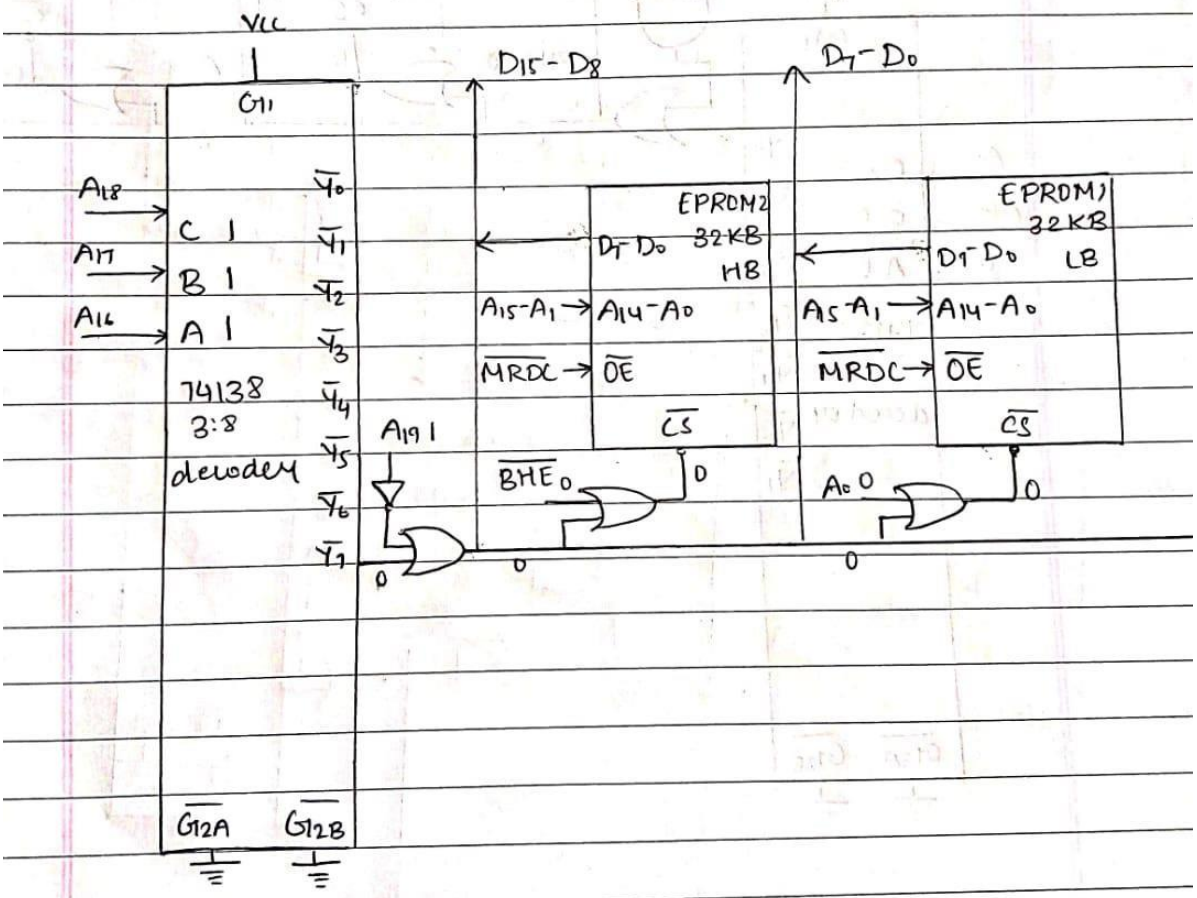
A_{15}, A_{16}, A_{17}, A_{18}, A_{19} —> free for RAM

A_{16}, A_{17}, A_{18}, A_{19} —> free for EPROM

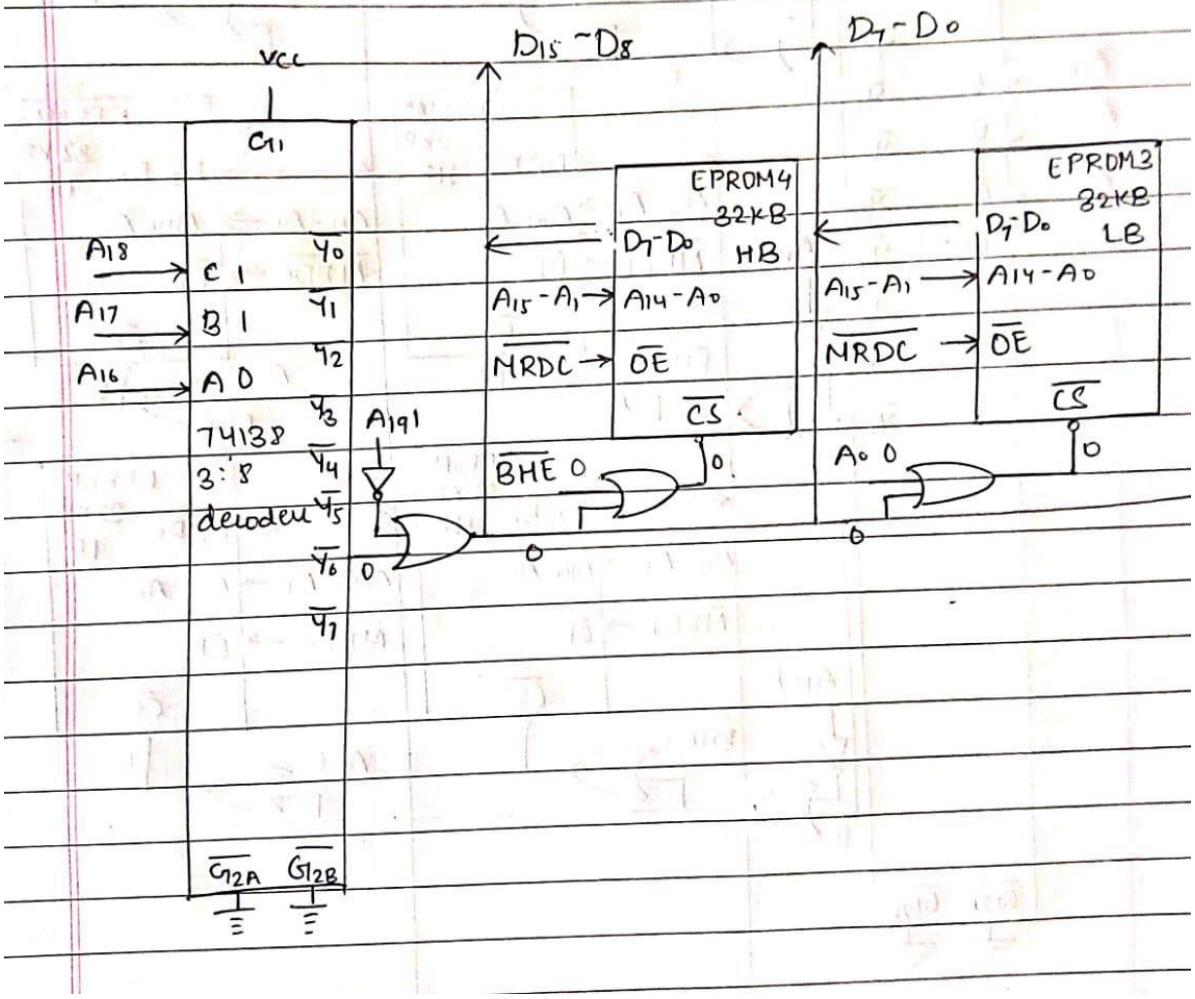
Interfacing RAM set 1



Interfacing EPROM set 1



Interfacing EPROM set 2



Q3. Difference between linear and absolute decoding techniques.

Absolute decoding	**Linear decoding**
All higher address lines are decoded to select the memory or I/O device.	Few higher address lines are decoded to select the memory or I/O device.
More hardware is required to design decoding logic.	Hardware required to design decoding logic is less and sometimes it can be eliminated.
Higher cost for decoding circuit.	Less cost for decoding circuit.
No multiple addresses.	It has a disadvantage of multiple addresses. (Shadow addresses)
Used in large systems.	Used in small systems.