MP Assignment 2

Name: Denvin Davis Roll no.: 07

Q1. Explain operating modes of 8253 IC.

8253/54 can be operated in 6 different modes. Following are the operating modes:

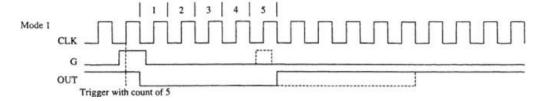
Mode 0 — Interrupt on Terminal Count

- It is used to generate an interrupt to the microprocessor after a certain interval.
- Initially the output is low after the mode is set. The output remains LOW after the count value is loaded into the counter.
- The process of decrementing the counter continues till the terminal count is reached, i.e., the count become zero and the output goes HIGH and will remain high until it reloads a new count.
- The GATE signal is high for normal counting. When GATE goes low, counting is terminated and the current count is latched till the GATE goes high again.



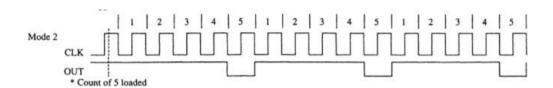
Mode 1 – Programmable One Shot

- It can be used as a mono stable multi-vibrator.
- The gate input is used as a trigger input in this mode.
- The output remains high until the count is loaded and a trigger is applied.



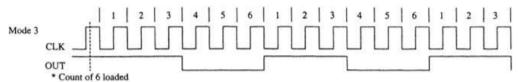
Mode 2 – Rate Generator

- The output is normally high after initialization.
- Whenever the count becomes zero, another low pulse is generated at the output and the counter will be reloaded.



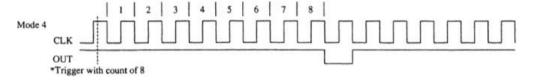
Mode 3 – Square Wave Generator

• This mode is similar to Mode 2 except the output remains low for half of the timer period and high for the other half of the period.



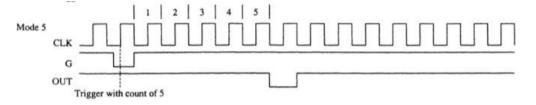
Mode 4 – Software Triggered Mode

- In this mode, the output will remain high until the timer has counted to zero, at which point the output will pulse low and then go high again.
- The count is latched when the GATE signal goes LOW.
- On the terminal count, the output goes low for one clock cycle then goes HIGH. This low pulse can be used as a strobe.



Mode 5 – Hardware Triggered Mode

- This mode generates a strobe in response to an externally generated signal.
- This mode is similar to mode 4 except that the counting is initiated by a signal at the gate input, which means it is hardware triggered instead of software triggered.
- After it is initialized, the output goes high.
- When the terminal count is reached, the output goes low for one clock cycle.



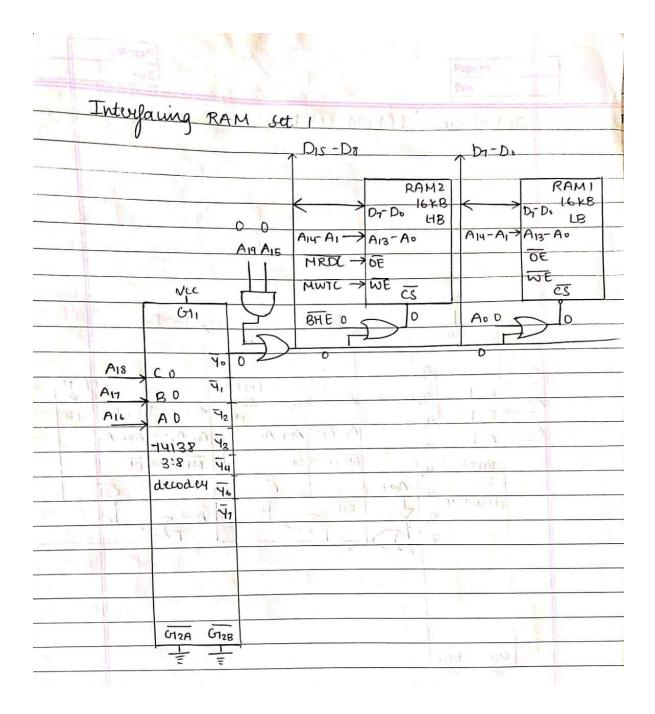
- Q2. Design 8086 based system for following specifications:
 i) 8086 in minimum mode with clock frequency 5MHz.
 ii) 128 KB EPROM using 32KB*8 chips
 iii) 32 KB RAM using 16KB*8 chips

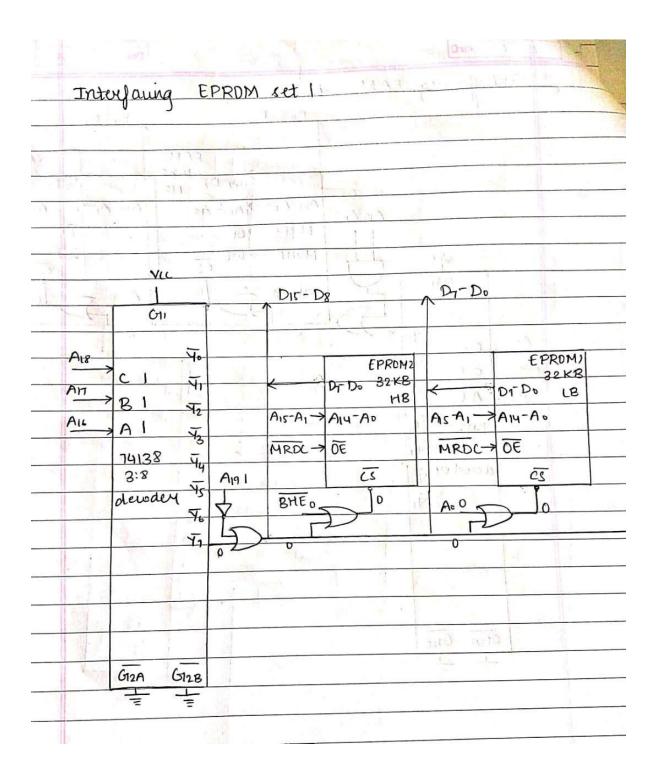
40	Design 8086 based system for following specifications:
Q2)	Design 8086 based system vor correct of trequency 5MHz i) 8086 in minimum mode with clock frequency 5MHz
	11 ROSS in minimum made and
	ii) 128 Kb EPROM using 32Kb* 8 chips
Δ.	(ii) 32 kb RAM wing 168 kb * 8 chips
Ans ->	1) Mode of operation
	minimum mode
	crystal frequency = 3 x clock frequency
	= 3×5
	= 15 MHz
The letter of th	2) Memory calculation
	EPROM
	Required size = 128 Kb
	Available size = 32 Kb
	No. of chips reg = Req size / Available size
	= 128/32 = 4 chips
	No. of sets reg = No. of chips reg / No. of banks
	= 4/2 = 2 sets
	set size = Available size x no. of banks
	= 32 x 2 = 64 Kb
	= 64 x 1 Kb
	= 26 x 210
	= 216 memory locations for EPROM.
	WELL STO DOF ETHORY
	16 address lines preserved for EPROM (Ao-Ais)
	$A - D \rightarrow 1$
	HIR-4114-20 1014 14 1
	OFFFF H -> man size of set
	and the second s
1	

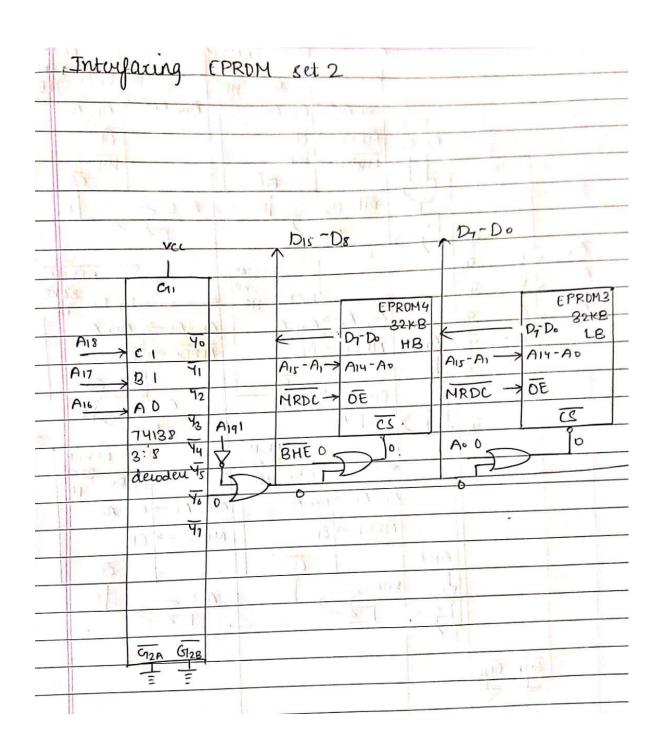
Ending address - set size =FFFFF H - OFFFF H = F0000 H Ending address = Otarting address of set 1 - 1 = F0000 H - 1 = EFFFF H = F0000 H - 1 = EFFFF H Otarting address = Ending address - set size = FFFFFH - OFFFF H = E0000 H Chip Address Even bank Odd bank 1 set 1 starting F0000 H Ending FFFFE H Ending FFFFE H Ending EFFFE H ENDING EFF	5et 1	Ending address Starting address	= FFFFF H			
Ending address = Starting address of set 1 - 1 = F0000 H - 1 = EFFFF H Starting address = Ending address - set size = EFFFFH - OFFFF H = E0000 H Chip Address Even bank Odd bank 1 set 1 Starting F0000H F0001H Ending FFFFEH FFFFFH 1 set 2 Starting E0000 H E0001H Ending EFFFEH EFFFFH address lines required for interfacing = Available size at EPROM = 32 Kb = 25 × 210 Kb = 26 × 210 Kb = 27 × 210 Kb = 28 × 210 Kb = 29 × 210 Kb = 210 = 15 address lines (A1 - A15) = Required Size = 32 Kb Alable Size = 16 Kb Chips req = Req size / Avail Size = 32 / 16 = 2 chips		and tells - Ending address - set size				
tricking address = Starting address of set 1 - 1 = F0000 H - 1 = EFFFF H Starting address = Ending address - set size = FFFFFH - OFFFF H = E0000 H Chip Address Even bank Odd bank I set 1 Starting F0000H F0001H Ending FFFFEH FFFFFH 1 set 2 Starting E0000 H E0001H Ending EFFFEH EFFFFH address lines required for interducing = Available size at EPROM = 32 Kb = 25 × 210 Kb = 25 × 210 Kb = 25 × 13 address lines (AI-AID) streetved for banking. cocessor) PI-AID \rightarrow AD-AIM (EPROM) street size = 16 Kb lable size = Required favoil size = 32/16 = 2 chips			TIFFF H - OF	FFF H		
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Starting address = Ending address - set size = FFFFFH - OFFFF H = E0000 H Chip Address Even bank Odd bank 1 set 1 Starting F0000H F0001H Ending FFFFEH FFFFFH 1 set 2 Starting E0000 H E0001H Ending EFFFEH EFFFFH address lines required for interducing = Available size at EPROM = 32 Kb = 25 × 210 Kb = 215 = 15 address lines (A1-A15) brocessor) A1-A15 A6-A14 (EPROM) cocessor) A1-A15 A6-A14 (EPROM) cocessor) A1-A15 A6-A14 (EPROM) cocessor) cocessor = 16 Kb d chips req = Req size / Avail size = 32/16 = 2 chips		g duarers =				
Etip Address Even bank Odd bank Set 1 Starting F0000H Ending FFFFEH Ending Ecooo H Ending EFFFEH Ending EFFFEH Ending EFFFEH ENTER H Set 2 Starting Ecooo H Ending EFFFEH ENTER H ENT	jet 2 Sto	= F0000 H - 1 = FFFFF H				
Etip Address Even bank Odd bank I set 1 Starting F0000H F0001H Ending FFFFEH FFFFFH Det 2 Starting E0000 H E0001H Ending EFFFEH EFFFFH Det address lines required for interfacing = Available size of EPROM = 32 Kb = 20 × 210 Kb = 20 × 210 Kb = 20 × 10 Kb = 20 × 20 Kb		= Ending address - set size				
Chip Address Even bank Odd bank 1 set 1 Starting FOOOOH FOOOIH Ending FFFFEH FFFFFH 1 set 2 Starting EOOOO H EOOOIH Ending EFFFEH EFFFFH 2 address lines required for interfacing = Available size of EPROM = 32 Kb = 25 × 210 Kb = 215 = 13 address lines (A-AIS) 2 reserved for banking. Accessor) AI-AIS AB-AIH (EPROM) 3- 1 ired size = 32 Kb I able size = 16 Kb I chips req = Req size / Avail size = 32 / 16 = 2 chips				rtt M		
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Ending FFFFE H Ending FFFFE H Set 2 starting E0000 H Ending EFFFE H ENDING	Chip	Address	Even bank	Odd bank		
Ending FFFFEH Set 2 Starting E0000 H Ending EFFFEH EFFFFH address lines required for interdacing = Available size at EPROM = 32 Kb = 25 × 210 Kb = 26 × 210 Kb = 27 = 15 actoress lines (A1-A15) Accessor) A1-A15 ↔ A0-A14 (EPROM) Accessor) A1-A15 ↔ A0-A14 (EPROM) B1-A15 ↔ A0-A14 (EPROM) B1-A15 ← A15 ← A16 ← A16 Dize = 32 Kb Achips req = Req size / Avail size = 32 / 16 = 2 chips	EPROM set 1					
Ending EFFFEH EFFFEH address lines required for interducing = Available size of EPROM = 32 Kb = 25 × 210 Kb = 25 × 210 Kb = reserved for banking. Docessor) FiAis (EPROM)		Ending	FFFFEH	FFFFFH		
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address lines required for interfacing = Available size of EPROM = 32 Kb = 25 × 210 Kb = 25 = 15 address lines (A1-A10) > reserved for banking:		Ending	EFFFE H	EFFFF H		
lable size = 32 Kb lable size = 16 Kb d chips req = Requize / Avail size = 32/16 = 2 chips	= 2° = 2°	$5 \times 2^{10} \text{ Kb}$ $5 = 15 \text{ address}$ $d \text{ for banking}$				
dired size = 32 Kb Nable size = 16 Kb d chips req = Req size / Avail size = 32/16 = 2 chips	(processor) FII-FIIS					
Nable size = 16 Kb d chips req = Reg size / Avail size = 32/16 = 2 chips	RAM :-					
dable size = 16 Kb d chips req = Requize / Avail size = 32/16 = 2 chips	Avilable Size = 16 Kb					
d chips req = Require / Hvail size = 32/16 = 2 chips						
		rea = Reg si	ze/Avail size			
at sets rea = Avail chip sire/o no. of banks.	No- of chips	= 32/1	6 = 2 chip3			
of sets teg = float chip size / = $2/2 = 1$	No- od chips	= 32/1	chia size la no	of banks.		

	set size = Available chip size x no. at banks.					
	= 16 x 2 = 32 Kb					
	= 2 ⁵ x 2 ¹⁰					
	= 215					
	$A_0 - A_{14} \rightarrow 1$ 0000 0111 1111 1111 F					
	A15-A19 > 0 0 7 1 + 1 T					
	Maximum set size = O7FFFM					
	Starting address of RAM set 1 = 00000 H					
	Ending address = starting address + set size					
	= 00000 H + 07FFFH					
	= OTFFF H					
	Diller Frenchank Odd bank					
	Chip Address Even bank Odd bank					
	RAM Starting 00000H 00001H Ending #07FFEH 07FFFH					
	TENANTY OFFICE OFFICE OF THE PERSON OF THE P					
	1 11 0					
	No of address lines required for intérfacing					
	= oize of available RAM					
	= 16 KB					
	= 214 = 14 address lines (FI - FII)					
1	As reserved for banking					
-	processor (A, -A14) (-> (Ao-A13) RAM					
1						
-						
-						
1						

Memor						
Memory	map:					4
Memory chip		Address	Bus			Memory Address
RAM 1	0000	1 0000	0000	0000	0000	00000 H
(61)	0000	01110	1111	1111	1111	OTFFE H
			NI STORY	- 642		0(11,12,11
RAM 2	0000	0000	0000	0000	0000	000014
(HB)	0000	0111	1111	111-1	1111	OTFFFH
		THE PLANT	A Ribo			
EPROMI	1111	0000	0000	0000	0000	F0000 H
(48)	(1 1 1	1111	1111	1111	1116	FFFFEH
	Mand his	* 100	m 1 1998	1 2/39	Jeff Hills	-
EPROM 2	1111	0000	0000	0000	0001	F0001 H
(HB)	1111	1111	1111	1111	Vill	FFFFF H
EPROM 3	1110	0000	, 0000	0000	0000	E0000 H
(rB)	1110	1111	1111	(111	1110	EFFFEH
				- Color	4111111	
EPROM 4	(110	0000	0000	0000	0001	E0001 H
(HB)	1110	1111	1111	(1()	- (11)	EFFFFH
			The Market	4242,4	harman .	
Ao -> Banking						
Aig, Aig, Aig, Aig -> Free for RAM						
AIG, AIT, AIB, AIQ -> Free for ES EPROM						
, (6	1 13					BER BEREIT







Q3. Difference between linear and absolute decoding techniques.

Absolute decoding	Linear decoding
All higher address lines are decoded to select the memory or I/O device.	Few higher address lines are decoded to select the memory or I/O device.
More hardware is required to design decoding logic.	Hardware required to design decoding logic is less and sometimes it can be eliminated.
Higher cost for decoding circuit.	Less cost for decoding circuit.
No multiple addresses.	It has a disadvantage of multiple addresses. (Shadow addresses)
Used in large systems.	Used in small systems.