Peter Hofstee

Cell Processor: Motivation, Architecture, Design, Programming and Applications

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The *Cell processor*, jointly developed by the *Sony-Toshiba-IBM* partnership, is a non-homogeneous chip multiprocessor intended for general-purpose applications, with a particular emphasis on multimedia performance. *Cell* combines a *64-bit Power Architecture™* core with 8 *Synergistic Processors*. In many cases, it delivers over an order of magnitude more performance than conventional PC processors. *Cell* achieves this performance and power efficiency by a new division of labor between the *Power* core and the *Synergistic Processors*. *Cell* allows a wide variety of programming models, a selection of which will be presented in this talk. We will also discuss applications which fit the *Cell* processor particularly well, and areas of further exploration.

Watch the video online!

Dr. H. Peter Hofstee is chief architect of the Cell Synergistic Processor and Cell chief scientist. He received his Ph.D. in computer science from the California Institute of Technology (Caltech) in 1995, and joined the Caltech faculty in 1995 and 1996. In 1996 he joined the IBM Austin research laboratory where he helped create the first GHz CMOS processor. Between 1997 and 2000, he worked on several other high-frequency server processors. In 2000, Hofstee helped create the concept for Cell, helping found the Sony-Toshiba-IBM design center in spring 2001. His current interest focuses on application of the Cell processor beyond the gaming space and on future Cell designs.

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