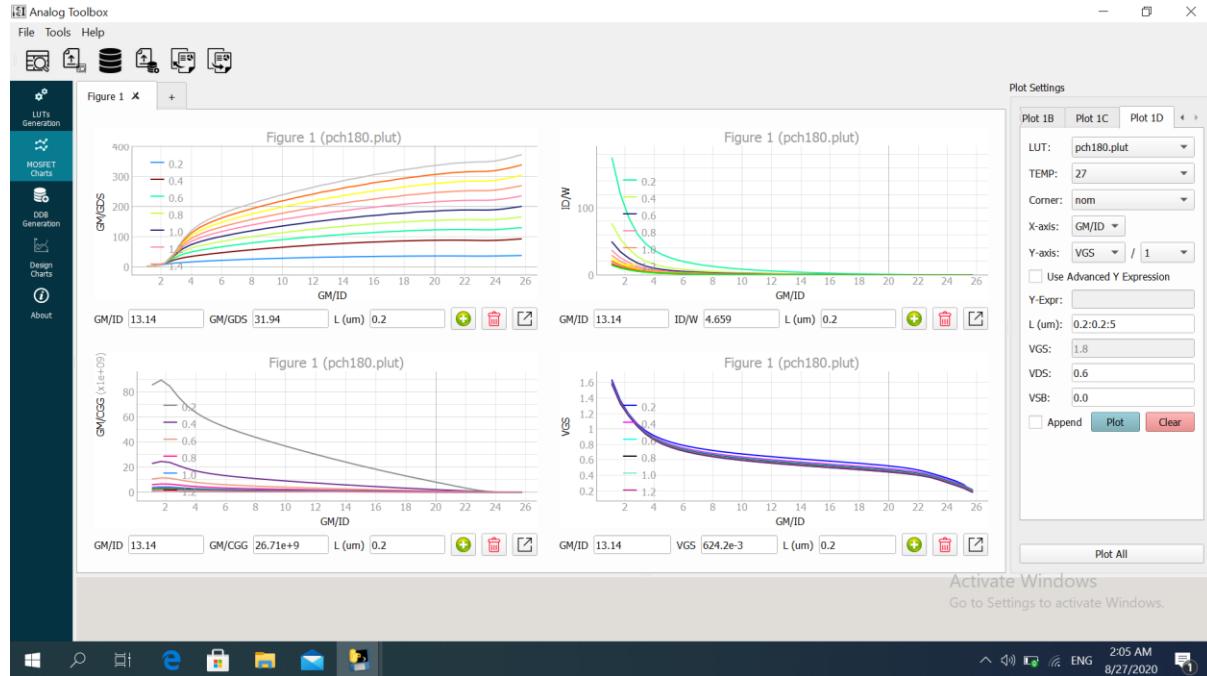


Mini Project: Fully-Differential Folded Cascode OTA

■ Part 1: gm/ID design charts

Using $L = 0.2\mu m$: $0.2\mu m$: $2\mu m$ & $VDS = \frac{VDD}{3} = 0.6$



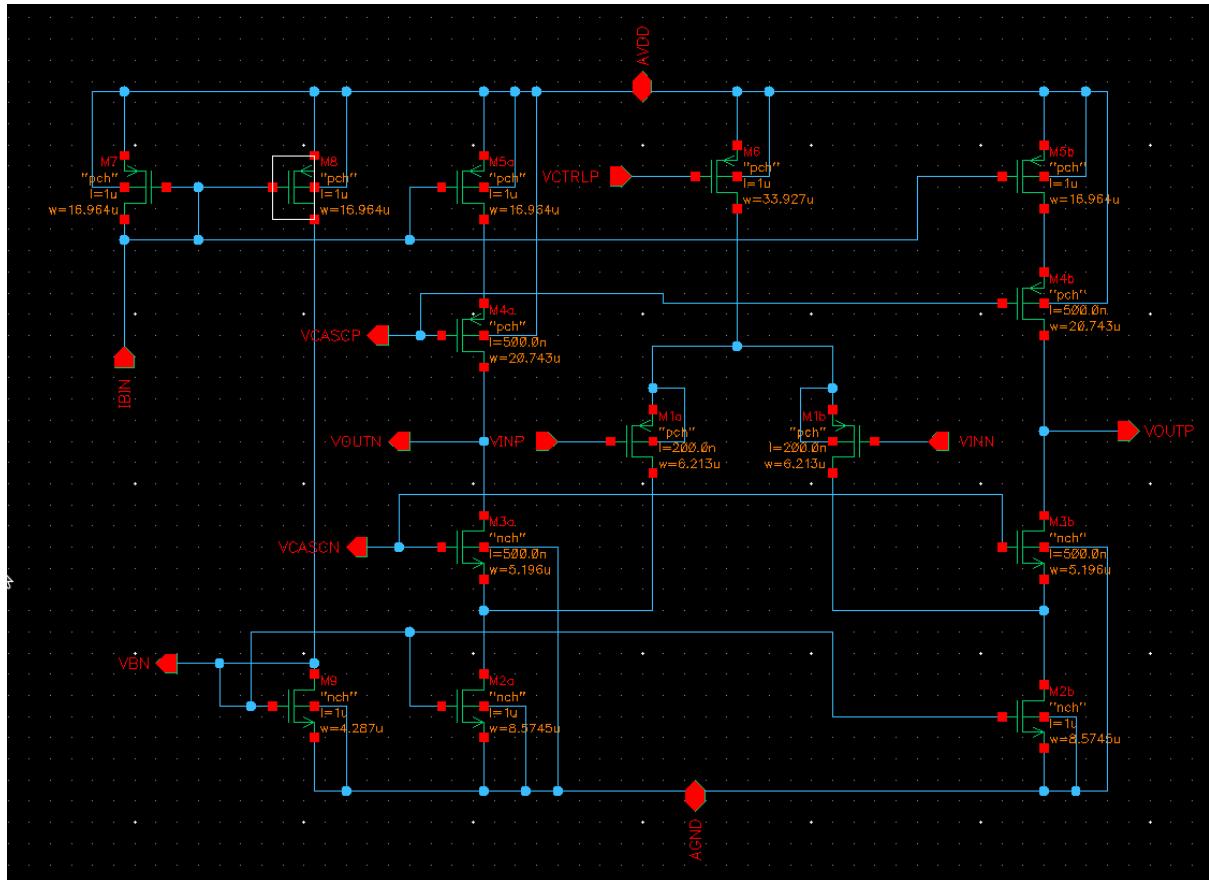
- $g_m r_o \left(\frac{g_m}{g_{ds}} \right)$ & $\frac{I_D}{W}$ & $\frac{g_m}{C_{gg}}$ & V_{GS} for PMOS



- $g_m r_o \left(\frac{g_m}{g_{ds}} \right)$ & $\frac{I_D}{W}$ & $\frac{g_m}{C_{gg}}$ & V_{GS} for NMOS

▪ Part2: OTA Design

spec	value
Supply voltage	1.8 v
Closed loop gain	2
Phase margin	$\geq 70^\circ$
OTA current	$\leq 80\mu\text{A}$
CMFB circuit current	$\leq 40\mu\text{A}$
CM input range- low	≤ 0
CM input range – high	$\geq 1.1\text{v}$
Differential output swing	1.2 pk-to-pk
Load	1 pF
DC loop gain	60db
Closed loop bandwidth	10 MHZ



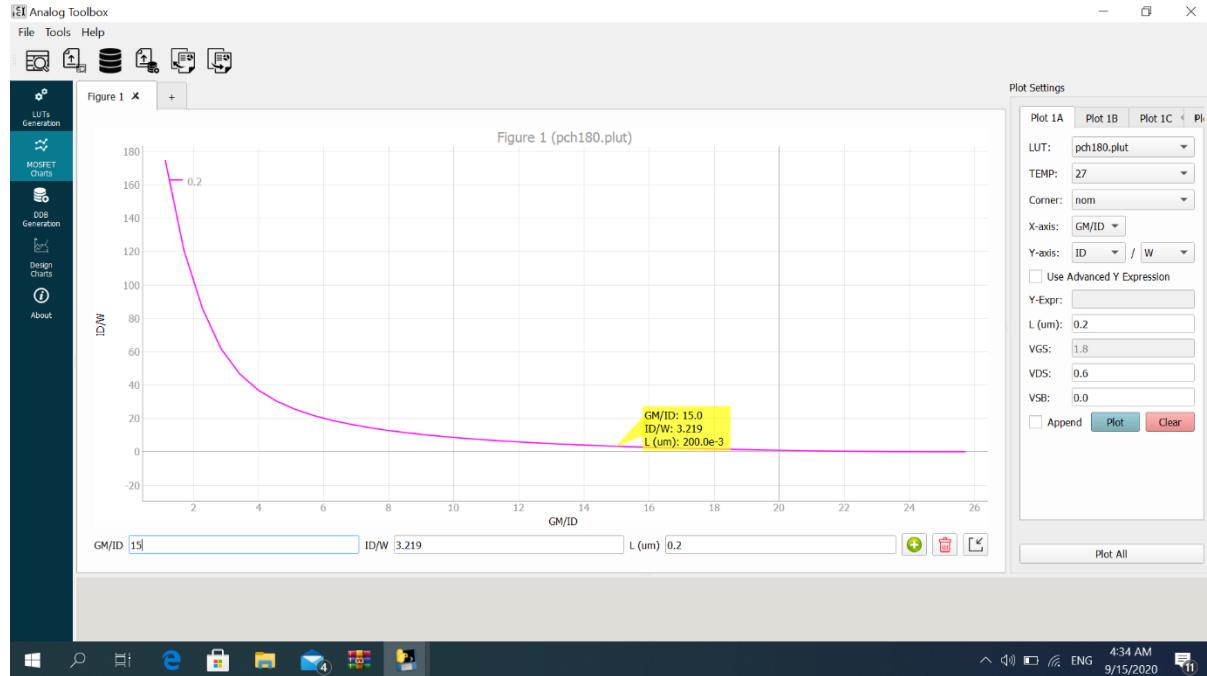
- The Folded OTA

- Design procedures:

- For the PMOS input pair M_1 :

$$\text{Let } L = 0.2\mu \text{ & } \frac{g_m}{I_D} = 15 \rightarrow V^* = \frac{2}{15} = 133.33mv$$

From design charts:



$$\bullet \left(\frac{I_D}{W} \right)_1 = 3.219 \rightarrow \because I_{D1} = 20\mu A \rightarrow \therefore W_1 = 6.213\mu m$$



$$\bullet V_{GS1} = 597.7mv$$

- For the current source and current mirror transistors $M_{2,5,6,7,8,9}$

$$\text{Let } L = 1\mu\text{m} \text{ & } \frac{g_m}{I_D} = 10 \rightarrow V^* = \frac{2}{10} = 200\text{mV}$$

From PMOS design charts:



- $\left(\frac{I_D}{W}\right)_{5,6,7,8} = 1.179$
 $\because I_{D5,7,8} = 20\mu\text{A} \rightarrow \therefore W_{5,7,8} = 16.964\mu\text{m}$
 $\because I_{D6} = 40\mu\text{A} \rightarrow \therefore W_6 = 33.927\mu\text{m}$



- $V_{GS5,6,7,8} = 609.2mv$

From NMOS design charts:



- $\left(\frac{I_D}{W}\right)_{2,9} = 4.665$

$$\because I_{D2} = 40\mu A \rightarrow \therefore W_2 = 8.5745\mu m$$

$$\because I_{D9} = 20\mu A \rightarrow \therefore W_9 = 4.287\mu m$$



- $V_{GS2,9} = 614.2mV$

➤ For the cascode transistors $M_{3,4}$

Let $L = 0.5\mu m$ & $\frac{g_m}{I_D} = 15 \rightarrow V^* = \frac{2}{15} = 133.33mV$

Let $V_{sb} = V_{2,5}^* = \frac{2}{10} = 0.2V$

From PMOS design charts:



- $\left(\frac{I_D}{W}\right)_4 = 964.2m \rightarrow I_{D4} = 20\mu A \rightarrow W_{cascP} = 20.743\mu m$



- $V_{GS4} = 611.1mv$

From NMOS design charts:



- $\left(\frac{I_D}{W}\right)_3 = 3.849 \rightarrow \because I_{D3} = 20\mu A \rightarrow \therefore W_{cascN} = 5.196\mu$



- $V_{GS3} = 624.7mv$

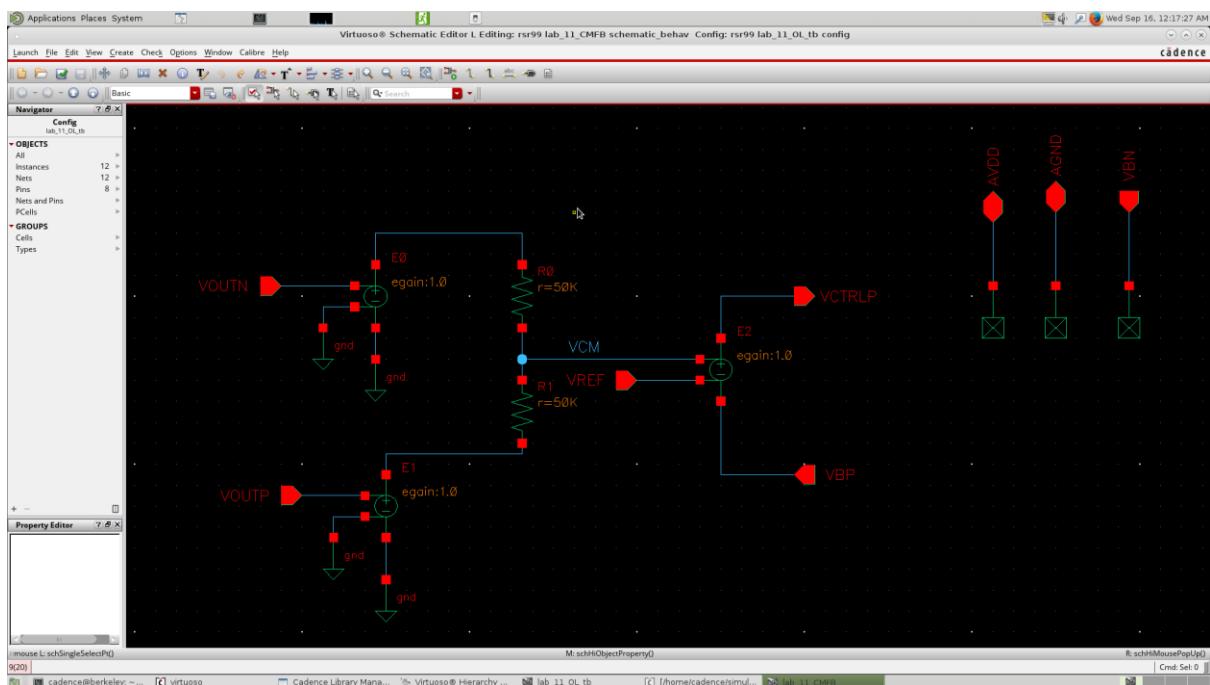
- In order to achieve the LG spec while keeping the same $\frac{g_m}{I_D}$ & V^* , I raised the cascode transistors sizing (W, L)
- ∵ The required LG was achieved when the sizing scaled up by 4.2

$$\therefore L_{3,4} = 0.5\mu * 4.2 = 2.1\mu m$$

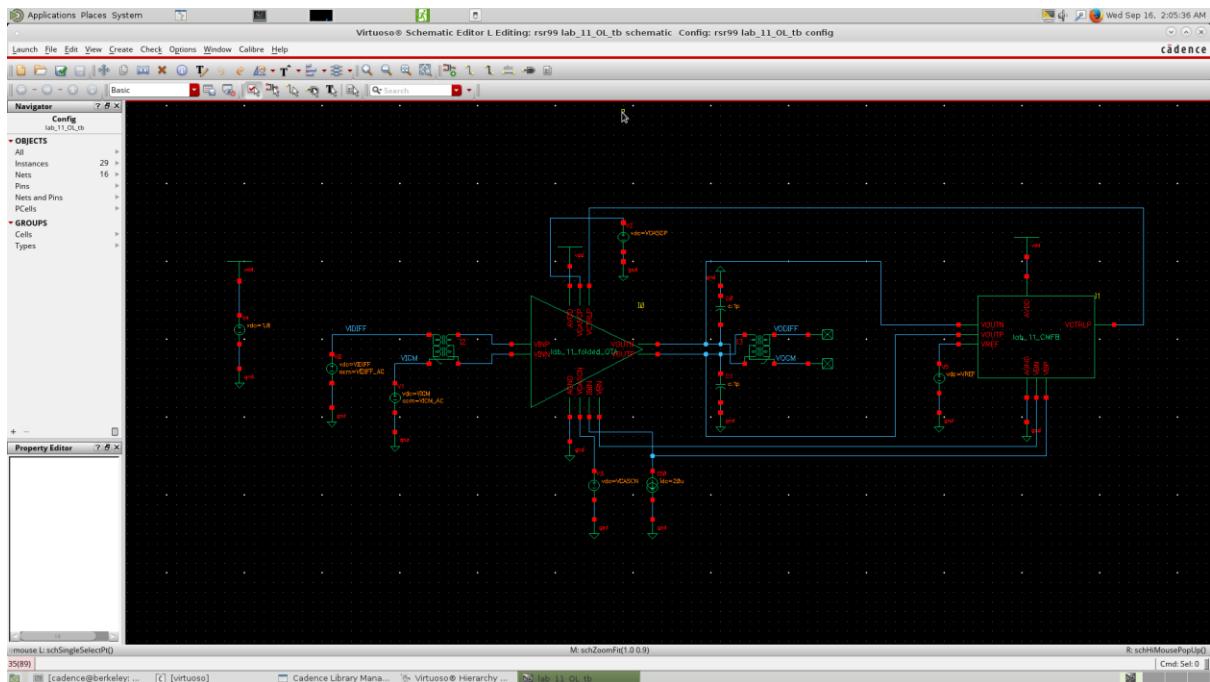
$$W_3 = W_{cascN} * 4.2 = 21.8232\mu m \text{ & } W_4 = W_{cascP} * 4.2 = 87.1206\mu m$$

- $V_{CASCN} = V_{GS3} + V_2^* = 824.7mV$
- $V_{CASCP} = V_{DD} - V_5^* - V_{GS4} = 988.9mV$

■ Part3: Open-Loop OTA Simulation (Behavioral CMFB)



- Behavioral CMFB

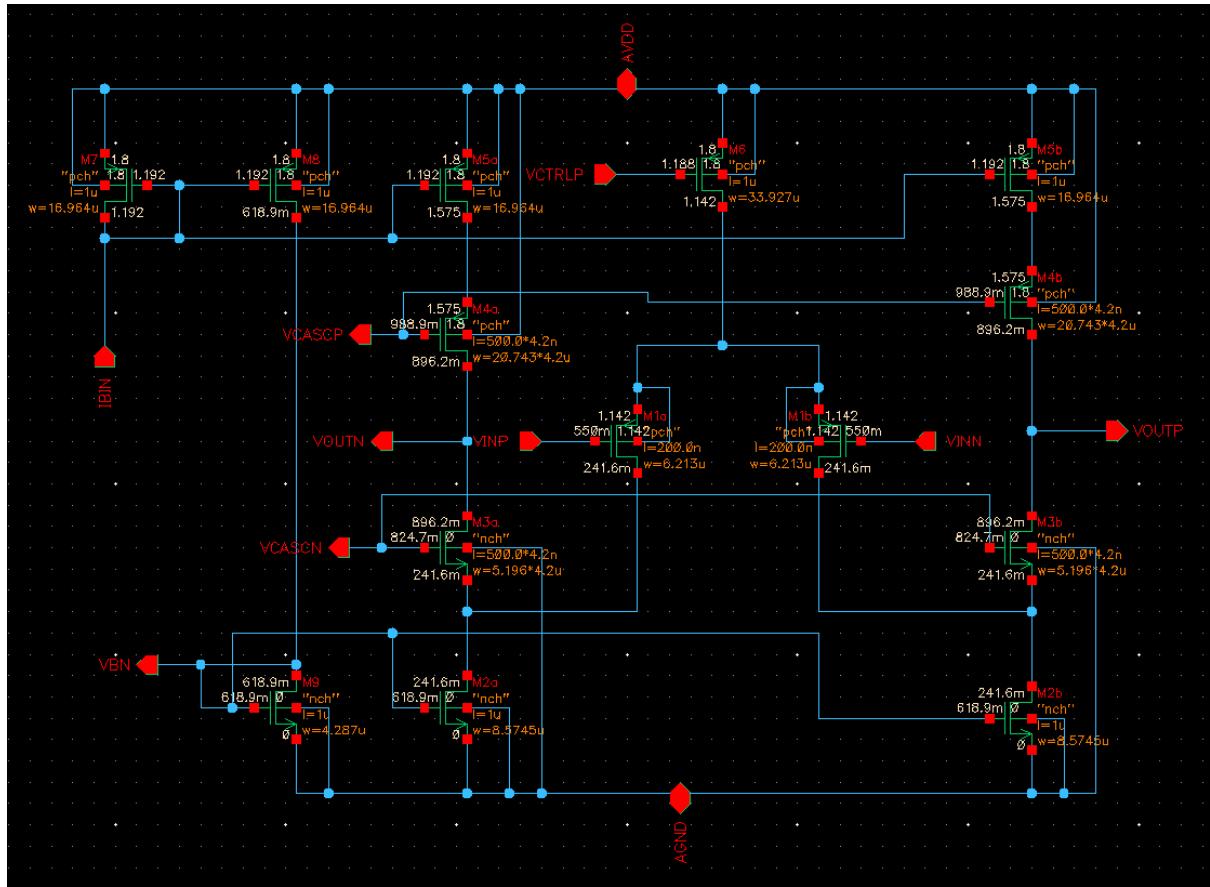


- Open-Loop testbench

1)

- $V_{ICM} = \frac{1.1+0}{2} = 0.55v$
- To maximize the symmetrical output swing V_{REF} is at the middle of output range

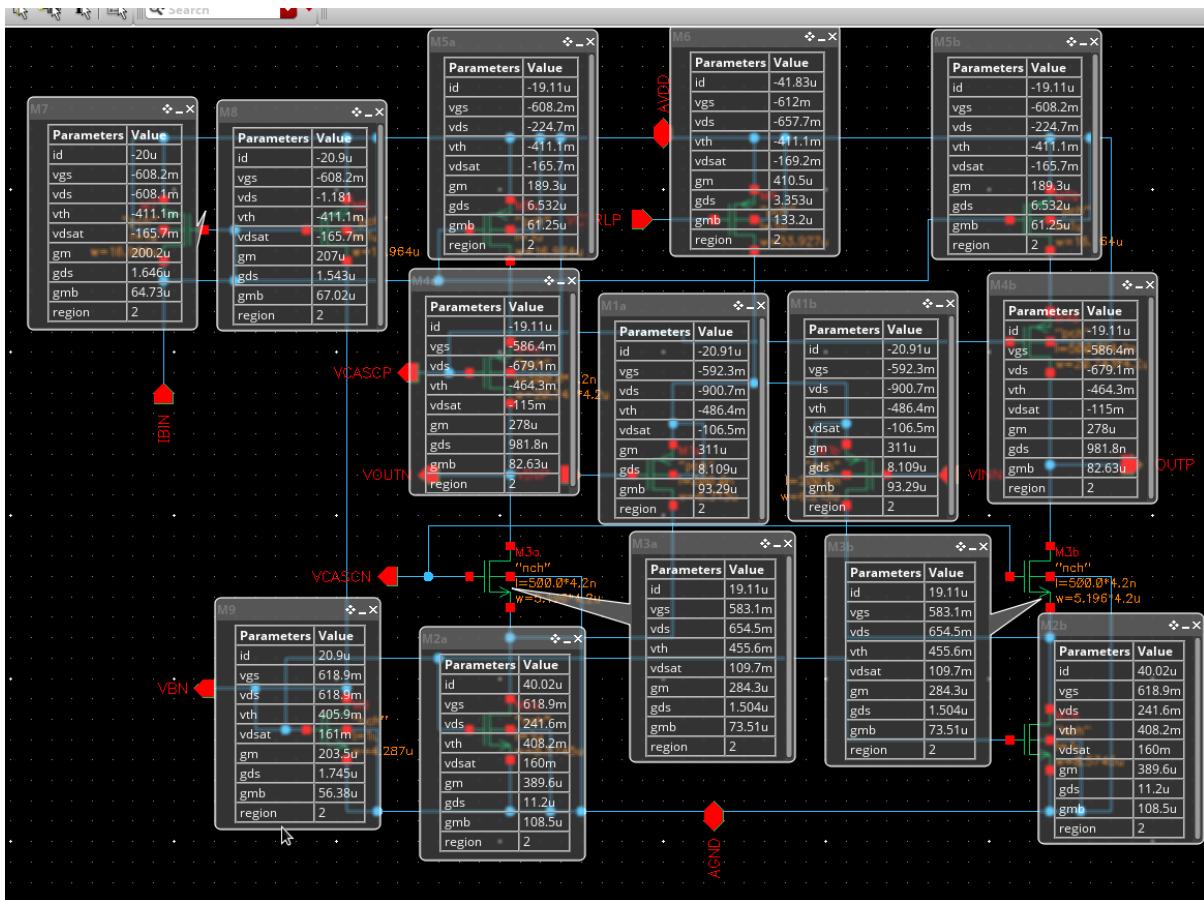
$$\therefore V_{REF} = \frac{V_{out,max} + V_{out,min}}{2} = \frac{(V_{DD} - V_5^* - V_4^*) + (V_3^* + V_2^*)}{2} = 0.9v$$



- Schematic of the OTA with DC node voltages
- The CM level at the OTA output = $896.2mv \approx 0.9v$
- The diff input voltages of the error amplifier are $V_{OCM}(896.2mv)$ & $V_{REF}(900mv)$ and they are almost the same

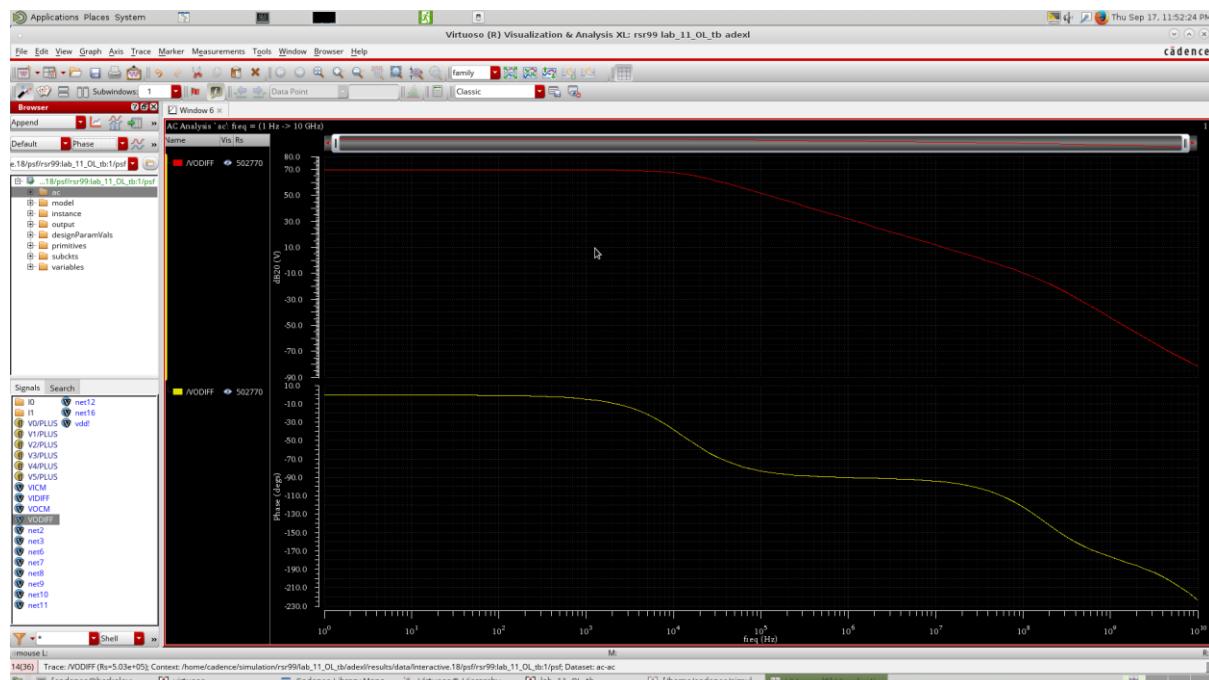
The diff output voltages of the error amplifier are $V_{CTRLP}(1.188v)$ & $V_{BP}(1.192)$ and they are almost the same

- The relation between input and output voltages of the error amplifier is the error amplifier gain as $A_{error\ amp} = \frac{\Delta V_{out}}{\Delta v_{in}} \approx 1$



- DC OP parameters of the OTA

- Diff small signal ccs



- Diff gain (db & phase) vs frequency

ymax(mag(v("/VODIFF" ?result "ac")))	3.136E3
ymax(dB20(mag(v("/VODIFF" ?result "ac"))))	69.93
bandwidth(mag(v("/VODIFF" ?result "ac")) 3 "low")	13.01E3
gainBwProd(mag(v("/VODIFF" ?result "ac")))	40.91E6
unityGainFreq(mag(v("/VODIFF" ?result "ac")))	39.75E6
phaseMargin(mag(v("/VODIFF" ?result "ac")))	180.0

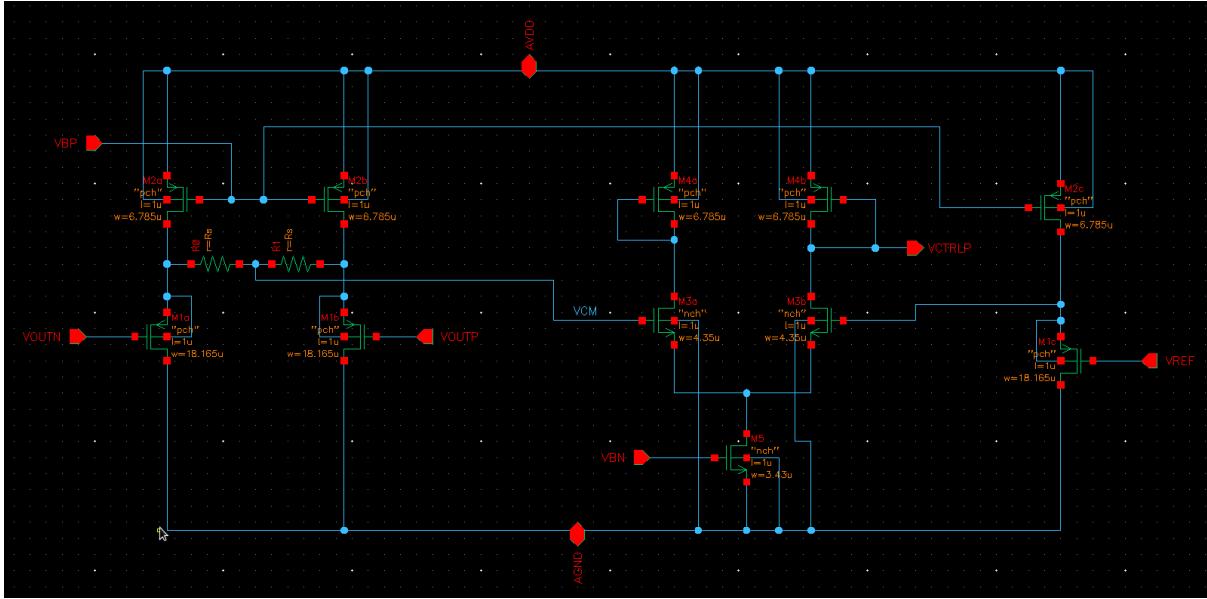
- Circuit parameters (DC gain, BW, GBW, UGF, and PM) from simulation
- Analytically:

$$\begin{aligned}
 & \triangleright R_{out} = (r_{o3}(1 + (g_{m3} + g_{mb3})(r_{o2} \| r_{o1}))) \| (r_{o4}(1 + (g_{m4} + g_{mb4})r_{o5})) \\
 & = \left(\frac{1}{g_{ds3}} \left(1 + (g_{m3} + g_{mb3}) \left(\frac{1}{g_{ds2}} \| \frac{1}{g_{ds1}} \right) \right) \right) \\
 & \| \left(\frac{1}{g_{ds4}} \left(1 + \frac{g_{m4} + g_{mb4}}{g_{ds5}} \right) \right) = 10.585M\Omega
 \end{aligned}$$

$\triangleright DC\ gain = A_{OL} = g_{m1}R_{out} = 3.292\ k = 70.35\ db$
 $\triangleright BW = \frac{1}{2\pi R_{out} C_l} = 15.036\ kHz$
 $\triangleright GBW = A_{OL} * BW = \frac{g_{m1}}{2\pi C_l} = 49.5\ MHz$

	Simulation results	Hand analysis results
DC gain	$3.136k = 69.93db$	$3.292\ k = 70.35\ db$
BW	$13.01kHz$	$15.036kHz$
GBW	$40.91GHz$	$49.5MHz$

▪ Part4: Open-Loop simulation (Actual CMFB)



- Actual CMFB circuit
- The CD amplifiers (a&b) introduce a DC shift to the V_{OCM} so in order to give the same DC shift to V_{REF} I add another CD amplifier (c) identical to the (a&b)
- \because the $40\mu A$ is divided between the CMFB branches $\rightarrow \therefore$ each branch has $\frac{40\mu A}{5} = 8\mu A$

$$\therefore I_{D1,2,3,4} = 8\mu A \quad \& \quad I_{D5} = 16\mu A$$

- Let $L = 1\mu m$ for all CMFB transistors
- For current sources and current mirrors load transistors $M_{2,4,5}$:

Let $\frac{g_m}{I_D} = 10 \rightarrow V^* = \frac{2}{10} = 200mV \rightarrow$ same $\frac{g_m}{I_D}$ & V^* of the Folded current sources

transistors as they form a current mirror connection and have the same V_{GS} :

- ❖ $(V_{DD} - V_{BP})$ for PMOS current sources $M_{5,7,8}$ of the OTA and M_2 of CMFB
- ❖ V_{BN} for NMOS current sources $M_{2,9}$ of the OTA and M_5 of CMFB
- ❖ $(V_{DD} - V_{CTRLP})$ for PMOS M_5 of the OTA and the current mirror load M_4 of the CMFB

\therefore similar to the current source transistors of the OTA :

- ❖ For PMOS : $\left(\frac{I_D}{W}\right)_{2,4} = 1.179 \rightarrow \therefore I_{D2,4} = 8\mu A$

$$\therefore W_{2,4} = 6.785\mu m \quad \& \quad V_{GS2,4} = 609.2mV$$

- ❖ For NMOS : $\left(\frac{I_D}{W}\right)_5 = 4.665 \rightarrow \therefore I_{D5} = 16\mu A$

$$\therefore W_5 = 3.43\mu m \quad \& \quad V_{GS5} = 614.2mv$$

➤ For the other transistors $M_{1,3}$: → let $\frac{g_m}{I_D} = 15$ → $V^* = \frac{2}{15} = 133.33mv$

From PMOS design charts:



- $\left(\frac{I_D}{W}\right)_1 = 440.4m \rightarrow \because I_{D1} = 8\mu A \rightarrow \therefore W_1 = 18.165\mu m$



- $V_{GS1} = 528.9mv$

From NMOS design charts:

For error amplifier input pair M_3 : $V_{sb} = V_5^* = 0.2$



- $\left(\frac{I_D}{W}\right)_3 = 1.846 \rightarrow \because I_{D3} = 8\mu A \rightarrow \therefore W_3 = 4.35\mu A$



- $V_{GS3} = 592.1mv$

- For the sensing resistors:

Let the max current flowing through them (when diff signal is max) = $10\% I_{D2}$

$$\therefore I_{Rs} = \frac{V_{out,max} - V_{out,min}}{2R_s}$$

$$\rightarrow \therefore R_s = \frac{V_{out,max} - V_{out,min}}{2I_{Rs}} = \frac{(V_{DD} - V_{2CMFB}^* - V_{GS1CMFB}^*) - (V_{2OTA}^* + V_{3OTA}^*)}{2I_{Rs}}$$

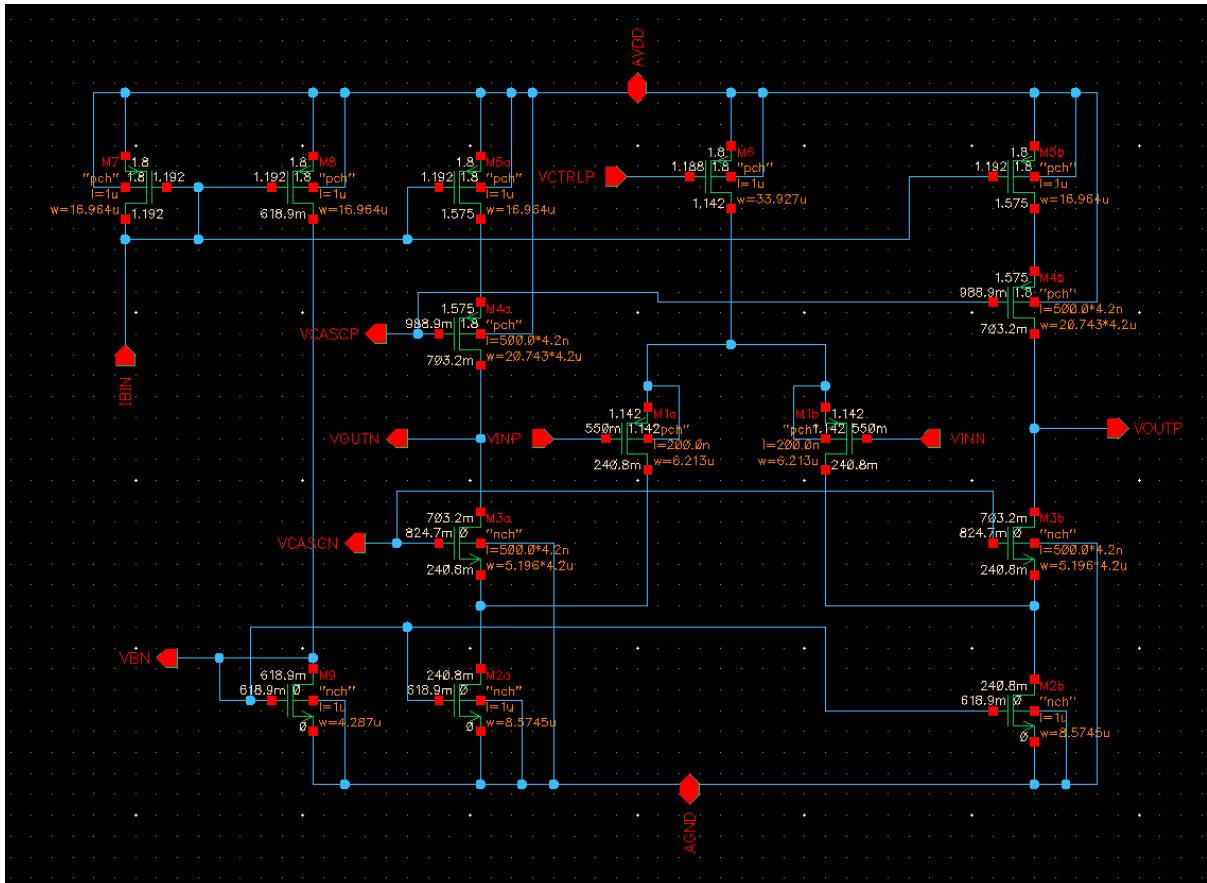
$$= 502.77k$$

- For V_{OCM} to be around the middle of its range with maximum symmetric output swing: V_{REF} will be in the middle of that range

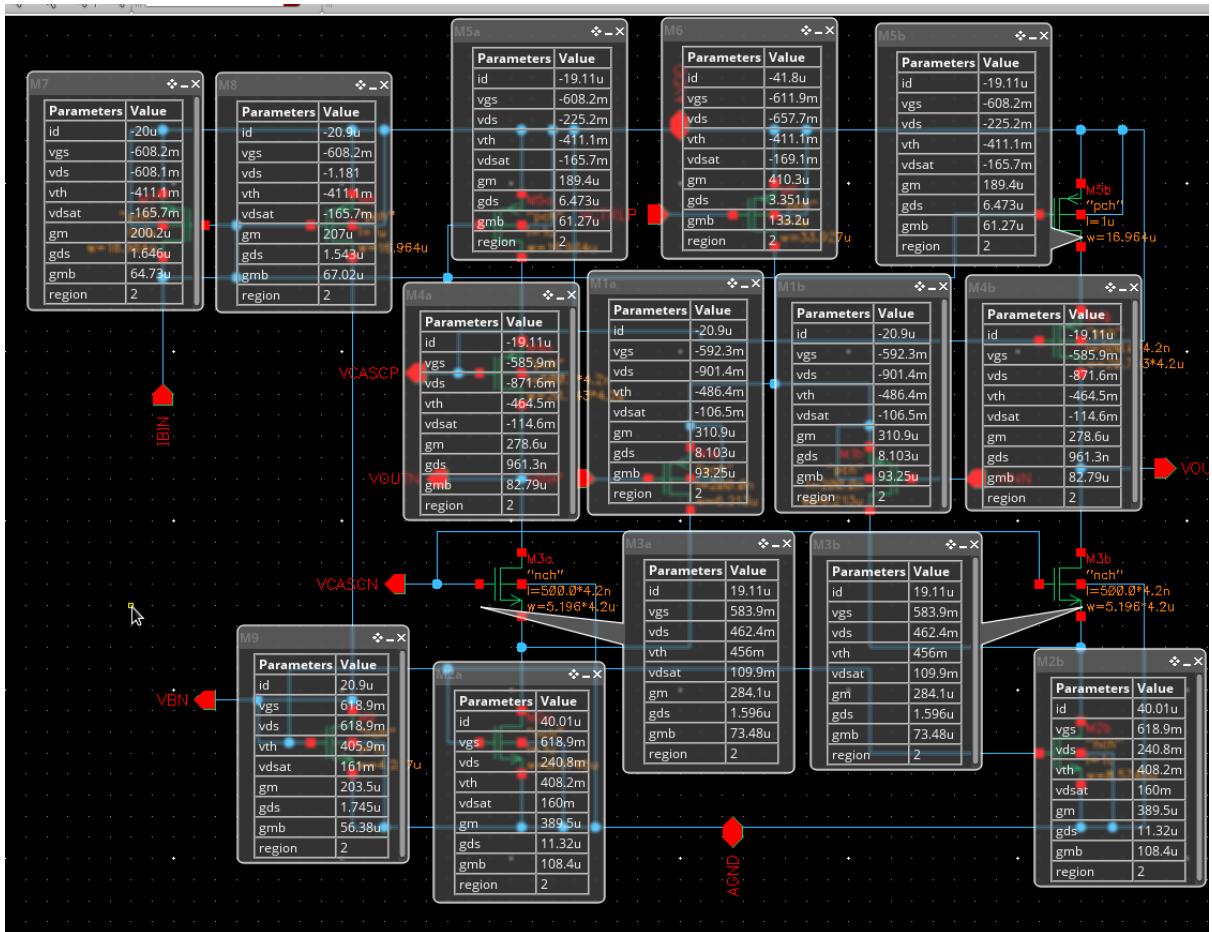
$$\therefore V_{REF} = \frac{V_{out,max} + V_{out,min}}{2} = \frac{(V_{DD} - V_{2CMFB}^* - V_{GS1CMFB}^*) + (V_{2OTA}^* + V_{3OTA}^*)}{2}$$

$$= 702.217mv$$

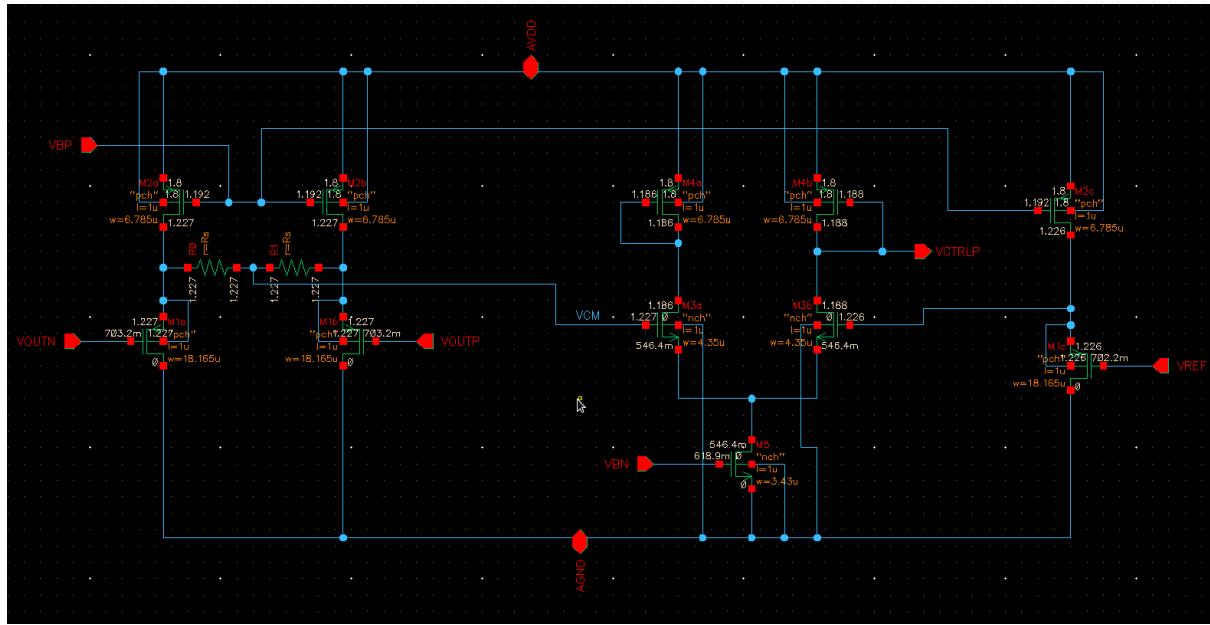
1)



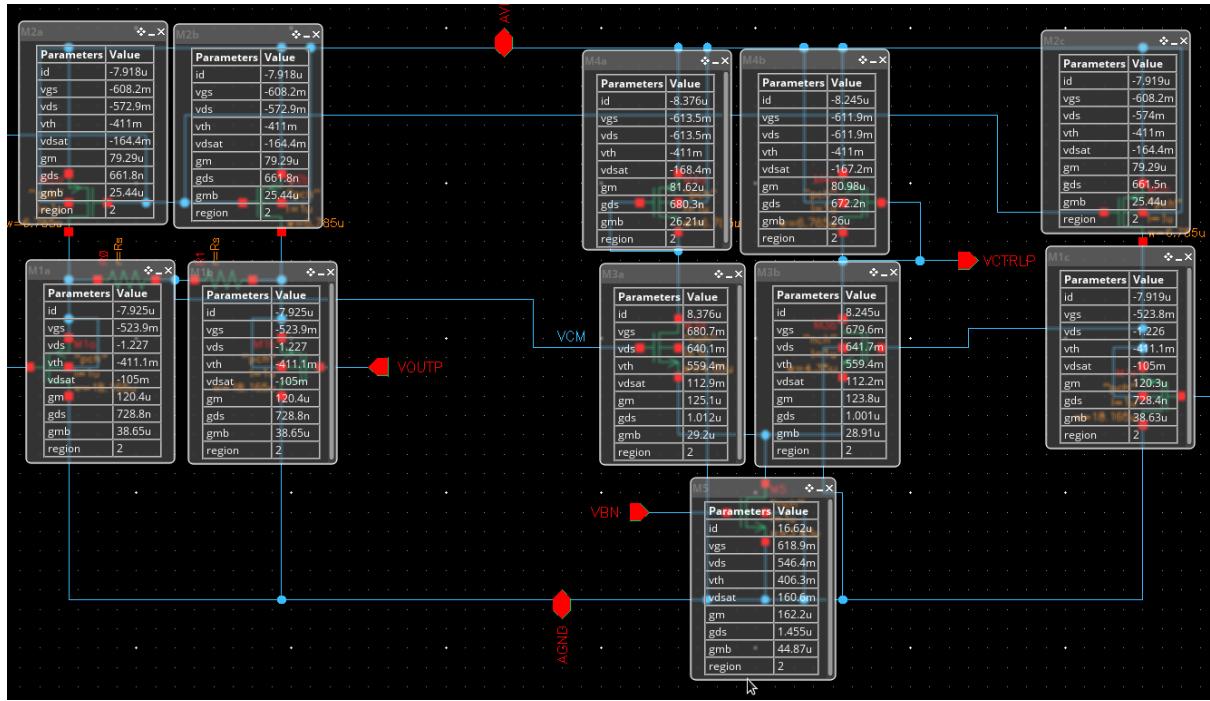
- Schematic of the OTA with DC node voltages
- The CM level at the OTA output = $703.2mV \approx V_{REF}$ as the error amplifier works to set the CM output level very close to V_{REF}



- DC OP parameters of the OTA

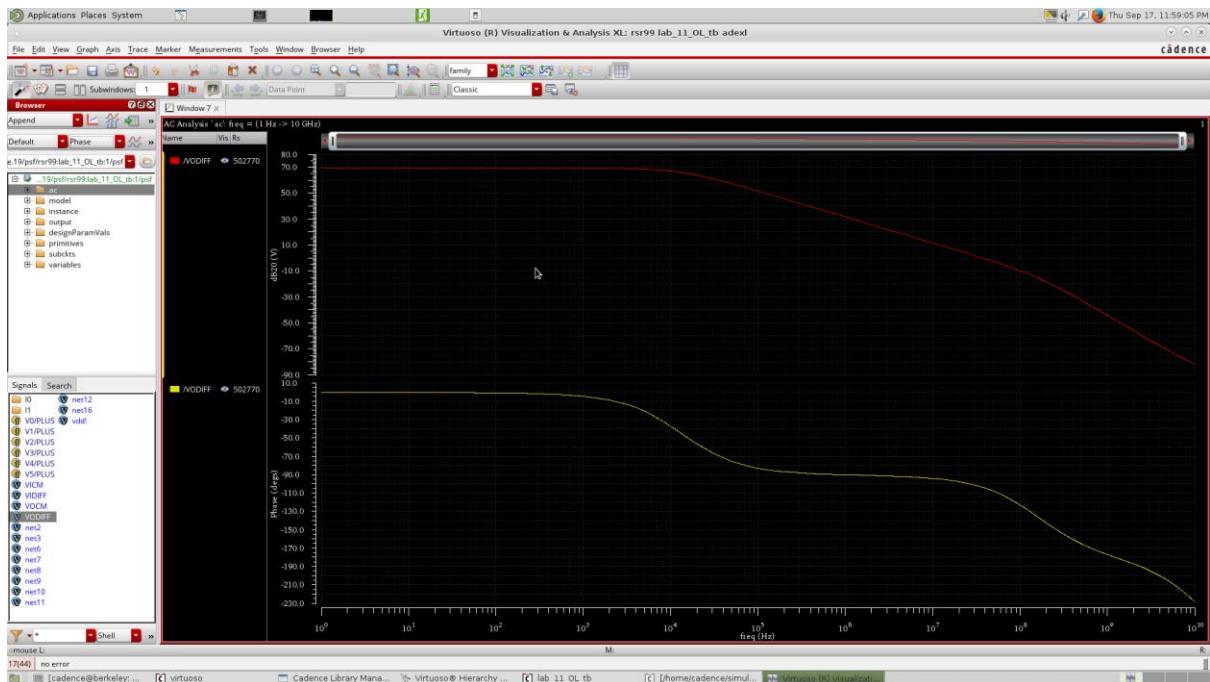


- CMFB circuit with DC node voltages
- The differential input voltages of the error amplifier are $(V_{OCM} + V_{GS1} = 1.227v)$ and $(V_{REF} + V_{GS1} = 1.226)$ and they are almost the same
- The differential output voltages of the error amplifier are $(1.188v \& 1.186v)$ and they are almost the same
- The relation between input and output voltages of the error amplifier is the error amplifier gain



- DC OP parameters of the CMFB circuit

2) Diff small signal ccs:

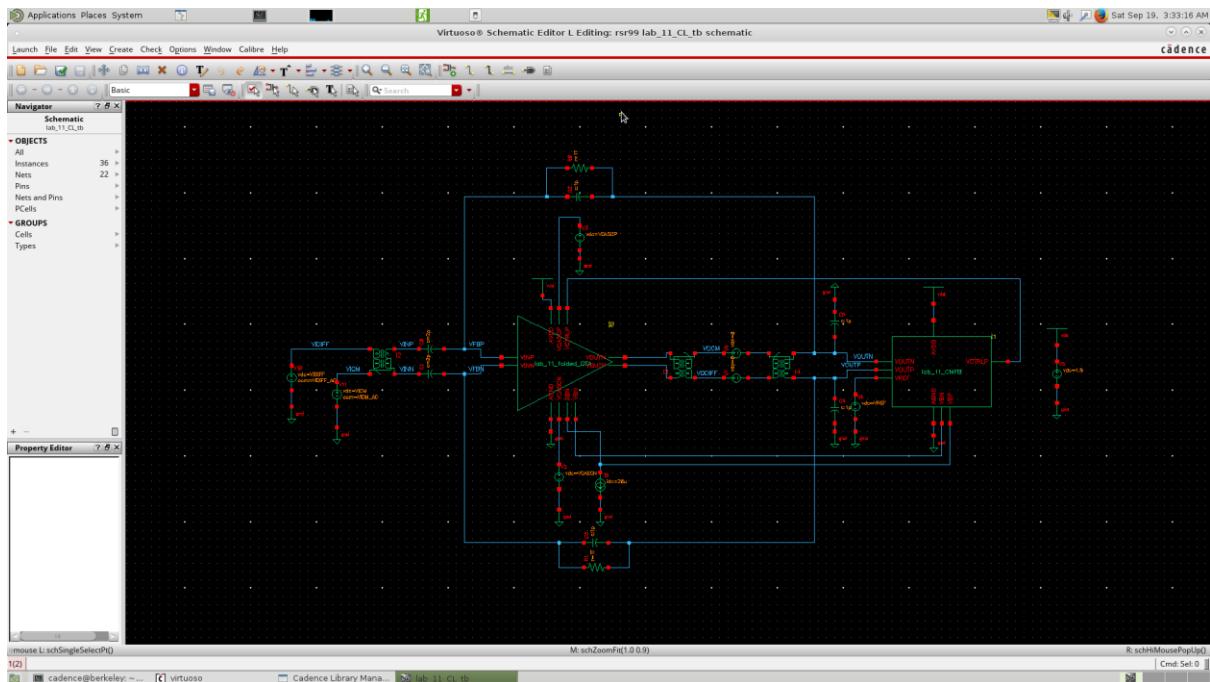


- Diff gain (db & phase) vs frequency

<code>ymax(mag(v("/VODIFF" ?result "ac"))))</code>	2.986E3
<code>ymin(dB20(mag(v("/VODIFF" ?result "ac")))))</code>	69.50
<code>bandwidth(mag(v("/VODIFF" ?result "ac")) 3 "low")</code>	13.51E3
<code>gainBwProd(mag(v("/VODIFF" ?result "ac"))))</code>	40.46E6
<code>unityGainFreq(mag(v("/VODIFF" ?result "ac"))))</code>	39.35E6
<code>phaseMargin(mag(v("/VODIFF" ?result "ac"))))</code>	180.0

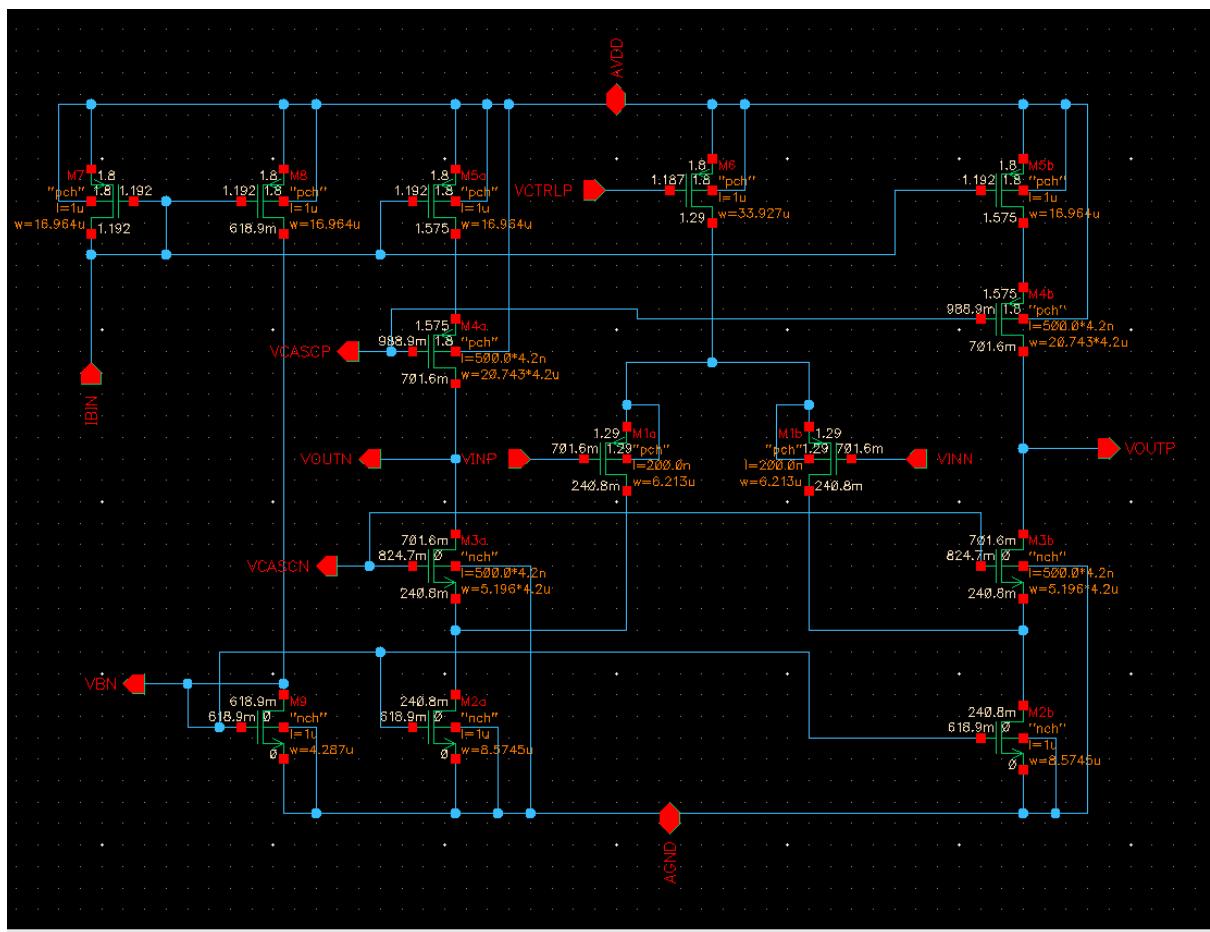
- Circuit parameters calculation from simulation

▪ Part5: Closed Loop Simulation (AC and STP Analysis)



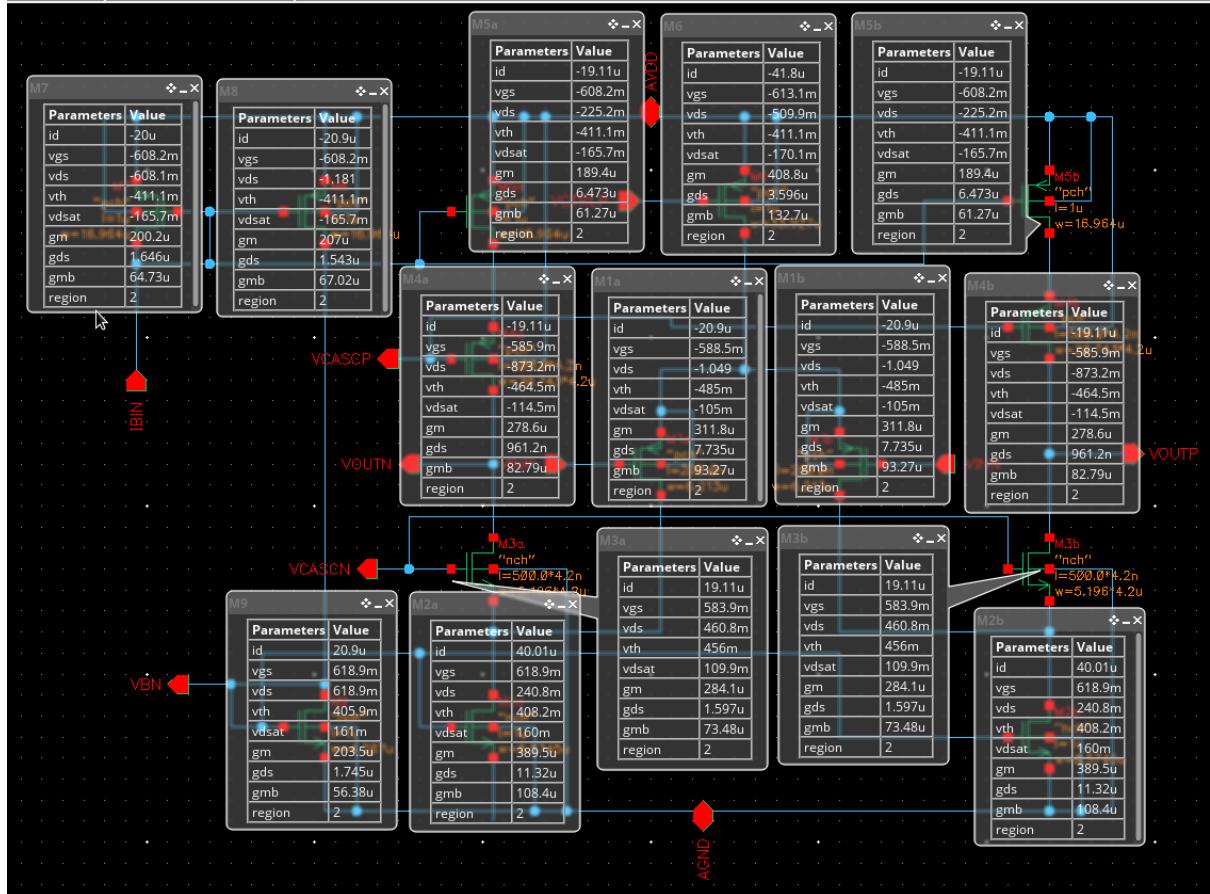
- Closed-Loop testbench

1)

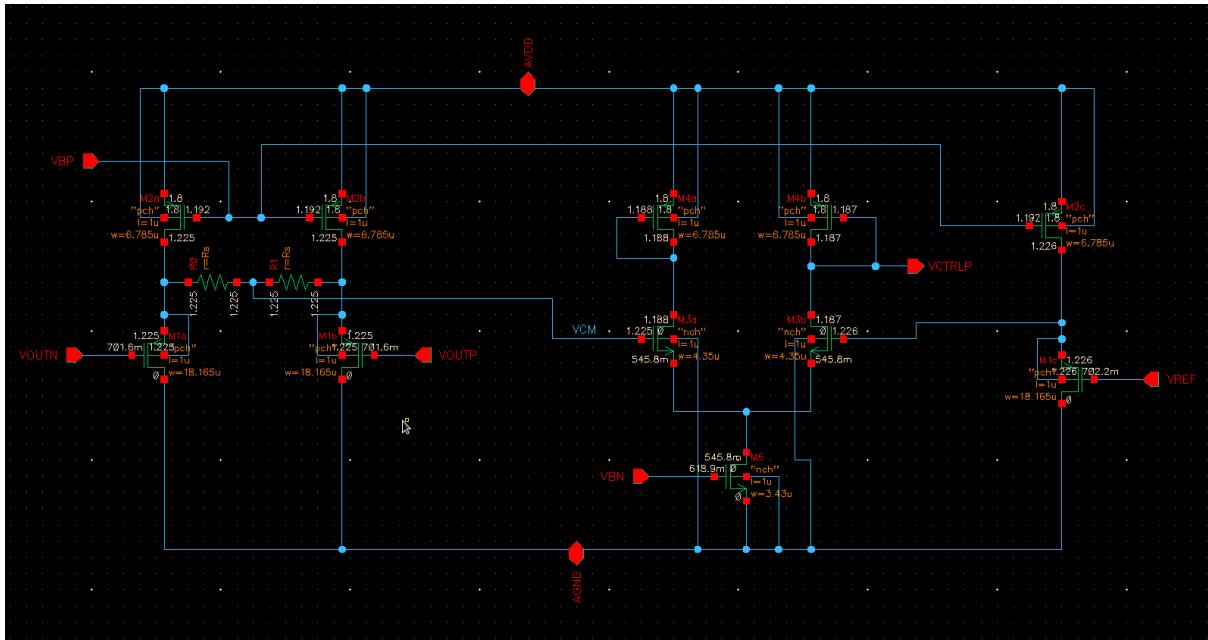


- Schematic of the OTA with DC node voltages in closed loop configuration

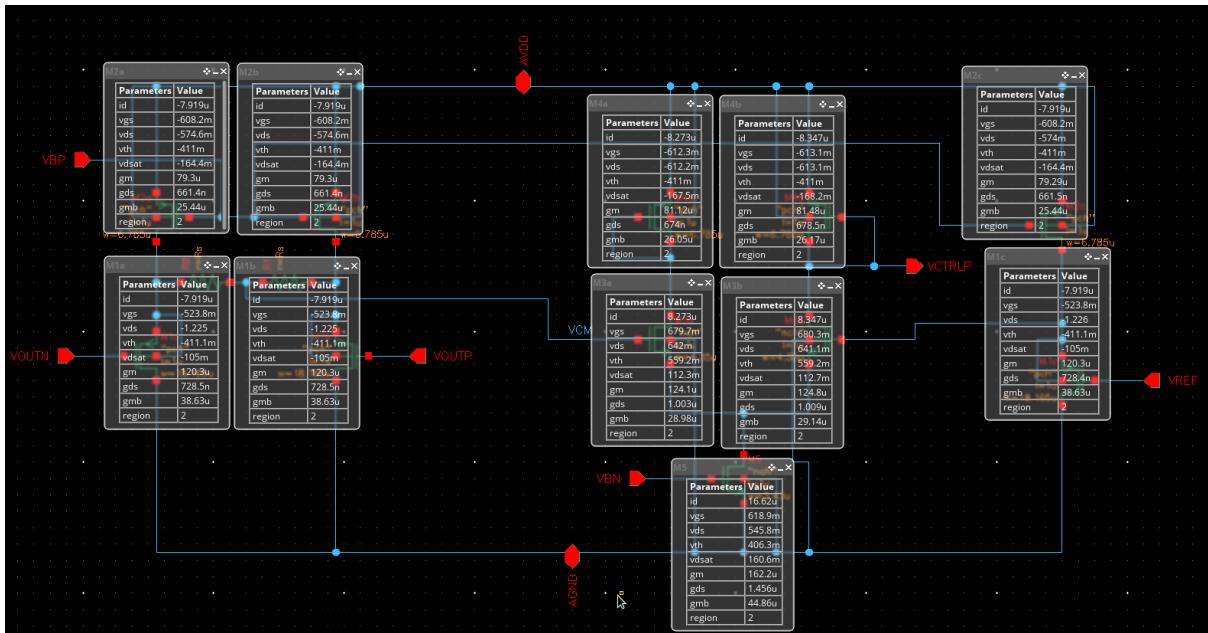
- The CM level at the OTA output = $701.6mv \approx V_{REF}$ as the CMFB circuit works to set $V_{OCM} \approx V_{REF}$
- The CM level at the OTA input = $701.6mv = V_{OCM}$ as the large resistance parallel to the feedback capacitance close the loop in DC and sets $V_{ICM} = V_{OCM}$



- Closed Loop DC OP parameters of the OTA

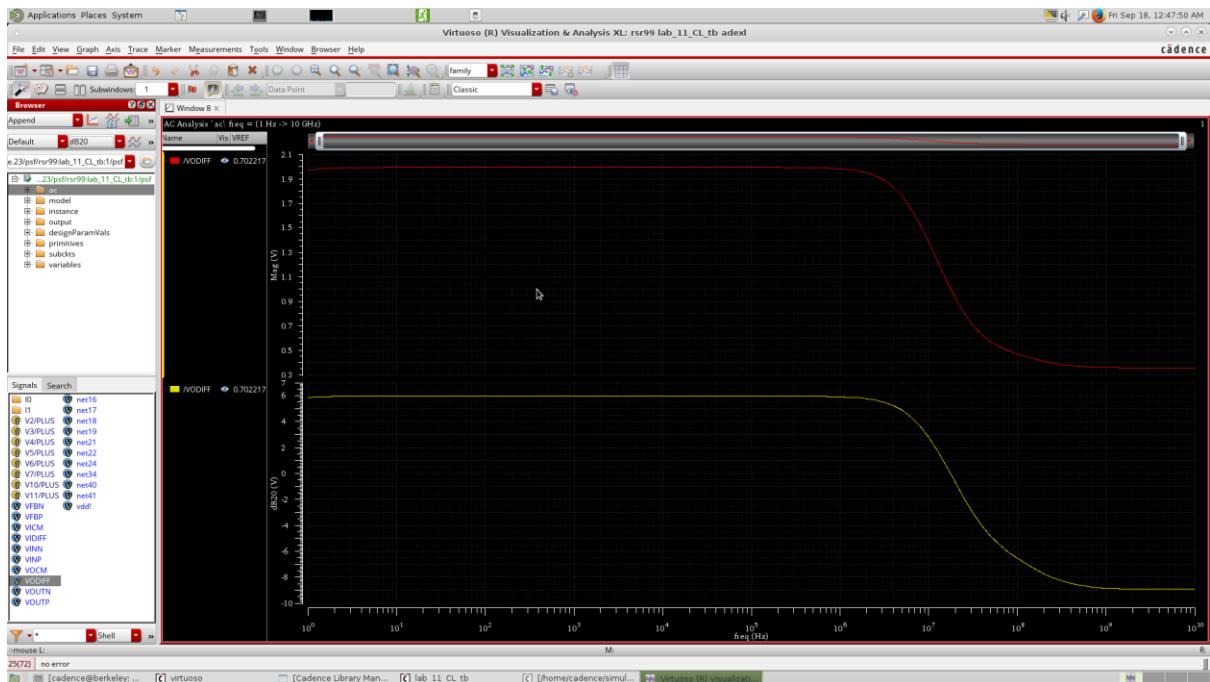


- CMFB circuit with DC node voltages in closed loop configuration



- Closed loop DC OP parameters of the CMFB circuit

2) Differential closed loop response:

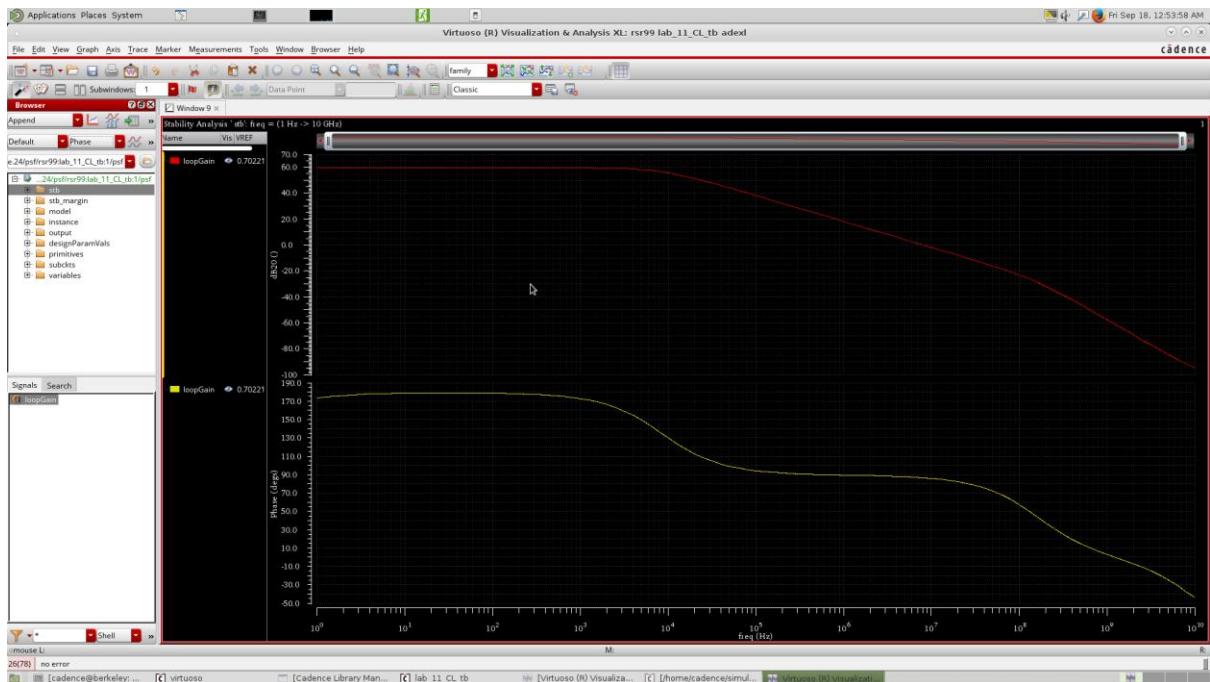


- V_{odiff} vs frequency

1	
VREF	702.2E-3
ymax(mag(v("/VODIFF ?result "ac"))))	1.998
ymax(dB20(mag(v("/VODIFF ?result "ac")))))	6.012
bandwidth(mag(v("/VODIFF ?result "ac")) 3 "low")	9.820E6
gainBwProd(mag(v("/VODIFF ?result "ac"))))	19.42E6
unityGainFreq(mag(v("/VODIFF ?result "ac"))))	17.87E6

- Circuit parameters calculation from simulation
- Closed loop gain = $1.998 \approx 2$
- $CL BW = 9.82MHz \approx 10MHz$

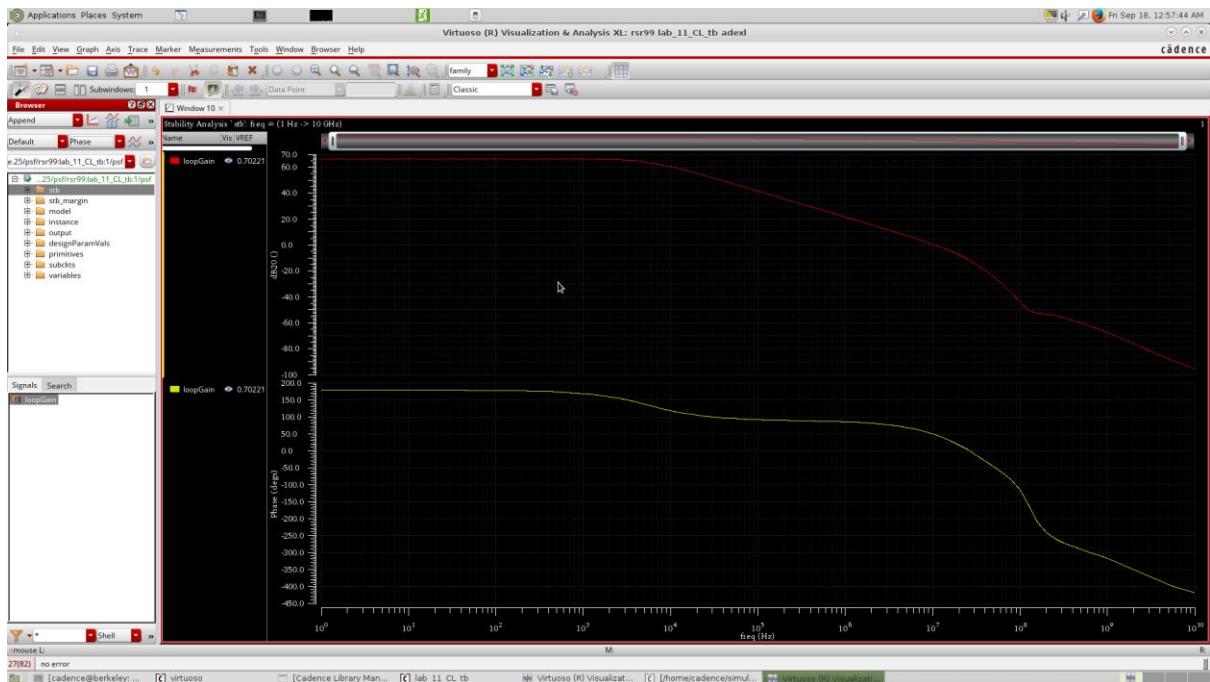
3) Differential and CMFB loops stability (stb analysis)



- Diff LG (db and phase)

	1
VREF	702.2E-3
ymax(mag(getData("loopGain" ?result "stb")))	1.002E3
ymax(dB20(mag(getData("loopGain" ?result "stb"))))	60.02
bandwidth(mag(getData("loopGain" ?result "stb")) 3 "low")	8.411E3
gainBwProd(mag(getData("loopGain" ?result "stb")))	8.448E6
getData("/phaseMargin" ?result "stb_margin") (Deg)	87.03

- Diff LG circuit parameters
- DC LG = $60.02\text{db} \approx 60\text{db}$



- CM LG (db and phase)

	1
VREF	702.2E-3
ymax(mag(getData("loopGain" ?result "stb"))))	2.211E3
ymax(dB20(mag(getData("loopGain" ?result "stb")))))	66.89
bandwidth(mag(getData("loopGain" ?result "stb")) 3 "low")	5.730E3
gainBwProd(mag(getData("loopGain" ?result "stb"))))	12.70E6
getData("/phaseMargin" ?result "stb_margin") (Deg)	47.07

- CM LG circuit parameters

	Diff loop results	CM loop results
GBW	8.448MHz	12.7MHz
PM	87.03°	47.07°

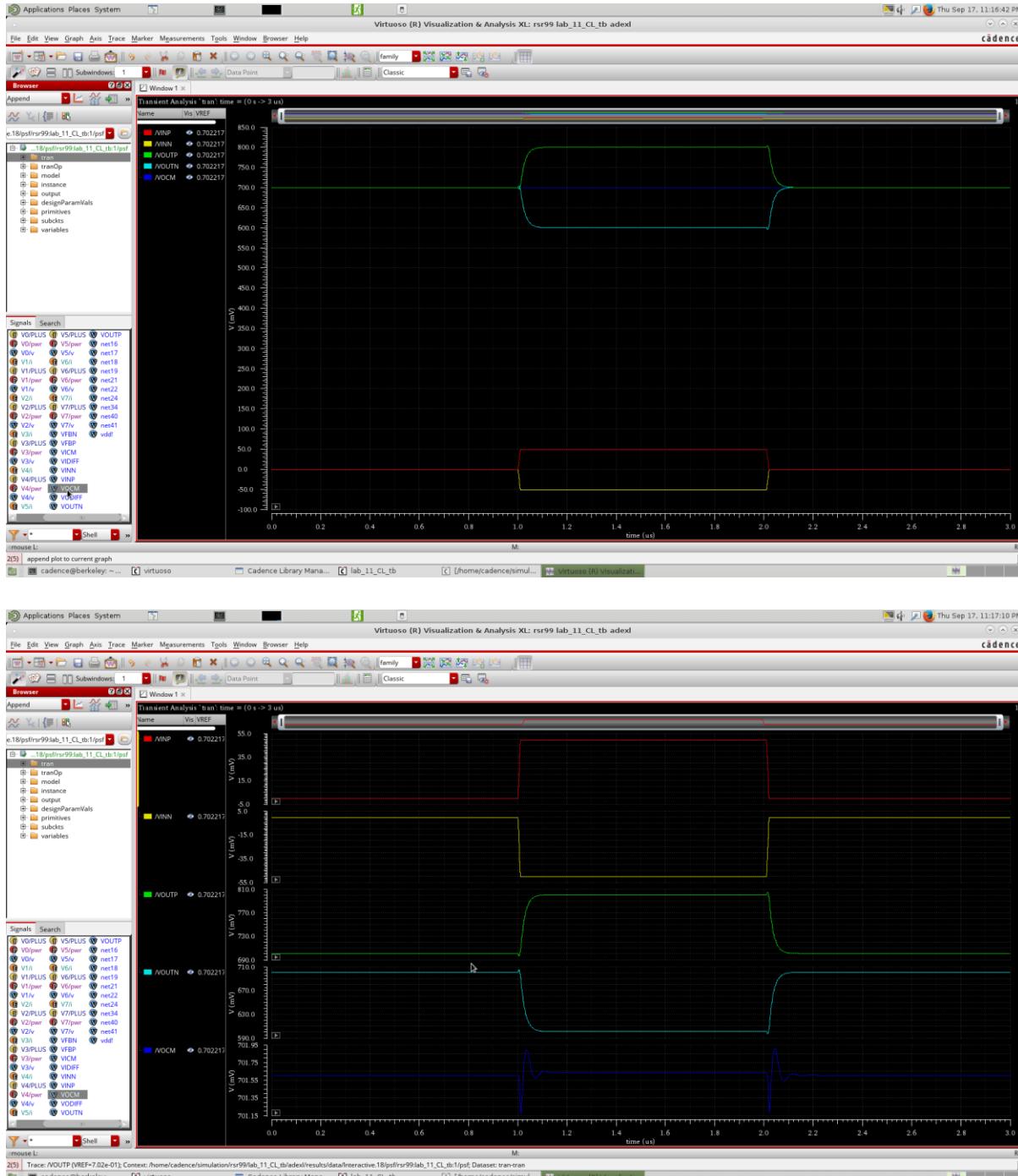
- $GBW_{CM} > GBW_{diff}$ as CM LG has higher gain and BW
- $PM_{CM} < PM_{diff}$ as $GBW \approx G_x \rightarrow G_{xCM} > G_{xdiff}$ and that make $PM_{CM} < PM_{diff}$

	Diff loop results	Open loop simulation
DC gain	$1.002k = 60.02db$	$2.986k = 69.5db$
GBW	$8.448MHz$	$40.46MHz$

- $\because LG = \beta A_{OL} \text{ & } \beta < 1 \rightarrow \therefore DC LG < DC A_{OL} \text{ & } GBW_{LG} < GBW_{OL}$

■ Part6: Closed Loop Simulation (Transient Analysis)

1) Differential and CMFB loops stability (transient analysis)

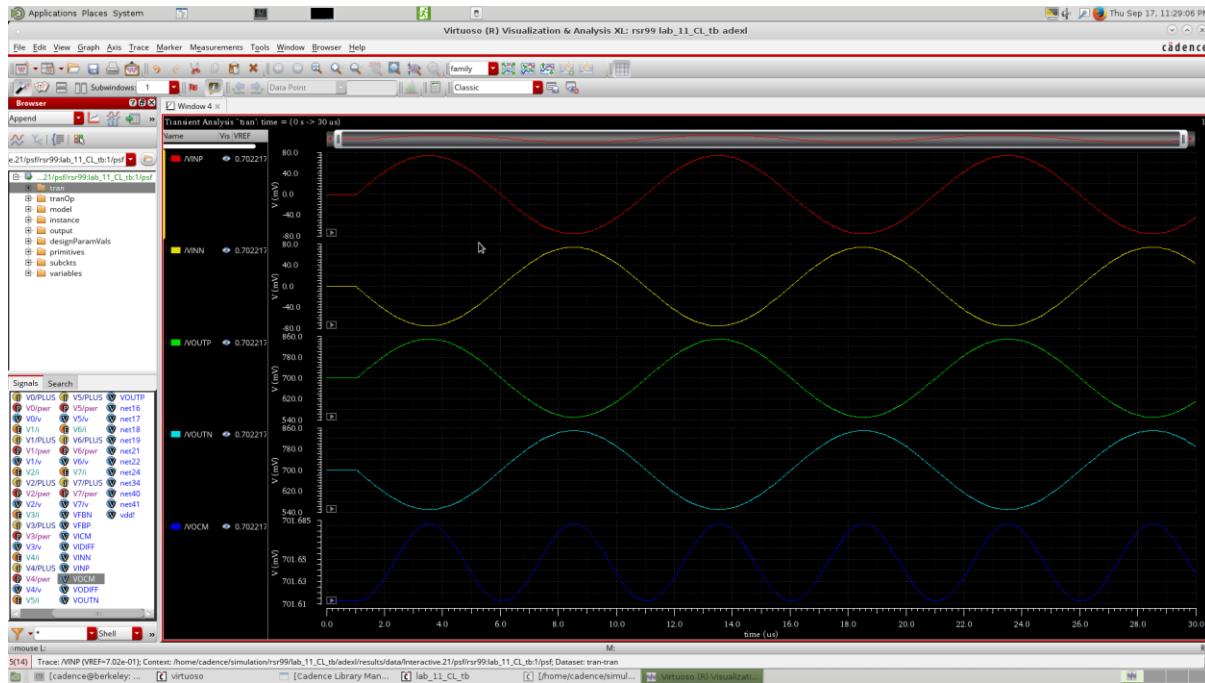
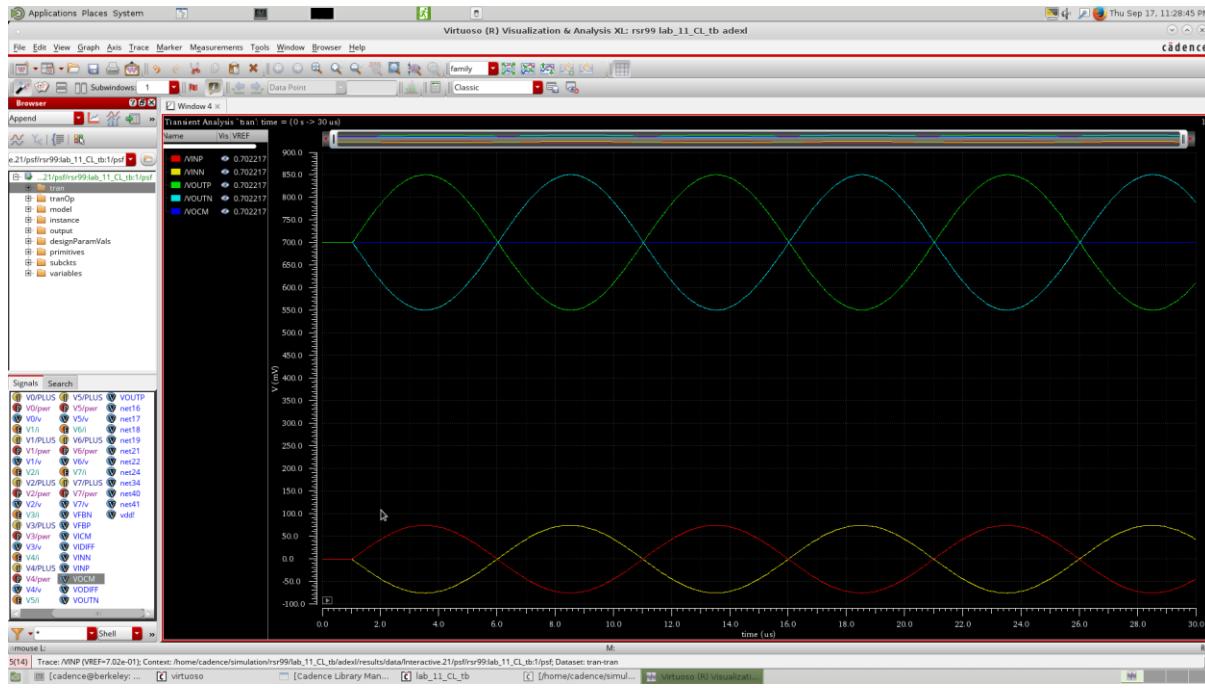


- Transient signals at $V_{INP}, V_{INN}, V_{OUTP}, V_{OUTN}$ & V_{OCM} with differential input pulse
- There is a little CM ringing as the CM is underdamped system due to $PM_{CM} = 47.07^\circ$
- Both loops are stable with $PM_{diff} = 87.03^\circ$ & $PM_{CM} = 47.07^\circ$

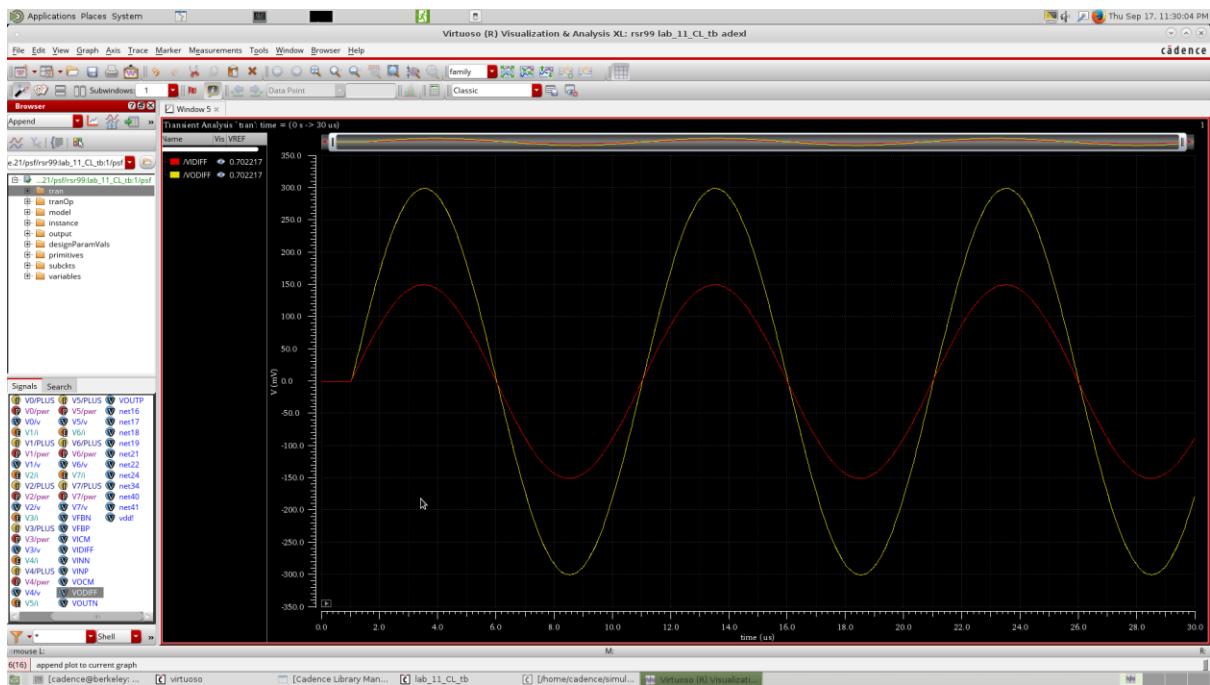


- Transient signals at V_{INP} , V_{INN} , V_{OUTP} , V_{OUTTN} & V_{OCM} with CM input pulse
- There is a little CM ringing as the CM is underdamped system due to $PM_{CM} = 47.07^\circ$
- Both loops are stable with $PM_{diff} = 87.03^\circ$ & $PM_{CM} = 47.07^\circ$

2) Output swing



- Transient signals at V_{INP} , V_{INN} , V_{OUTP} , V_{OUTN} & V_{OCM} with differential sinusoidal input



- Transient signal at V_{IDIFF} & V_{ODIFF}

<code>ymin(v"/VIDIFF" ?result "tran")</code>	<code>150.0E-3</code>
<code>ymin(v"/VIDIFF" ?result "tran")</code>	<code>-150.0E-3</code>
<code>ymin(v"/VODIFF" ?result "tran")</code>	<code>299.7E-3</code>
<code>ymin(v"/VODIFF" ?result "tran")</code>	<code>-299.7E-3</code>

- $V_{IDIFF} \text{ peak to peak} = V_{IDIFF,max} - V_{IDIFF,min} = 300\text{mV}$
- $V_{ODIFF} \text{ peak to peak} = V_{ODIFF,max} - V_{ODIFF,min} = 599.4\text{mV}$
- $A_{CL} = \frac{\Delta V_{ODIFF}}{\Delta V_{IDIFF}} = \frac{V_{ODIFF} \text{ peak to peak}}{V_{IDIFF} \text{ peak to peak}} = 1.998 \approx 2$