Programmer's guide for running custom assembly tests on SweRV EL2 on Verilator environment

1. Firstly the programmer can write any RISC V assembly with any instructions from RISC V IMC in a file with .s extension. Programmer can opt to use SweRV's predefined headers from the file defines.h by using: #include "defines.h" at the start of the assembly file.
2. Now if the programmer wants to make its code more readable he/she can add user defined headers by using #define HEADER_NAME (value of header).For example if the header to be defined is named as STDOUT and its value is 0xd0580000 so it can be defined as #define STDOUT 0xd0580000. (**note**: name and value must be in same line after #define).
3. Two forward slashes can be used for commenting.
4. Now .section .text can be used before defining any additional data that is required in the test to print which usually consists of ASCII for example you can see the hello world test of SweRV which is present in RV_ROOT/testbench/asm. (RV_ROOT = the/path/to/swerv/core).
5. Now the global header of starting the code is defined as .global _start and from the next line after writing _start: programmers can begin to write the assembly code to perform any operation through core.
6. Once the file is ready it must be placed under the directory of asm which is at RV_ROOT/testbench/asm.
7. Now to run the test through Verilator you can use the Makefile for doing so run the following commands.
   % export RV_ROOT=path/to/swerv/core
   % make -f $RV_ROOT/tools/Makefile verilator debug=1 TEST=name-of-asm-file
   Now the test should and it will generate a sim.vcd file for debugging the waveforms.
   For more details about running core in different configurations and to install the prerequisites please visit
   https://github.com/chipsalliance/Cores-SweRV-EL2

sample code files are provided for reference.
https://github.com/merledu/Rev-Soc/blob/master/core/testbench/asm/External_interrupts.s
https://github.com/merledu/Rev-Soc/blob/master/core/testbench/asm/spi_tb.s
https://github.com/merledu/Rev-Soc/blob/master/core/testbench/asm/timer_tb.s