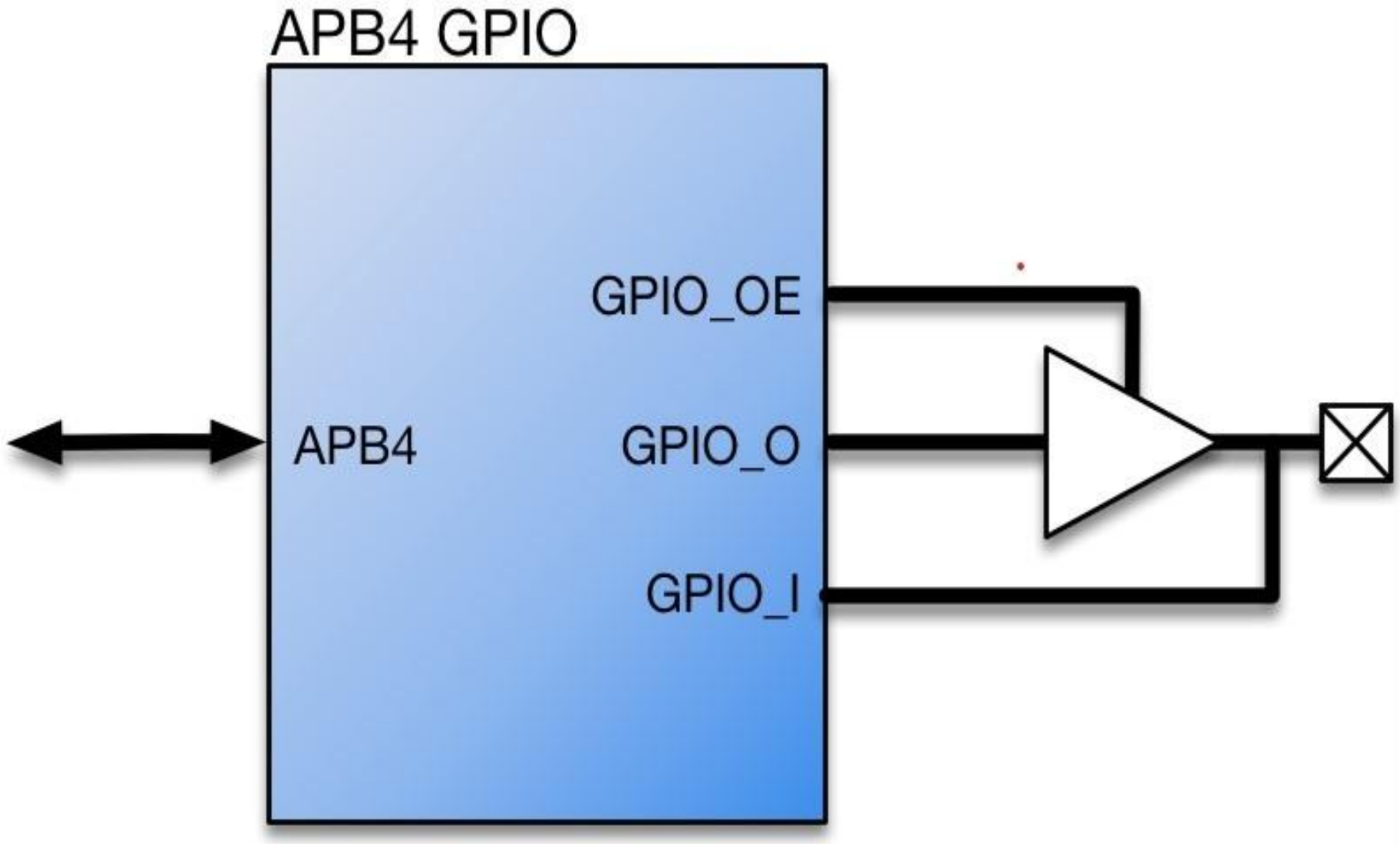
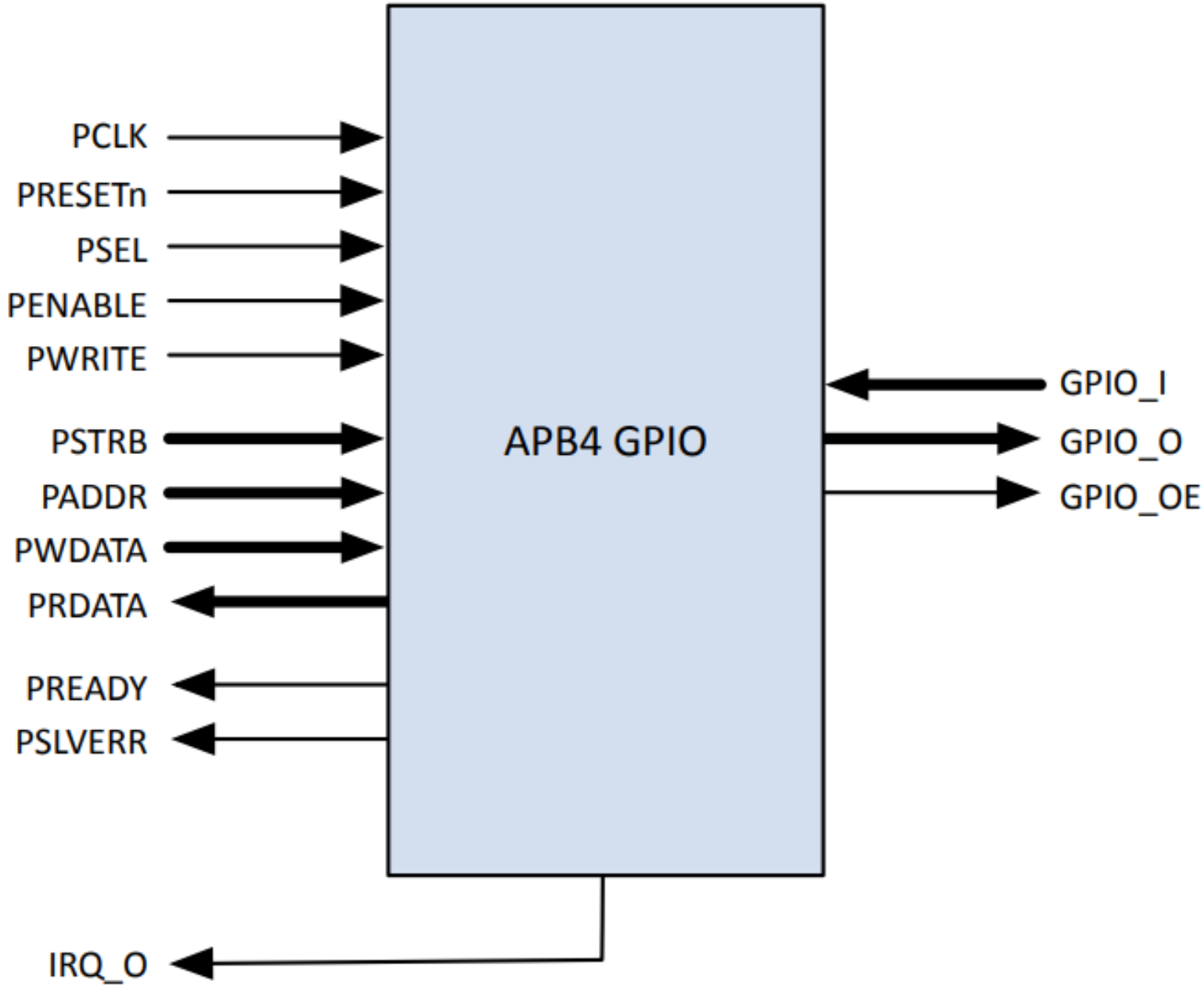
GPIO

General Purpose Input output (Fully parametrized)


APB4 GPIO
GPIO_OE
APB4
GPIO_O
GPIO_I


PCLK
PRESETn
PSEL
PENABLE
PWRITE
PSTRB
PADDR
PWDATA
PRDATA
PREADY
PSLVERR
IRQ_O
APB4 GPIO
GPIO_I
GPIO_O
GPIO_OE

PARAMETERS

PARAMETER	TYPE	DEFAULT	DESCRIPTION
GPIO_PINS	INTEGER	32	APB data bus and GPIO
STAGES	INTEGER	2	Number of input stages

REGISTER MAP

Register	Address	Access	Function
MODE	Base + 0x0	Read/Write	Push-Pull or Open-Drain Mode
DIRECTION	Base + 0x1	Read/Write	Output Enable control
OUTPUT	Base + 0x2	Read/Write	Output Data Store
INPUT	Base + 0x3	Read Only	Input Data Store
TRIGGER_TYPE	Base + 0x4	Read/Write	Trigger Type
TRIGGER_LVL0	Base + 0x5	Read/Write	Trigger Sense 0
TRIGGER_LVL1	Base + 0x6	Read/Write	Trigger Sense 1
TRIGGER_STATUS	Base + 0x7	Read/Write	Trigger Status
IRQ_ENABLE	Base + 0x8	Read/Write	Enable Interrupts

APB4 INTERFACE OF GPIO

Port	Size	Direction	Description
PRESETn	1	Input	Asynchronous active low reset
PCLK	1	Input	Clock Input
PSEL	1	Output	Peripheral Select
PENABLE	1	Output	Peripheral Enable Control
PWRITE	1	Output	Write Select
PSTRB	GPIO_PINS/8	Output	Byte Lane Indicator
PADDR	GPIO_PINS	Output	Address Bus
PWDATA	GPIO_PINS	Output	Write Data Bus
PRDATA	GPIO_PINS	Input	Read Data Bus
PREADY	1	Input	Transfer Ready Input
PSLVERR	1	Input	Transfer Error Indicator

MODE

MODE[n]	Operating Mode
0	Push-Pull
1	Open Drain

DIRECTION

DIRECTION[n]	Direction
0	Input
1	Output

TRIGGER TYPE

TRIGGER_TYPE[n]	Type
0	Level
1	Edge

TRIGGER LVL0

TRIGGER_LVL0[n]	Level Triggered	Edge Triggered
0	no trigger when low	no trigger on falling edge
1	trigger when low	trigger on falling edge

TRIGGER LVL1

TRIGGER_LVL1[n]	Level Triggered	Edge Triggered
0	no trigger when high	no trigger on rising edge
1	trigger when high	trigger on rising edge

TRIGGER STATUS

TRIGGER_STATUS[n]	Status
0	no trigger detected/irq pending
1	trigger detected/irq pending

INTERRUPT REQUEST ENABLE

IRQ_ENABLE[n]	Definition
0	disable irq generation
1	enable irq generation