A NEW AUTOMATIC EXPOSURE SYSTEM FOR DIGITAL STILL CAMERAS

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Abstract

This paper presents a newly developed automatic exposure (AE) system for digital still cameras (DSC). The through the lens (TTL) system which has been employed mainly by conventional camcorders has been applied as an exposure control system for DSCs. However, the TTL system requires a longer time to obtain an appropriate exposure value, and it is therefore not a suitable control method for DSCs which demand immediate imaging after the shutter button is pushed.

The authors have developed a high-precision AE capable of controlling the exposure quickly by converting the brightness of an object directly using the obtained value of an integrated image without using the photometric sensors other than a charge coupled device (CCD). They have also confirmed that the new system enables excellent exposure control without any problem.

I. INTRODUCTION

With the popularization of the personal computers (PC) and the expansion of the internet in recent years, DSCs have become a focus of attention, with diversified DSCs becoming smaller in size and higher in resolution frequency reported [1]-[5]. Since the DSC makes use of the CCD as an imaging devise in addition to conventional film camera technology, it uses the technology of home camcorders. There are two automatic exposure control systems applicable to the DSC: one using several photometric sensors employed in conventional film cameras, and the TTL system used in home camcorders.

In the case of AE using the TTL system, the mechanical iris or an electronic shutter of the CCD is set in advance to enable a continuous change in exposure time, and the integrated value of the obtained image signal is compared with the preset average picture level (APL) using a comparator, and the exposure time is continuously adjusted by using the iris or electronic shutter in order to obtain the desired APL.

Since the conventional TTL system needs a longer time before the appropriate exposure value is obtained, it is necessary to reduce the number of exposure adjustment steps or to increase the time constant of the circuit in order to shorten the time taken for convergence. This, however, causes the exposure adjustment accuracy to deteriorate and hunting to take place, so that the TTL system is not a suitable control system for DSC where the exposure control has to be completed in a short time in order to carry out imaging immediately after the shutter button is pressed.

Furthermore, the CCD has a low dynamic range of less than 4EV (exposure value) compared with silver-halide negative film [6], and therefore performing an exposure control with several photometric sensors calls for higher accuracy in the design than in the silver-halide film camera, so it is disadvantageous from the standpoints of miniaturization and low cost.

The authors have successfully developed a new AE system with high accuracy capable of performing exposure control quickly without using any photometric sensors other than the CCD. This system converts the brightness of the object from the obtained value of the integrated image, and is capable of making exposure controls after minimum feedback.

The remaining part of this paper is organized as follows. The basic principle of the system is given in Section II, the main flow indicating the processing sequence of the CPU in Section III, the system for power saving control in Section IV, and the experimental results in Section V. Finally, in Section VI, conclusions and suggestions for future study are presented.

II. PROPOSED AE SYSTEM

Fig. 1 shows the block diagram of the AE system,

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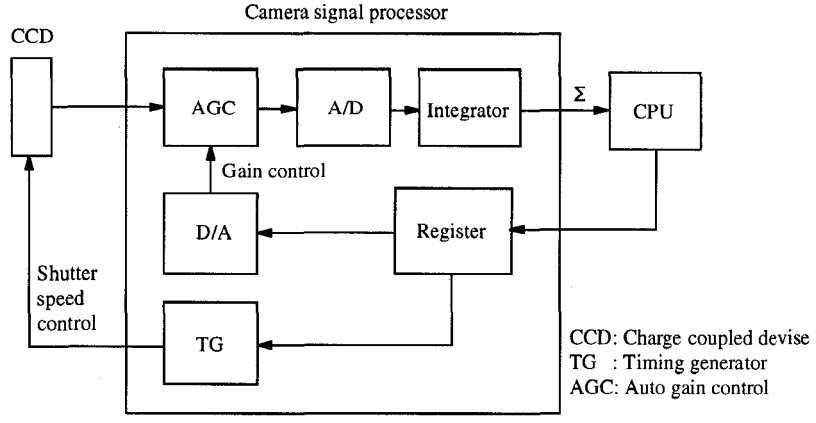


Fig. 1 Block diagram of the AE system

and Fig. 2 the sampling area for AE. In order to reduce the size and weight of the DSC, an electronic shutter system is used instead of a mechanical iris to control the drive pulse to the CCD, and to adjust the exposure by changing the charge storage time of the CCD.

The imaging signal from the CCD is fed into the processor before being subjected to gain control due to the automatic gain control (AGC) circuit. The integrator integrates the AGC output signal per 1 field as the imaging signal data within the sampling area and then, the camera signal processor stores the integrated value in the inner register. The CPU can read out the integrated value by pointing the address of the register.

The CPU calculates the shutter speed and AGC gain for the next image by using the obtained integrated data, and transmits them to the camera signal processor, which then carries out the imaging of the object according to the imaging conditions transmitted from the CPU.

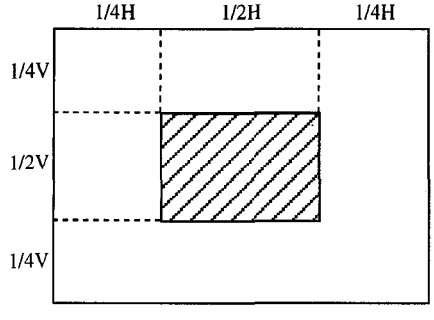


Fig. 2 Sampling aria for AE

In this system the shutter speed and AGC gain are calculated in the following manner. The integrated value of Σ of the imaging video signal can be expressed by equation (1).

$$\Sigma = k1 \times L \times G \times S \qquad (1)$$

Where;
Σ : Integrated value of imaging signal
$k1$: Constant
L : Brightness of the object
G : Gain of the AGC circuit
S : Shutter speed of the CCD

The brightness of the object L can be calculated by using equation (2) as follows.

$$L = \Sigma / (k1 \times G \times S) \qquad (2)$$

In other words the brightness of the object can be calculated by dividing the integrated value by the shutter speed and AGC gain at the time of imaging.

Thus the optimum shutter speed and AGC gain can be immediately set when calculating the brightness of the object, if the shutter speed and AGC gain which match the brightness of the object are set down in a look up table (LUT).

In order to achieve the proposed system easily it is necessary to make up a table of the shutter speed and AGC gain with brightness of the object as the address. However, since the normal illuminance for DSC is several hundred lx (under light inside a room) to several

tens of thousand lx (under a clear sky), an extremely large quantity of memory capacity is needed for addressing the illuminance over a wide range, and it is difficult to make an accurate calculation of the division in equation (2) in a short time even by using the simple CPU (ex. 8bit CPU) in order to calculate the brightness of the object.

The authors have, therefore, set up an LUT as given below to allow composition of the LUT with appropriate memory capacity, and to make the calculation in equation (2) easier.

$$logL = log\ \Sigma - logS - logG - logk1 \qquad (3)$$

The brightness of object L is set to cause exponential change. It is more convenient to carry out conversion as shown in the equation (3) since the exposure value is generally treated in terms of logarithmic value so as to be expressed by the relationship between the object brightness and the F number, etc.

In order to carry out the exposure control complying with the object brightness ranging from 100 lx to 100000 lx, the object brightness Ln is expressed by the equation given below.

$$Ln = (100000/100)^{1/(N-1)} \times L_{(n-1)} \qquad (4)$$

where;
Ln : Brightness of the object with nth address value
N : Address number in LUT
Lo : 100 [lx]

With the object brightness Ln expressed as shown in equation (4), the left-hand side of equation (3) turns into a linear function. Further, since each item on the left-hand side of equation (3) turns into a linear function if both sides of equation (3) are divided by the difference $(logLn - logLn\text{-}1)$ of $log\ L$, i.e. the difference between the minimum value $logLmin$ of $logL$ and the maximum value $logLmax$ of $logL$ divided by the address number, $[(logLmax - logLmin)/(N\text{-}1)]$, so that when the constant C logLo is subtracted, the left-hand side has a value equivalent to the address value from 0 to $N\text{-}1$ as shown in equation (5).

$$\begin{aligned} &Address\ value\ n\ (0, 1, 2, \ldots\ldots, N\text{-}1) \\ &\quad = ClogL - ClogLo \\ &\quad = Clog\ \Sigma - ClogS - ClogG - Clogk1 - ClogLo \\ &\quad = Clog\ \Sigma - ClogS - ClogG - k2 \qquad (5) \end{aligned}$$

Where;
C : $(N\text{-}1)/(logLmax - logLmin)$
$k2$: Constant $[(Clogk1 + ClogLo)]$

The object brightness can thus be expressed in terms of address value by using equation (5), which eliminates the need for a table to express the object brightness. Fig. 3 shows the configurations of LUT.

Address	LUT5
•	•
•	•
•	•
Σm	Clog Σm
•	•
•	•
•	•

Address	LUT1	LUT2	LUT3	LUT4
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
n	Sn	ClogSn	Gn	ClogGn
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•

Fig. 3 Configurations of LUT

The shutter speed S and $ClogS$ corresponding with the address value are set in LUTs 1 and 2, the AGC gain G and $ClogG$ in LUTs 3 and 4, and $Clog\ \Sigma$ with integrated value Σ as the address value in LUT5, and the shutter speed S and AGC gain G are selected from these LUTs to provide optimum exposure corresponding to the object brightness by the obtained integrated value, the shutter speed S, and AGC gain G which were used at the time of imaging.

The relationships between the illuminance, shutter speed, and AGC gain are shown in Fig. 4, with the control system used here being the AE control that gives preference to the shutter speed which gives priority to the S/N.

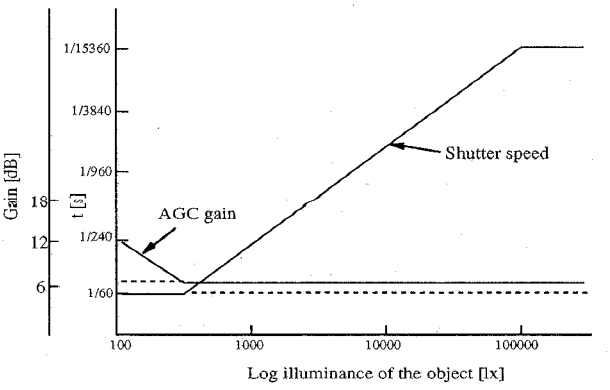


Fig. 4 Relationships between gain and time, and illuminance

As shown in equation (5), this system carries out addition and subtraction only, thus reducing drastically the operational load to the CPU, with the memory capacity used for LUT configurations being 5 × 7 × 8 bit.

III. MAIN FLOW

The main flow chart of processing inside the CPU is shown in Fig. 5, and the exposure control is explained using this flow chart.

First, the imaging (**S1**) is carried out at the initial values of **S0**, **G0** (address **n0**). Next, the integrated value $\sum$ of the image at **S0** and **G0** is read out from the camera signal processor (**S2**). The exposure time is too short when the integrated value $\sum$**m** is less than 1, so that the exposure time is automatically increased to the preset level without going through the operation process (**S4**).

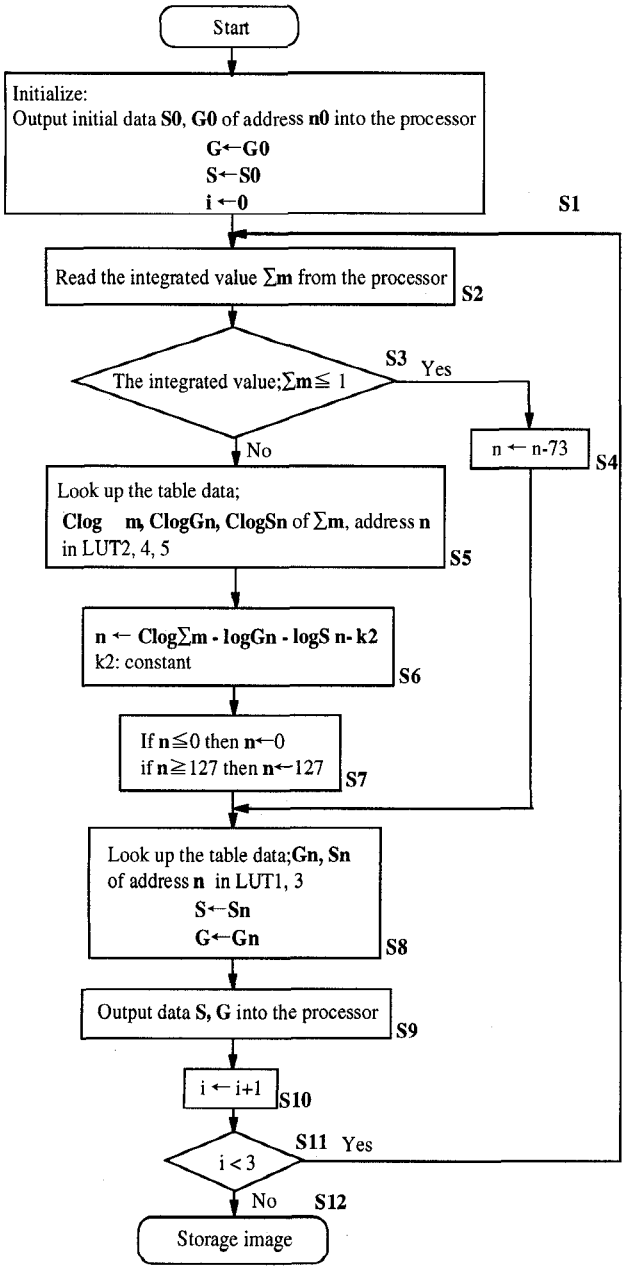


Fig. 5 Main flowchart

Next, **ClogG** and **ClogS** are obtained from the address value **n** (initial address **n0**) with the shutter speed **S** and AGC gain **G** set at the time of imaging, LUT2, and LUT4. Then, **Clog**$\sum$**m** is obtained from the readout integrated value $\sum$**m** and LUT5 (**S5**). The object brightness i.e. the address value **n** (**S6**) is obtained from the **ClogG, ClogS** and **Clog**$\sum$**m** by using equation (5). After confirming the underflow and overflow of **n** (**S7**), the shutter speed **S** and AGC gain **G** are obtained, with the calculated **n** as the address value for LUT1 and LUT3 (**S8**). The obtained shutter speed **S** and AGC gain **G** are then transmitted to the camera signal processor (**S9**).

With the operations **S2 - S9** repeated three times (**S10**, **S11**), the photographed image is stored.

IV. MODE TO REDUCE POWER CONSUMPTION

With the DSC becoming smaller in size and lighter in weight, the demand for small size batteries has accordingly increased, while the general-purpose batteries (LR6, LR03: AA, AAA) also being increasingly used for the sake of convenience. Thus the reduction in power consumption of DSC has become more important.

The newly developed DSC, shown in Fig. 6, is composed of a camera block, and a digital block for processing the image before recording it in the storage medium, each with a separate power supply. The CCD has a high drive voltage, and so the power supply to the

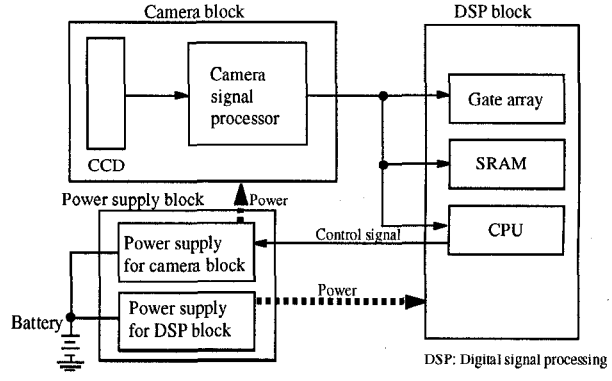


Fig. 6 Block diagram to control power supply

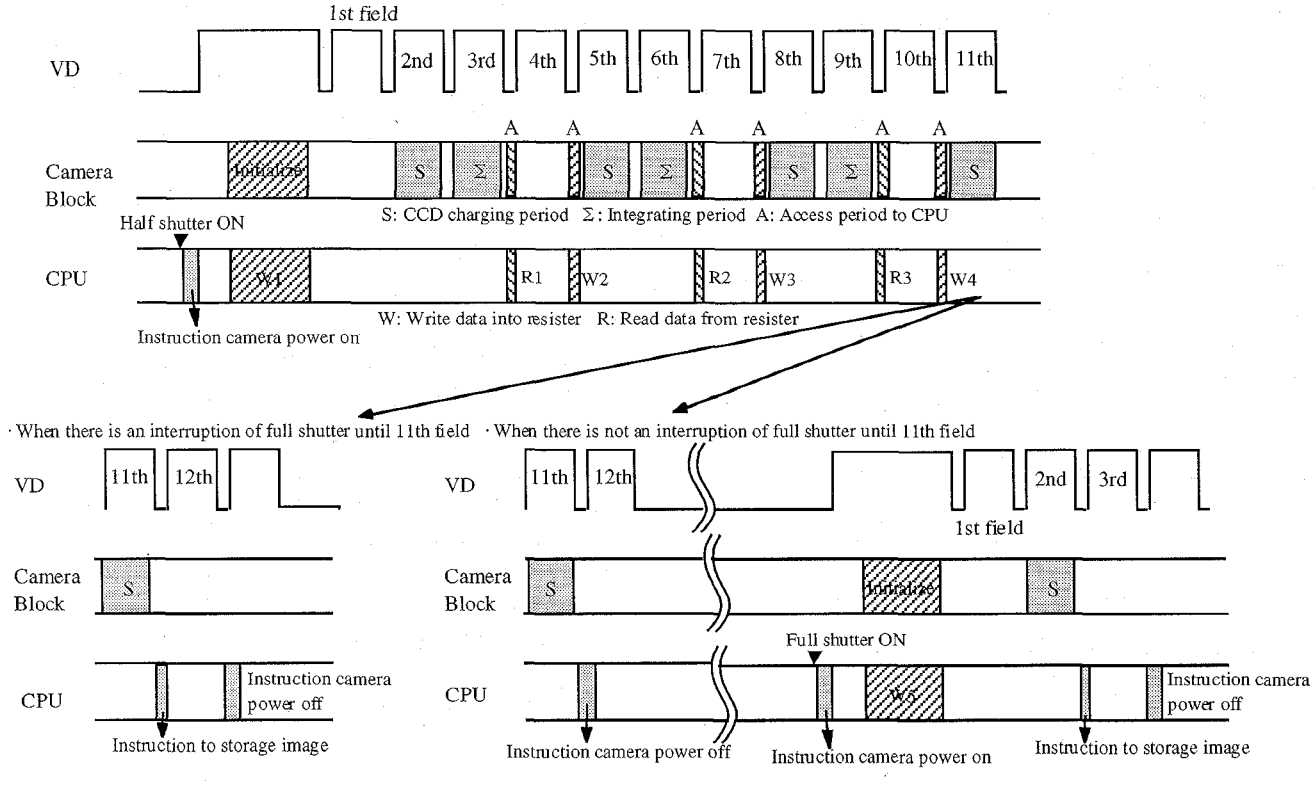


Fig. 7 Timing chart of AE sequential control

camera is cut off at times other than when imaging, thus contributing to a drastic reduction in power consumption.

Furthermore, the DSC camera, like a conventional film camera, is equipped with a two-step shutter button (full shutter and half shutter), and has an AE lock function at half shutter. In this system the camera block functions only during the time the exposure value is obtained in order to reduce the power consumption. The camera, therefore, functions only during the 3-cycle feedback when the exposure is measured, and the power supply for the camera block is cut off if the full shutter button is not pressed during the time.

The power supply control and AE operation are carried out in the following manner. Fig. 7 shows the timing chart of the AE sequential control between the camera block and the CPU.

First, on detecting that the half shutter button is pressed, the CPU turns the power supply for the camera block to 'on', and after the power supply becomes steady in 30 msec, it writes down the initial values (shutter speed S0, AGC gain G0) in the camera signal processor (initialization **W1**). With the power supply turned on and the initialization completed, the camera block starts normal operation. Since the 1st-field after the initialization is not used as a dummy as shown in Fig. 7, the CPU at the 4th VD reads out the integrated value of the imaging data charged in the CCD in the 2nd-field (**R1**). The CPU then calculates the shutter speed S and AGC gain G to provide optimum exposure by using these readout integrated data, and the shutter speed S and AGC gain G set at **W1** as shown in Section III, and transmits the calculated data to the camera signal processor at the 5th VD (**W2**).

The CPU repeats the read/write operations two more times (**R2, W3, R3, W4**), and on detecting that the full shutter button is pressed, it transmits a command to the gate array (G/A) to take in the image photographed with the shutter speed S and AGC gain G set in the **W4**, and on receiving the 'image take-in end' signal from the G/A, the CPU turns the power supply to the camera block to 'off'.

In case the full shutter button is not pressed until the VD after **W4** writing, the CPU keeps in memory the shutter speed S and AGC gain G before turning the power supply for the camera block to 'off'. Once the

full shutter button is pushed, the CPU turns the power supply for the camera block to 'on' again as shown in Fig. 7, then initializes the camera signal processor with the shutter speed S and AGC gain G of **W4** intact as stored (**W5**). The image is taken in after the 3VD dummy field is activated. The power supply for the camera block turns to 'off' when the 'image take-in end' signal is transmitted to the CPU from the G/A.

In summary, this AE operation sets the "locked" state when the half-shutter button is pressed. Moreover, turning the power supply for the camera block to 'on/off' by the AE operation contributes to a reduction in power consumption.

V. EXPERIMENTAL RESULTS

The authors carried out field tests under diverse environmental conditions, with the experimental results given below.

In the outdoor field tests, they were able to confirm that excellent exposure values were obtained causing no overexposure or underexposure. Experiments were made under conditions of different illumination of various objects in order to carry out quantitative calculations of any error in respect of an appropriate exposure. Assuming that halogen lamps were used as the illumination under sunshine and a gray-scale chart as the object. The images are shown in Fig. 8, and the results in Table 1. The images in Fig. 8 are raw data before color separation and gamma compensation, so the images are uneven and displaying poor gradation in low luminance area. Results in Fig. 8 showed no overexposure or underexposure of images, and were within the optimum exposure latitude.

Σ is the mean value of the integrated image data in the sampling area as shown in Fig. 2, and should be preferably set to *48* [48/255(8 bit)] in this system, while the error is obtained by using the equation (6) given below.

$$Error = 100 \times (1 - \Sigma / 48) \qquad (6)$$

Next, testing was carried out under a fluorescent lamp, since flicker influences to measure the exposure [7],[8]. The experimental results are shown in Tables 2 and 3. Fluorescent lamps of 50 Hz and 60 Hz were used, while a white chart and a color bar chart were employed as the objects. Errors ware within 11% under the influence of flicker.

Table 1 Exposure error under halogen lamp

ND filter	Illuminance[lx]	Integrated value Σ	Error[%]
ND0	27000	46.1	-3.96
ND2	13500	45.8	-4.58
ND4	6750	40.0	-16.67
ND8	3375	40.3	-16.04
ND16	1688	41.9	-12.71
ND32	844	41.6	-13.33
ND64	422	43.2	-10.00
ND128	211	52.2	8.75

Error max = -16.7[%]

ND: neutral density filter (ND n = attenuation rate 1/n)

Table 2 Exposure error under 50Hz fluorescent lamp (in eastern region in Japan)

3100K

Take number	Chart A		Chart B		Chart C	
	Σ	Error[%]	Σ	Error[%]	Σ	Error[%]
1	43.4	-9.58	48.2	0.42	48.2	0.42
2	44.5	-7.29	49.8	3.75	50.3	4.79
3	44.1	-8.12	49.9	3.96	50.4	5.00
4	45.5	-5.21	49.8	3.75	48.6	1.25
5	44.2	-7.92	47.8	-0.42	50.5	5.21
6	44.9	-6.46	51.0	6.25	51.5	7.29
7	48.0	0.00	52.4	9.17	51.6	7.50

5100K

Take number	Chart A		Chart B		Chart C	
	Σ	Error[%]	Σ	Error[%]	Σ	Error[%]
1	43.6	-9.17	49.4	2.81	48.1	0.21
2	44.6	-7.08	47.0	-2.19	49.0	2.08
3	43.9	-8.54	48.6	1.25	47.9	-0.21
4	45.4	-5.42	49.1	2.29	49.1	2.29
5	50.7	5.63	49.5	3.13	48.9	1.88
6	45.9	-4.38	47.5	-1.04	49.1	2.29
7	44.8	-6.67	47.0	-2.08	49.5	3.13

Error max = -9.2[%]

Chart A : White chart (4000lx) , Chart B : White chart + ND4, Chart C : Color bar chart

Table 3 Exposure error under 60Hz fluorescent lamp (in western region in Japan)

3100K

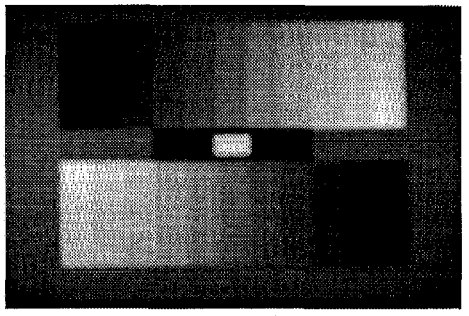
Take number	Chart A		Chart B		Chart C	
	Σ	Error[%]	Σ	Error[%]	Σ	Error[%]
1	44.5	-7.29	50.1	4.38	49.2	2.52
2	46.5	-3.13	48.9	1.88	46.7	-2.71
3	47.5	-1.04	49.6	3.33	49.7	3.54
4	49.3	2.71	51.1	6.46	47.7	-0.62
5	44.7	-6.88	51.5	7.29	47.5	-1.04
6	47.6	-0.83	49.6	3.33	48.8	1.67
7	46.6	-2.92	49.8	3.75	48.3	0.62

5100K

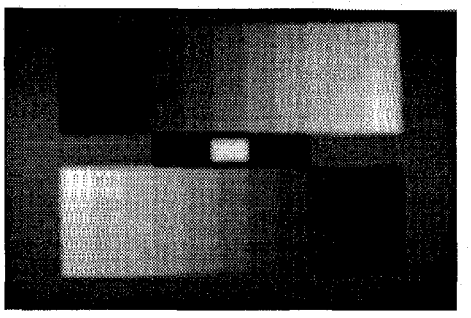
Take number	Chart A		Chart B		Chart C	
	Σ	Error[%]	Σ	Error[%]	Σ	Error[%]
1	45.1	-6.00	48.4	0.83	51.9	8.13
2	47.0	-2.08	48.8	1.67	51.9	8.13
3	49.2	2.50	51.1	6.46	49.3	2.71
4	48.5	1.04	53.4	11.25	50.0	4.17
5	46.6	-2.92	48.2	0.62	53.0	10.42
6	46.8	-2.50	48.3	0.42	48.6	1.25
7	45.5	-5.21	49.1	2.29	52.6	9.58

Error max = 11.3[%]

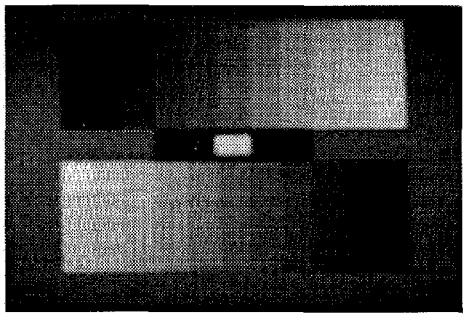
Chart A : White chart (4000lx) , Chart B : White chart + ND4, Chart C : Color bar chart



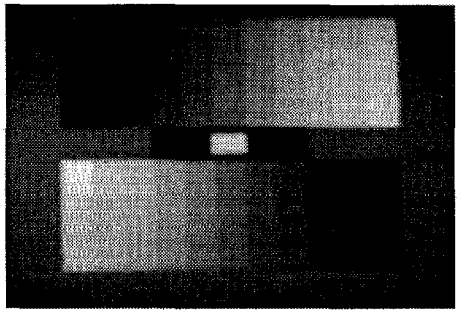
(a) ND0



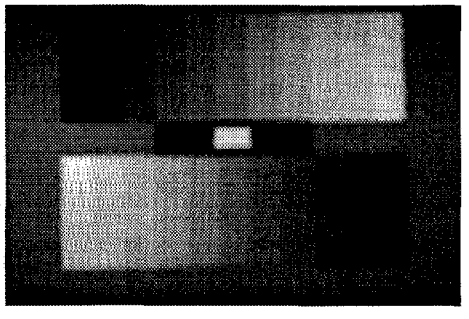
(b) ND2



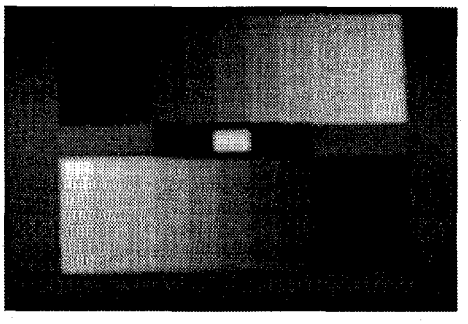
(c) ND4



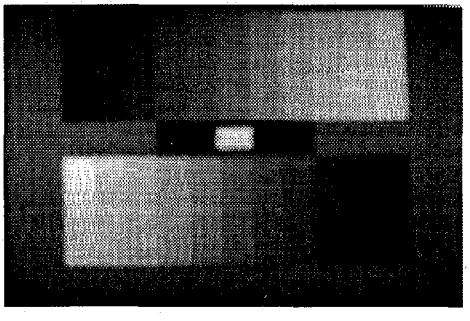
(d) ND8



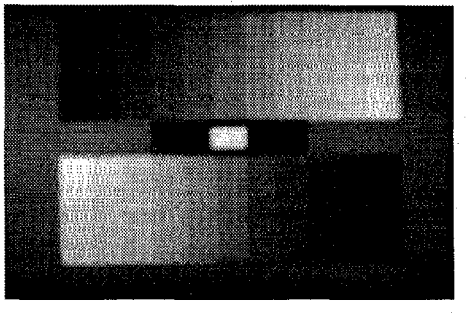
(e) ND16



(f) ND32



(g) ND64



(h) ND128

Fig. 8 Image examples under halogen lamp

VI. CONCLUSION

New algorithms of AE for DSC have so far been proposed. In the newly developed system an appropriate exposure value is obtained by calculating the brightness of the object. It has been found out that the exposure value can be set through simple calculation using logarithmic conversion and preparing the LUT for set values.

This system realizes an AE for the DSC of excellent accuracy, and a shorter imaging time than with the conventional TTL system.

Furthermore, the system showed no overexposure or underexposure of the image due to irregularities of AE, and was found to fall within the optimum exposure latitudes, causing no adverse effects on the image. Following field tests The system was found to realize excellent AE without any problem.

An application S/W exclusively for displaying the image on PC was developed simultaneously with the newly developed DSC. This S/W has the area set in Fig. 2 as in the case of the DSC, and has the gain controlled to allow APL within the area to be constant. This gain control eliminates the AE error mentioned in Section V, and the S/N after the gain controlled by the application S/W is found to cause no problems if the error is within the range given above.

In this system the imaging due to the obtained exposure value is reflected after 2 fields, and the integrated value is obtained after 3 fields, so that it needs 12 fields to take in the image even under the control of 3-cycle (3-times) feedback. The authors are determined to make further study of a system needing a shorter time for the completion of the exposure control.

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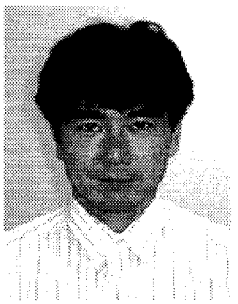
Biography

Tetsuya Kuno received his B.E. degree in electrical engineering from Fukui University, Fukui, Japan, in 1989. He joined Mitsubishi Electric Corporation in 1989, and has been engaged in the research and development of image processing for CCD cameras. He is a member of the ITEJ, IEICEJ, and IS&T.

Hiroaki Sugiura received his B.E. degree from Nagoya University, Aichi, Japan, in 1982 and his Ph.D. degree from Chiba University, Chiba, Japan, in 1995, respectively. He joined Mitsubishi Electric Corporation in 1982 and has been engaged in the research and development of imaging technologies. His current interest is color management technology of multimedia systems and equipment. He is a member of IEEE, IS&T, ITEJ, and CSAJ.



Narihiro Matoba received his B.S. degree in electric engineering from Himeji Institute of Technology, Hyogo, Japan, in 1985. He joined the Computer Works, Mitsubishi Electric Corporation. He was engaged in the development of printers. Since 1990, he has been engaged in research on color image processing at the Information Technology R&D Center. He is a member of IIEEJ.