Name

Uni Degree

Nationality

Address • Tele Nr.

in : linkedin ID here
GitHub Profile: ReiErt

EDUCATION

• Uni name
O3.2024
Computer Engineering, Bachelor of Science
3.1 GPA

• Uni2, if needed 2013

Language Studies, Bachelor of Arts

WORK EXPERIENCE

• Work1 09.2023-03.2024

Roll1 Location

- Description1
- Description2

Maschinenfabrik Reinhausen

09.2022-09.2023

Internship in FPGA Developement in Power Electronics Department

Location

3.5 GPA

- Develope FPGA IP on bare metal in VHDL for synthesis on a Xilinx Zynqberry SoC.
- Test via software: Write testbenches and validate via Modelsim simulations.
- Optimise place & route. Automate bitstream generation with Vivado.
- Hardware testing with oscilloscope & logic analyser.

• Owayo GmbH 2013-2016 and 2017-2022

Translator and Order Manager

Location

- Translate. Front end programming in html.
- Coordinate product sales and production for English and German speaking customer base.

PROJECTS

• Project1 03.2024

Short description of project

- Tools & Tech Used: Modelsim, Vivado, Linux Kernel, Quantis PCIe (Quantum Generator), C, Python
- Sinewave Generator FPGA IP from Block RAM and Cordic Algorithm

02.2023

Analogue Sinewave Generator in desired Frequency

- FPGA IP is used in Load Tap Changer.
- Tools & Tech Used: Zynqberry SoC, Oscilloscope, Logic Analyser, Vivado, Xilinx SDK, Modelsim, Python
- 30x30 LED Arcade Board with WIFI and Custom Games

06.2023

Student Project

- Meet timing constants. Validate PHY. Build bride between hardware & software.
- Tools & Tech Used: ESP32 Microcontroller, RTOS, C++, Oscilloscope, VSC, Logic Analyser

SKILLS AND INTERESTS

Developer Tools and Frameworks: RTOS, Xilinx SDK, Vivado, ISE, Modelsim, VSC, Git, Jira, LaTeX, Linux, CLI Programming/Script Languages: C, C++, VHDL, Python, TCL, Matlab, x86_Assembly, SQL, Bash Languages: French: Intermediate - English/German: Native

City, the 13th of March, 2024