MEC302: Embedded Computer Systems

Theme II: Design of Embedded Computer Systems
Lecture 6 – Input, output and peripheral devices

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Outline

- Input and Output (I/O) Hardware
  - General-purpose digital I/O
  - Pulse width modulation
  - Data interfaces: serial, parallel and buses
- Mechanisms to interact with the external world
  - Interrupts and exceptions
  - Interrupt controllers
  - Interrupt models
- 8051 Architecture (to be used in Lab sessions and assignments)
  - Technical specification/Programming environment/Edsim51 emulator

I/O Hardware

For the controller to operate in the physical world, it needs:

1. Read instructions from the physical memory

- Flash memory, USB interface, etc.;

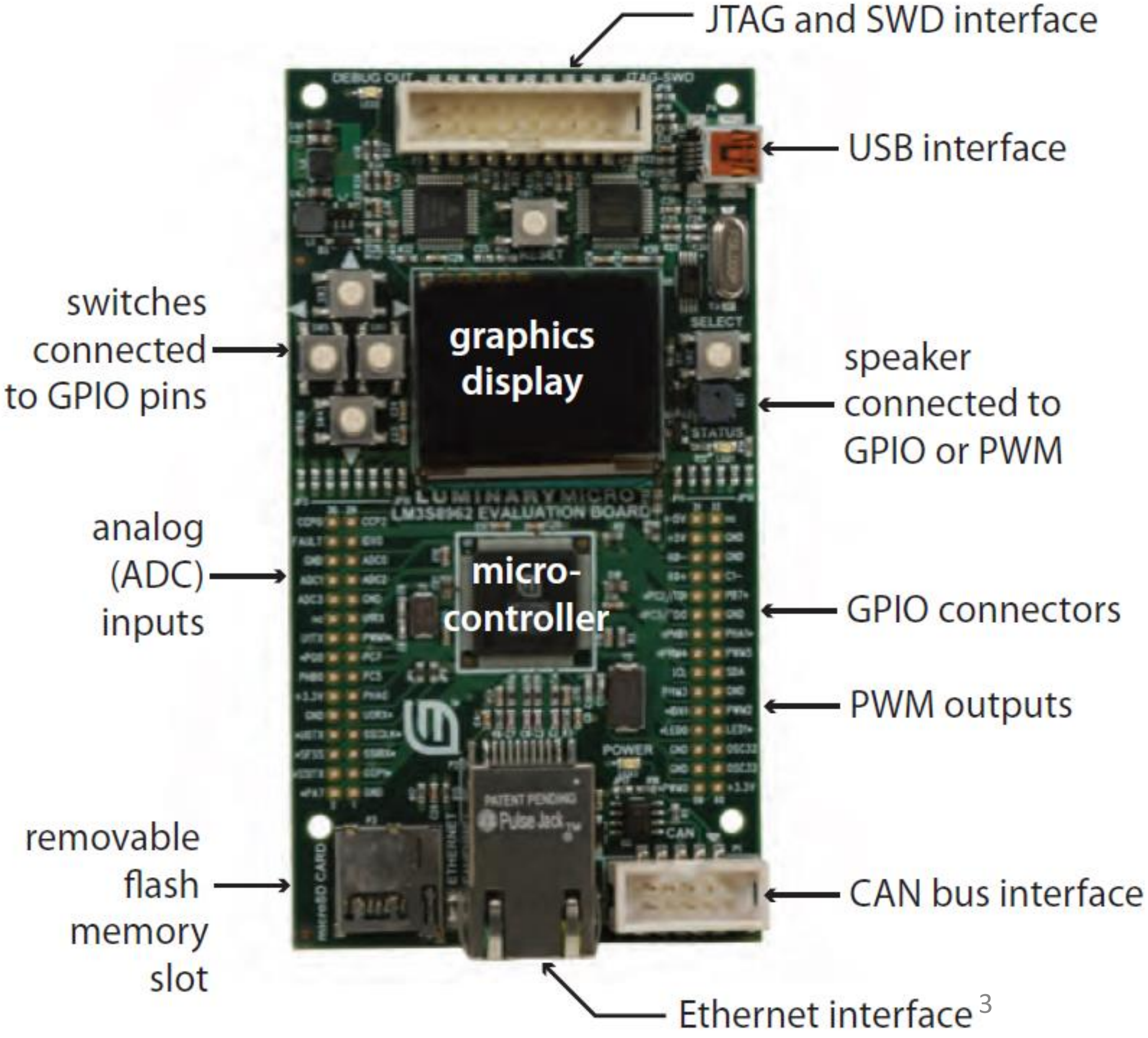
2. For inputs:

- Distinguish discrete voltage levels
  - Convert analog signals to a binary sequence of data (ADC);
  - General purpose input and output (GPIO)
  - Data transfer interfaces (USB, Eth., CAN)

3. For outputs:

- Provide binary output via digital GPIO
- Provide non-binary output through
  - Sequence of bits (GPIOs, DAC);
  - One bit output varying in time (eg, PWM);
  - Data transfer interfaces (USB, Eth., CAN).

#Stellaris LM3S8962 evaluation board:



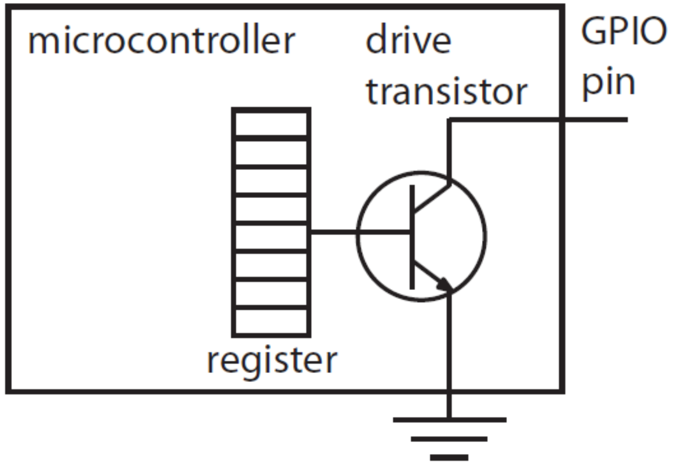
I/O Hardware

General-Purpose Digital I/O

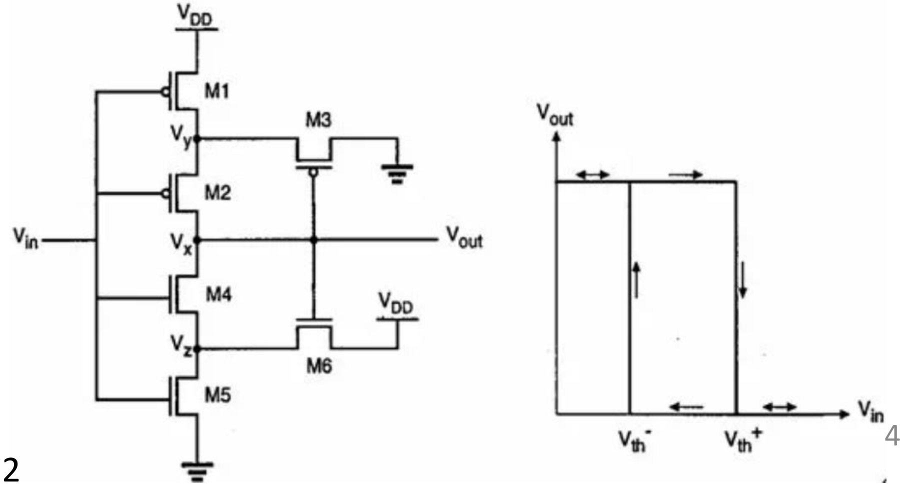
- Represent logical 0 or 1 with an actual voltage level being either 0 or +V (Low or High) – not necessarily respectively;
- When configured as output
  - "Write" to a **Memory-Mapped Register (MMR)** controls the pin voltage from software;
- When configured as input
  - External signal (voltage) "writes" to a register through a circuitry, e.g., **Schmitt trigger** for voltage compatibility and to avoid chattering

Input and output current needs to be maintained (eg, via resistors, amplifiers and isolators).

#GPIO output configuration (ie, open collector):



GPIO input configuration (ie, Schmitt trigger) [1]:



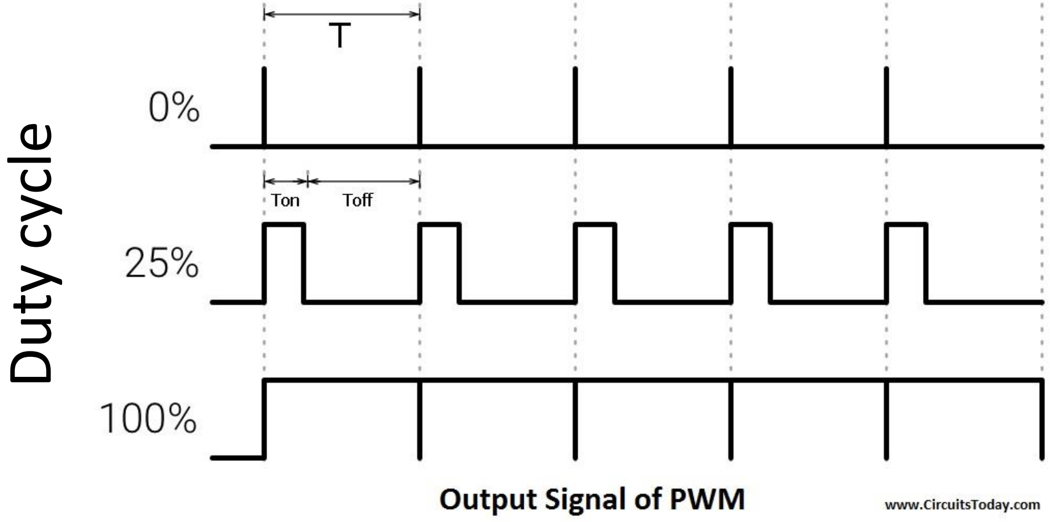
[1] Sequential CMOS and NMOS Logic Circuits, https://slideplayer.com/slide/3942472

I/O Hardware

Pulse width modulation (PWM) – binary output periodic signal of variable duration;

- The main PWM characteristics are:
  - Output frequency;
  - Duty cycle.
- Technique for delivering a variable amount of power to control external devices, e.g.:
  - Speed of electric motors;
  - Brightness of LED and incandescent light;
  - Temperature of a heating element;
  - Other devices that tolerate rapid changes in voltage and current.

PWM signal:



#Consider a resistive heating element.

The amount of power supplied by PWM:

$$P = \frac{T_{Duty}}{T} \cdot \frac{V^2}{R},$$

where T_{Duty} can be flexibly varied.

I/O Hardware

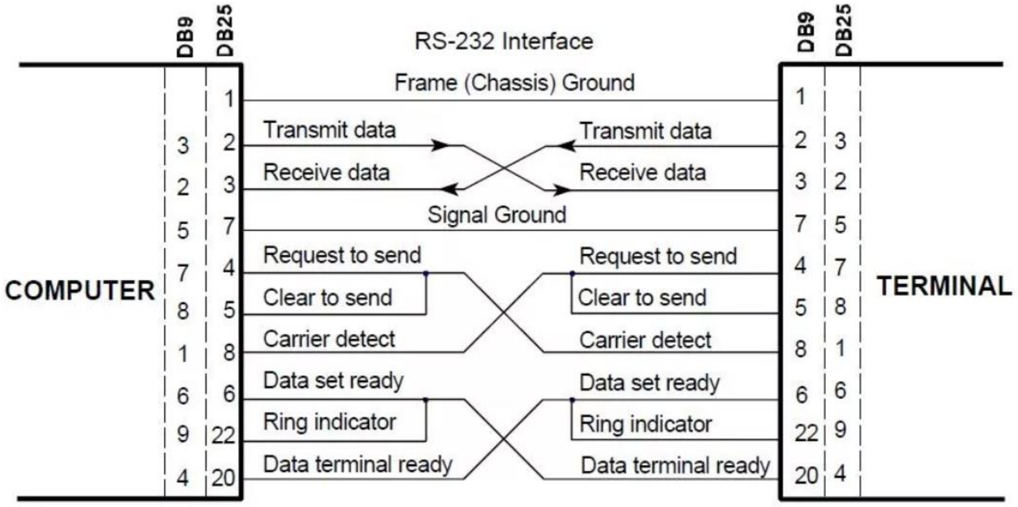
Data interfaces:

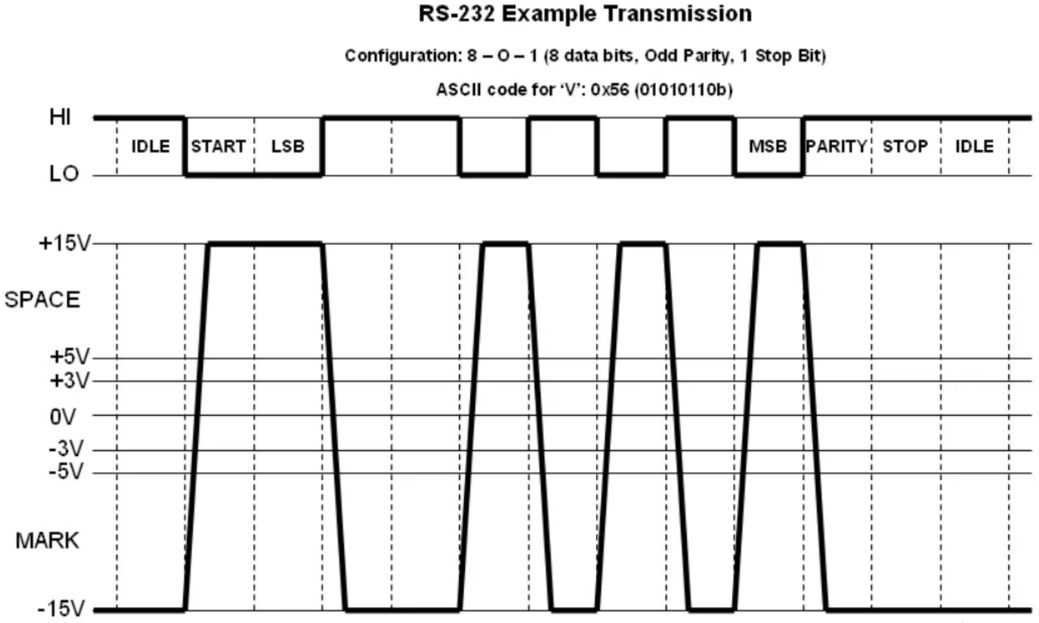
- **Serial interface** sends information (i.e., a byte) point-to-point as a sequence of bits.
  - E.g., RS-232 – is EIA* standard for asynchronous data transfer between two devices:
    - **Universal Asynchronous Receiver/Transmitter (UART)** is a hardware device on a controller to convert 8-bit register into a sequence of bits.

#C program to send a sequence of 10 bytes:

```
for (i = 0; i < 10; i++) {
      while(!(UCSR0A & 0x20));
      UDR0 = x[i];
}
```

- Other serial interfaces are:
  - RS-422/423, 485;
  - Universal Serial Bus (USB);
  - Many others: I2C, PCI, FireWire, MIDI,…





RS-232 Example Transmission
Configuration: 8 – O – 1 (8 data bits, Odd Parity, 1 Stop Bit)
ASCII code for 'V': 0x56 (01010110b)
HI
LO
IDLE
START
LSB
MSB
PARITY
STOP
IDLE
+15V
SPACE
+5V
+3V
0V
-3V
-5V
MARK
-15V

* - Electronics Industries Association

I/O Hardware

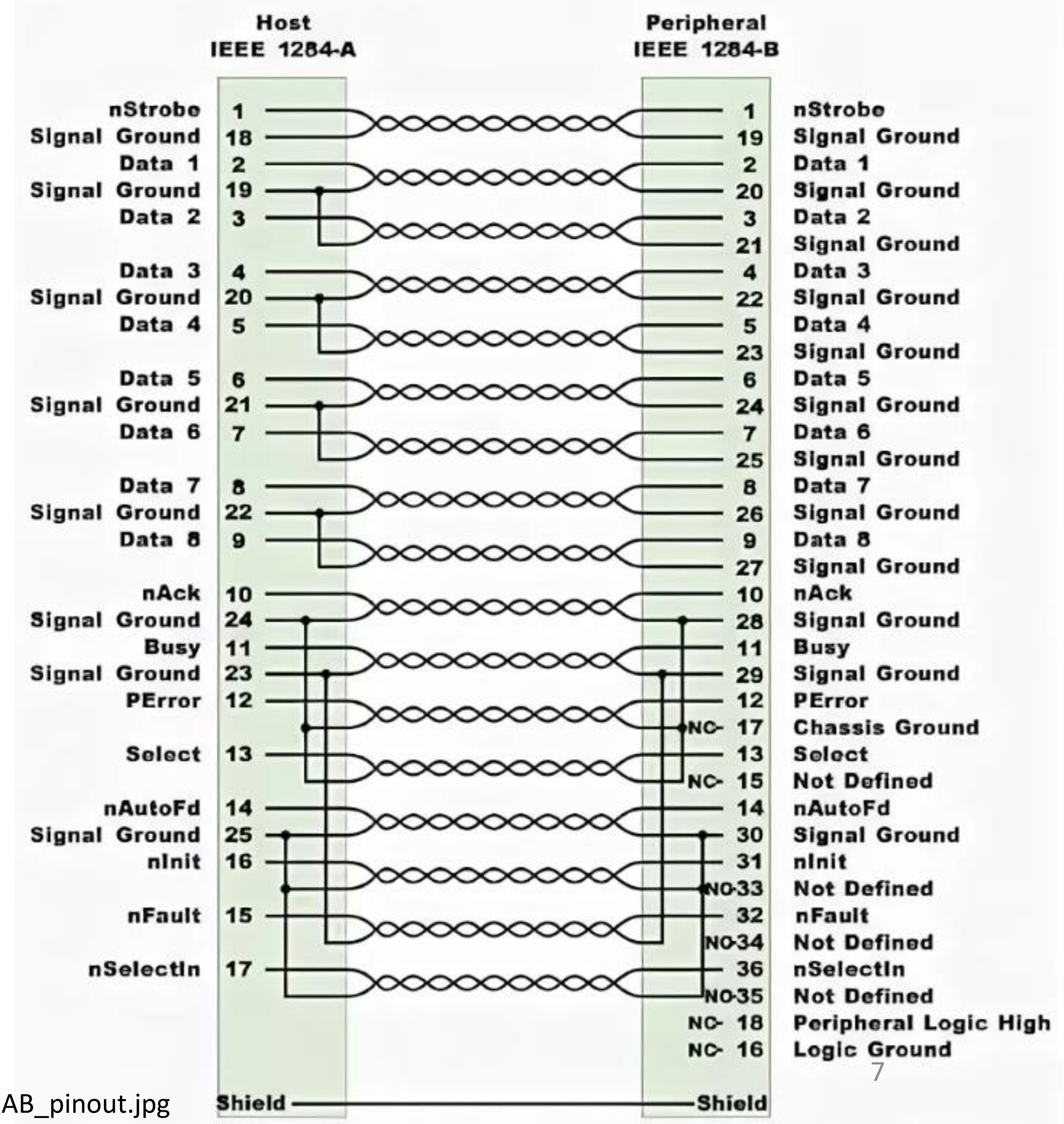
Data interfaces:

- **Parallel interface** uses multiple data lines to simultaneously send bits from point to point
  - IEEE-1284 printer port

They did not find spread use in embedded systems. Compared to serial interfaces, parallel are:

- Conceptually, faster, but not in practice;
- More prone to noise;
- Challenging to maintain synchrony across wires;
- Bulkier, heavier and more expensive.

#IEEE-1284 printer port wiring [4]:



[4] Wikipedia, IEEE1284 Printer Pinout, https://de.wikipedia.org/wiki/Datei:IEEE1284-PrinterCableAB_pinout.jpg

I/O Hardware

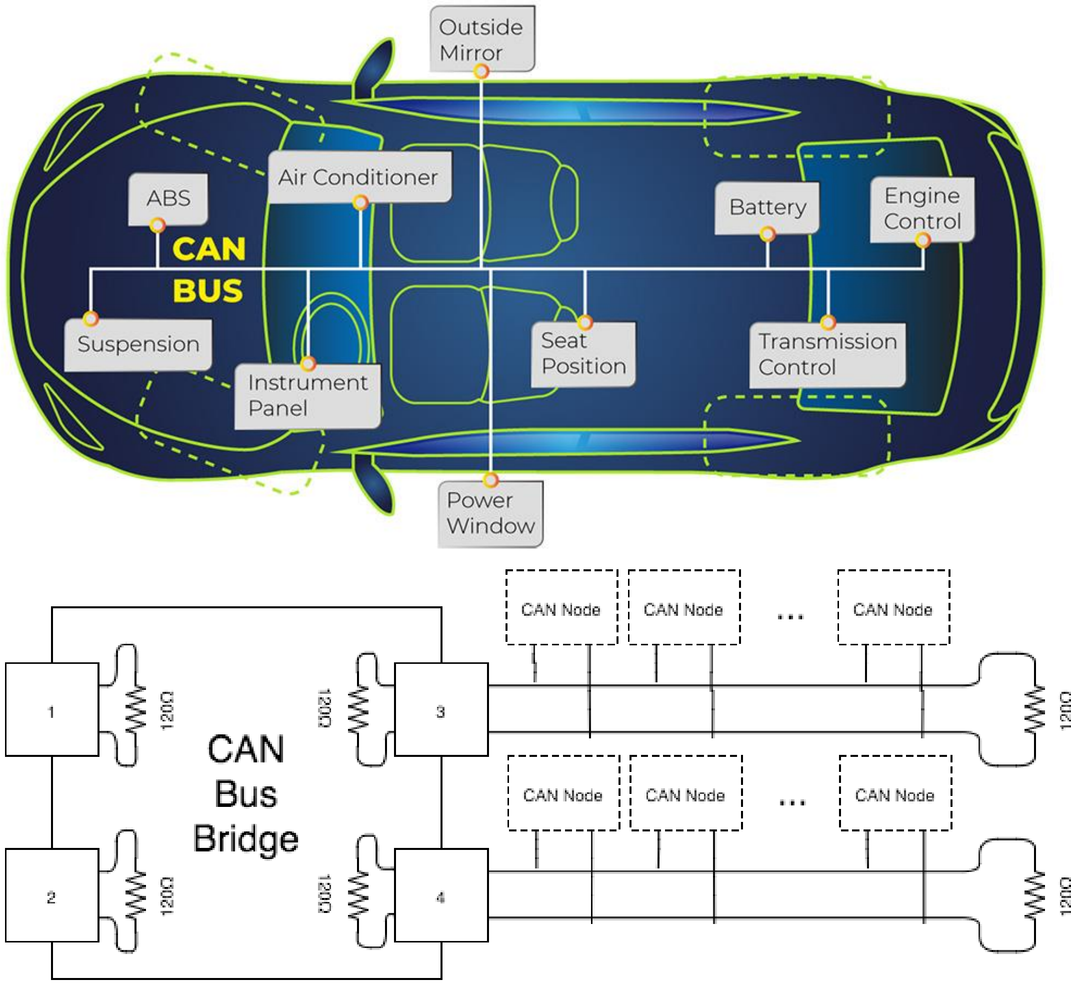
Data interfaces:

- **Bus** is an interface shared among multiple devices (in contrast to a point-to-point connection):
  - **Memory bus** connects **cache** with external **RAM**;
  - **Peripheral buses** (**SCSI, ISA, PCI, ATA**) in computers connect video cards, sound cards and disk drives;
  - Industry buses (Ethernet, PROFIBUS, CAN, etc.).

Communication protocols provide rules for data transmission between devices:

- **Media-access control (MAC)** protocol to arbitrage access to the bus:
  - Master-slaves technology;
  - Time-triggered bus;
  - Token ring
  - Bus arbiter;
  - Carrier Sense Multiple Access (CSMA).

CAN bus illustration [5]:



[5] Can bridge, https://github.com/russery/can_bridge/blob/master/README.md

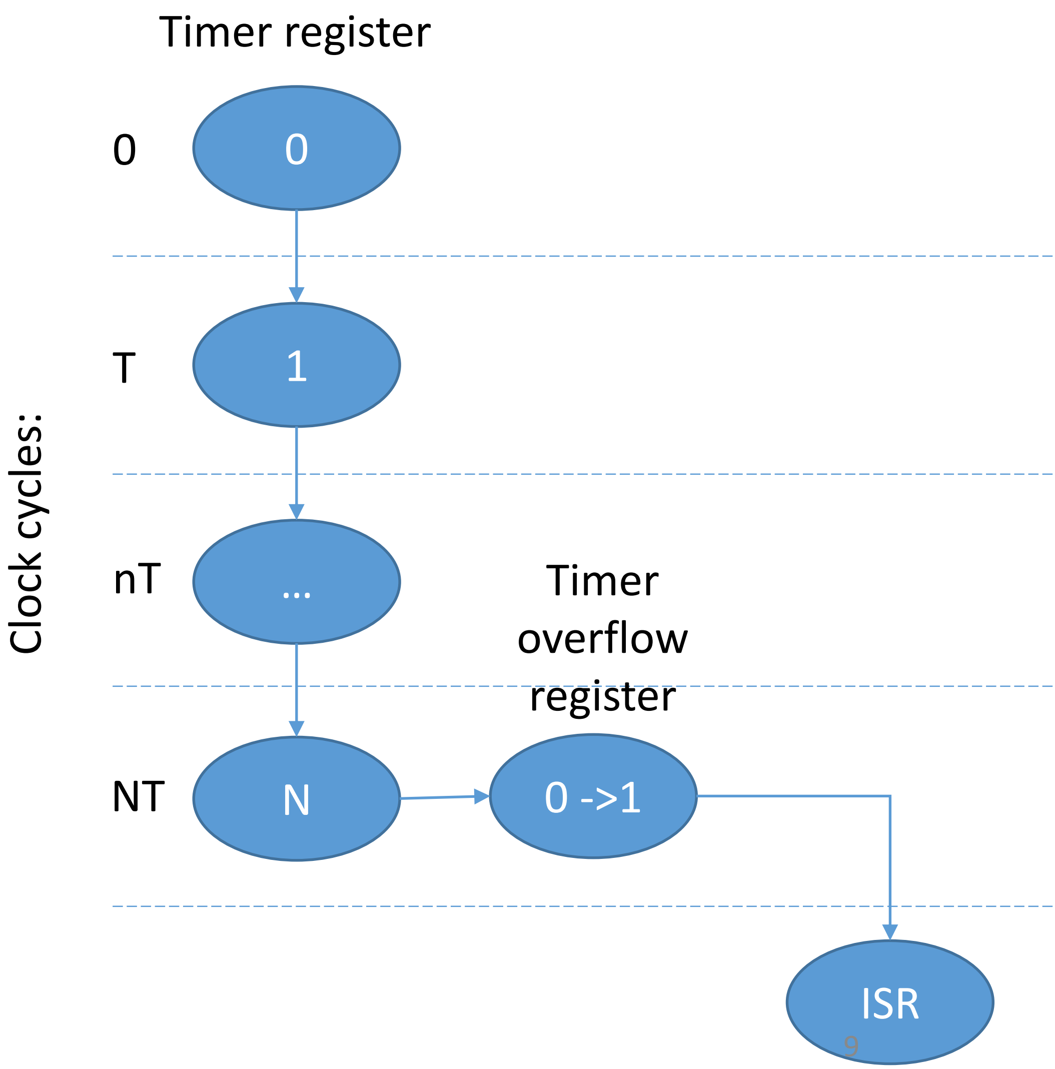
Mechanisms to interact with the external world

Timing and reaction are vital for most embedded applications!

Most (if not all) controllers provide hardware and software mechanisms for immediate reaction to an external signal and precise timing:

- **Interrupts** pause execution of a program for a pre-defined code sequence, i.e., **Interrupt Service Routine (ISR)**. Three kinds of events to invoke ISR:
    - Software – called within currently executed software and/or timer-counter by writing to a MMR;
    - Hardware – called by external signal through an interrupt request line (i.e., specific pin).
    - Exception – internal hardware detects fault (eg, segmentation fault).
- **Timers** count CPU cycles and increment or decrement its MMR (eg, every 12th cycle as in 8051 architecture);
- **Counters** count external events (i.e., voltage level change on a specific pin) and increment or decrement its MMR.

Interrupt triggered by the **timer**:



Timers and counters

Hardware and software implementation of timers is up to a manufacturer. For details, users are referred to µC documentation.

#Let’s consider the manual for a 8051µC [6]:

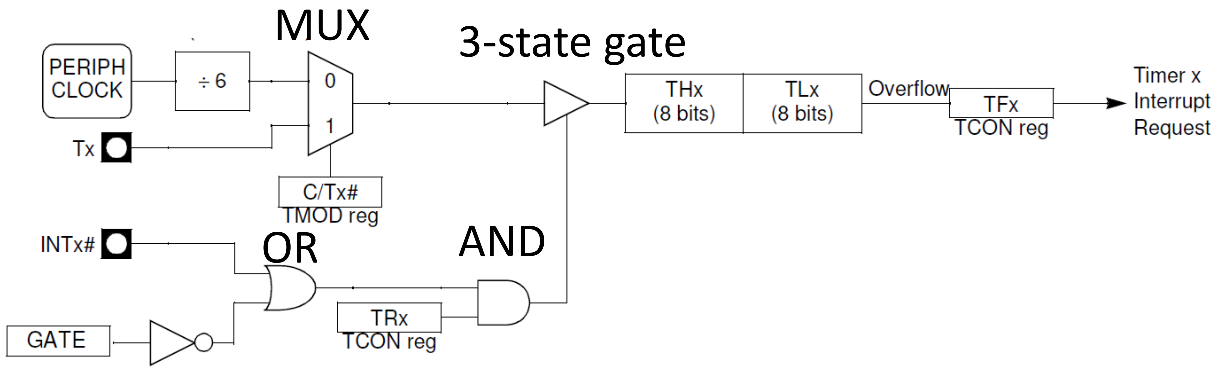
- Two GP 16-bit timers/counters (T0 and T1):

TH0/1	TL0/1

- Each of them has 4 modes (**M0-3**)
- They are configured with the register **TMOD**:

(MSB)			Bits				(LSB)
7	6	5	4	3	2	1	0
Gate	C/T	M1	M0	GATE	C/T	M1	M0
Timer/Counter 1				Timer/Counter 0			

Timer/Counter Mode 1 operation logic [6]:



#Configure and run timers and counters in C:

1. TMOD = 0x61; // Set Timer0 to M1, Counter1 to M2
2. TH0 = 0x3C; TL0 = 0xAF; // Set initial value to 15535;
3. TR0 = 1; // Start Timer0
4. TR1 = 1; // Start Counter1

- Controlled with the register **TCON**:

(MSB)			Bits				(LSB)
7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Timer/ Counter 1		Timer/ Counter 0		Interrupts control			

[6] Atmel 8051 Microcontrollers Hardware Manual, https://www.microchip.com/content/dam/mchp/documents/OTH/ProductDocuments/UserGuides/doc4316.pdf

Interrupt controllers

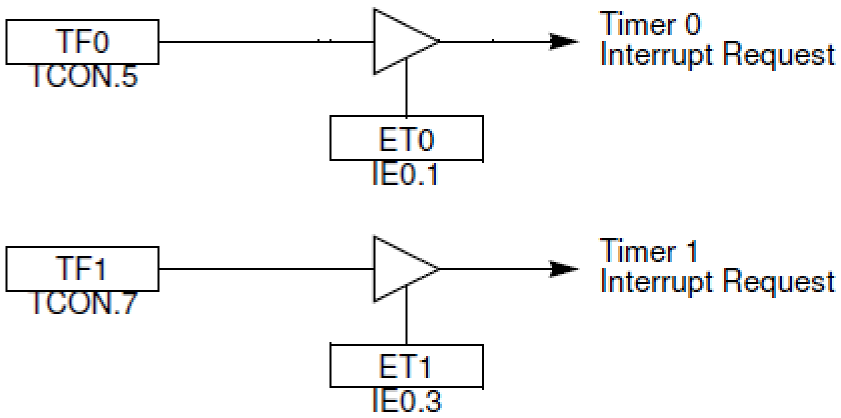
Continuing with the manual for a 8051µC [6], each timer/counter handles one interrupt.

- Interrupts controlled with four **LSB** bits in **TCON** (prev. slide) – internal/external (on/off);
- Interrupts are configured with the register **IE**:

(MSB)			Bits				(LSB)
7	6	5	4	3	2	1	0
EA	X	X	ES	ET1	EX1	ET0	EX0

where EA enables interrupts, ES serial port interrupt, ETx set interrupt by timer x, EXx set external interrupt.

Timer interrupt operation logic [6]:



# Configure interrupt for Timer0 in C:

```
…
void main(void){
  IE = 0x82; // Enable and set interrupt for Timer0
  while(1){ // Do something loop
     …}}

void ISR_name(void) interrupt 1{
  TH0 = 0x3C; TL0 = 0xAF; // Reset timer init value;
  … // Other instructions of ISR
  }
```

[6] Atmel 8051 Microcontrollers Hardware Manual, https://www.microchip.com/content/dam/mchp/documents/OTH/ProductDocuments/UserGuides/doc4316.pdf

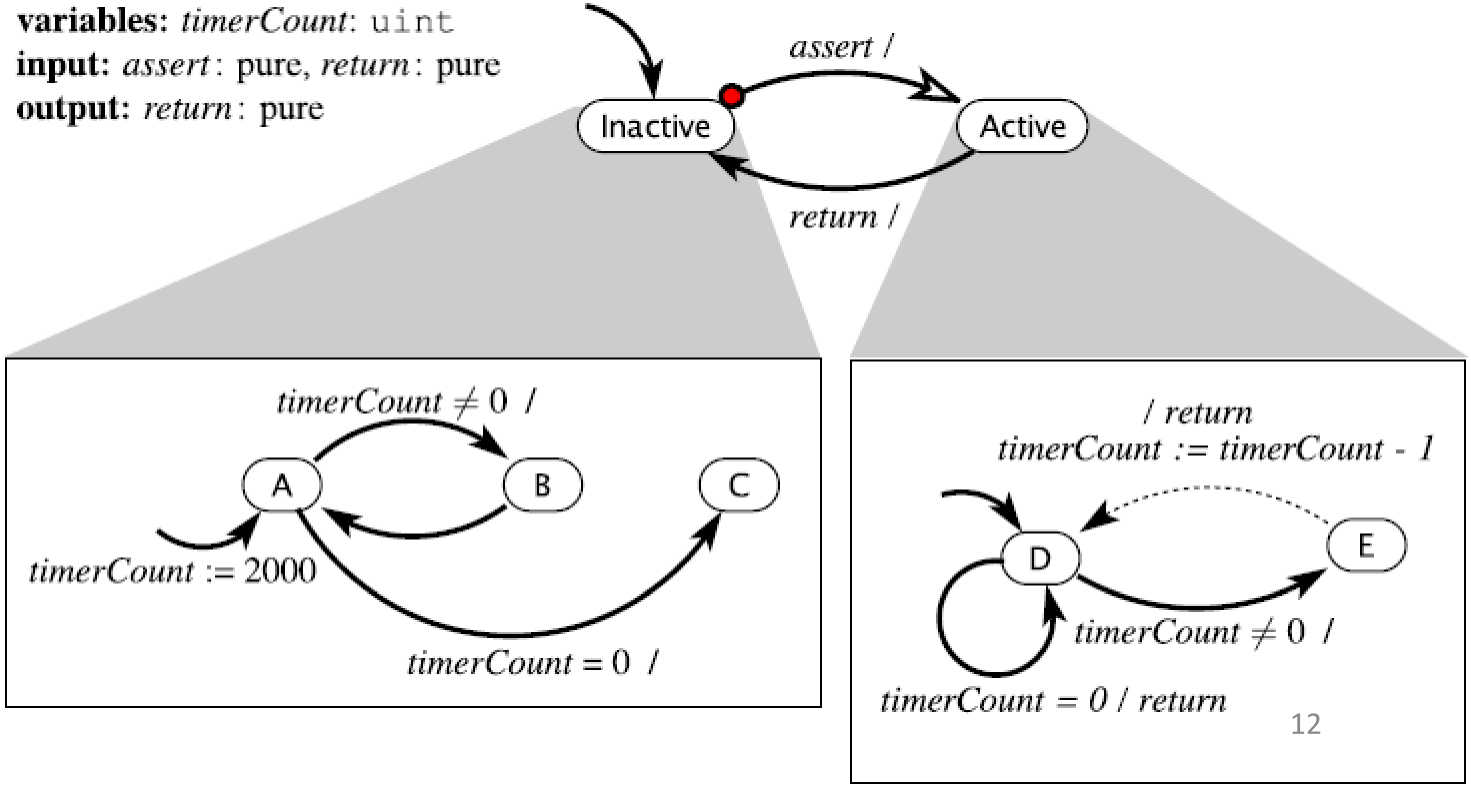
Modelling interrupts

To avoid unexpected behavior - it is important to think about atomicity of the instructions that could be interrupted and variables shared between functions!

Interaction between an ISR and the main program can be represented with Finite State Machines (FSM).

#Consider the following code and its hierarchical FSM:

```
     volatile uint timerCount = 0;
     void ISR(void) {
         … disable interrupts
D→       if(timerCount != 0) {
E→           timerCount--;
         }
         … enable interrupts
     }
     int main(void) {
         // initialization code
         SysTickIntRegister(&ISR);
         … // other init
A→       timerCount = 2000;
B→       while(timerCount != 0) {
          … code to run for 2 seconds
         }
     }
C→   … whatever comes next
```



variables: *timerCount*: uint
input: *assert*: pure, *return*: pure
output: *return*: pure

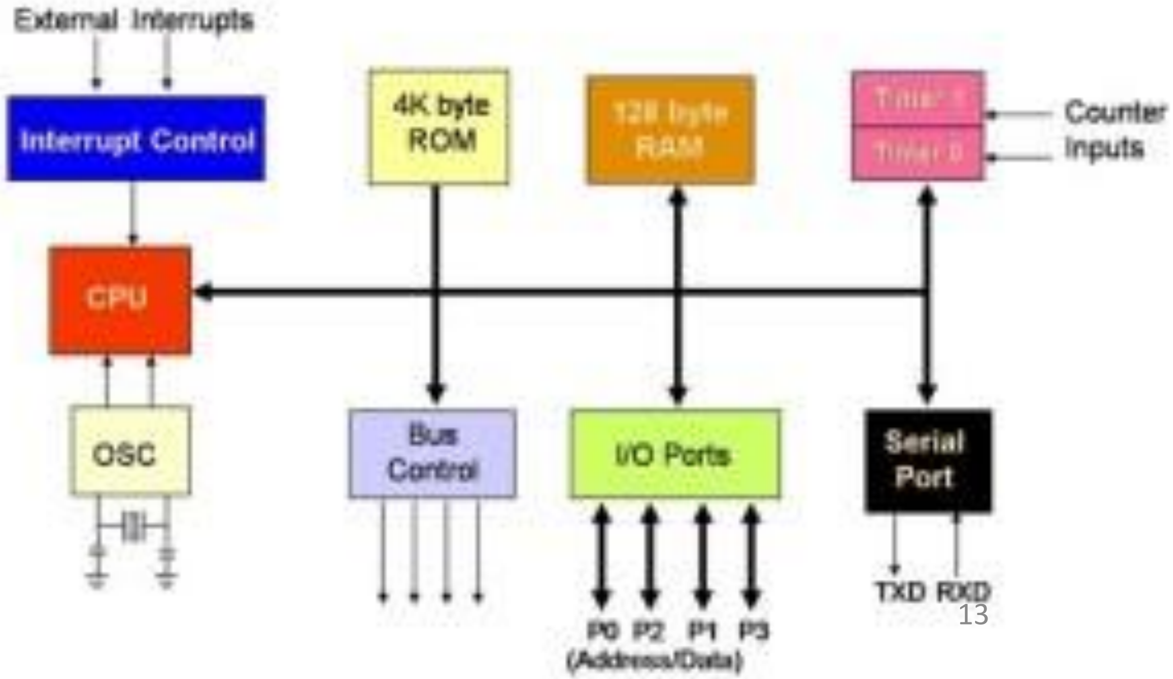
8051 Architecture µC

Technical specification:

- 8-bit CPU with two Registers;
- On-chip oscillator – 12 MHz clock;
- 32 GP I/O (4 groups of 8 pins – P0-P3);
- 4KB ROM for program instructions;
- 128B RAM:
  - 64B special registers (i.e., I/O, timers and peripherals);
  - 64B for operational needs;
- Two 16-bit timers/counters:
  - Timers increment every 12th clock cycle;
- Serial port: Tx and Rx (duplex transmission)
- Five interrupts:
  - 2x peripheral (ext.); 2x timer (int.); 1x data port.

Physical realization – 40-pins DIP:

Block diagram of 8051 µC:



8051 Architecture µC

Programming 8051µC:

- Software (IDE) – **Keil uVision 5**:
  - Officially available online for download (Windows only);
  - In dedicated computer rooms on campus (SD546, SD554, SC375, CBG13);
- Language – Embedded C:
  - Uses syntax and semantics of the C language / global variables not allowed;
  - Additional support: fixed-point arithmetic; named address spaces; I/O hardware addressing.
  - Every program starts with the declaration of 8051µC registers: #include <REG51F.H>
  - Most of the programs (i.e., main functions) run in infinite loop:

```
void main(void){
        while(1){…
}}
```

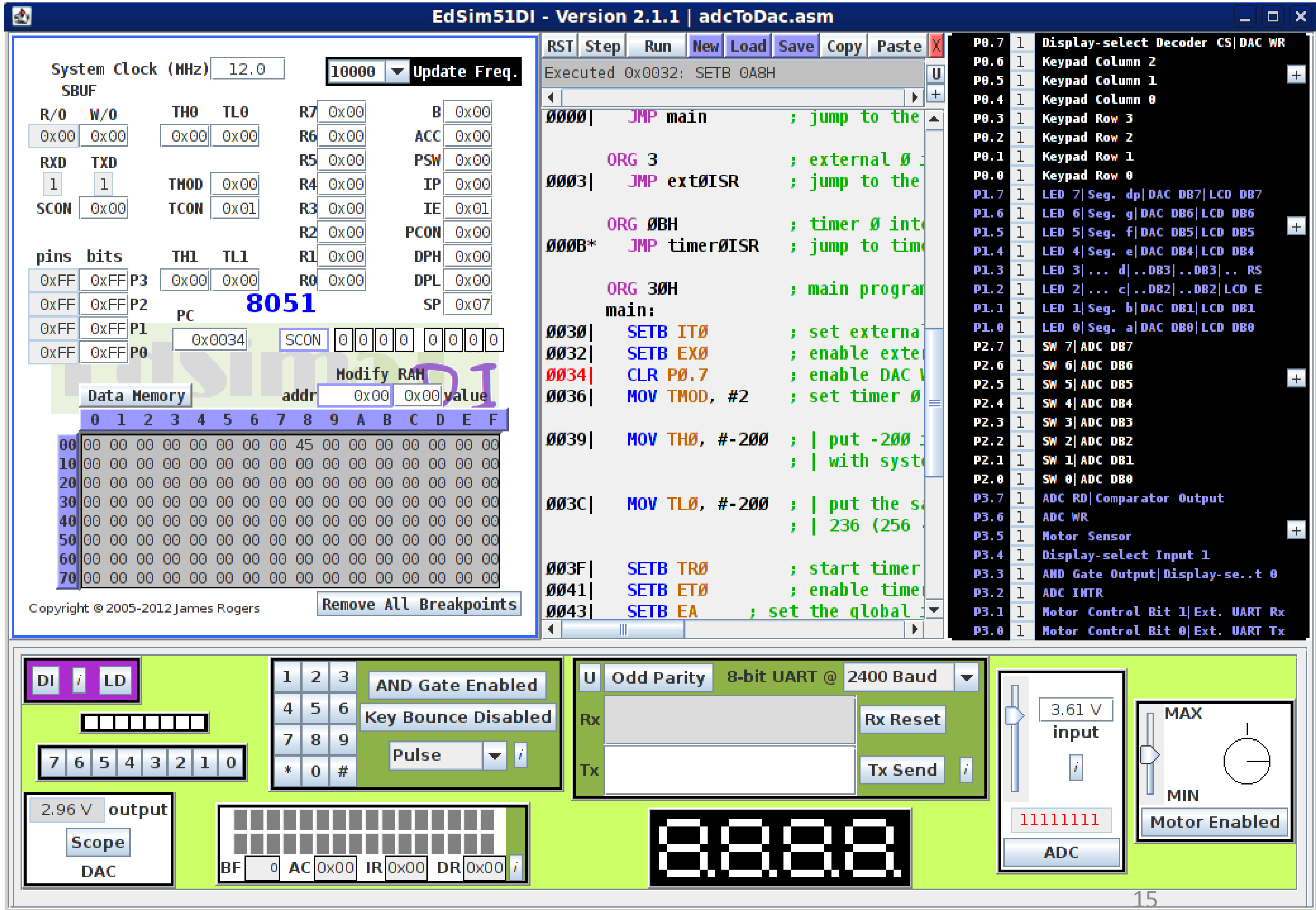
  - Custom functions can be called from the main function or by the interrupts:

```
void func_name(void) interrupt 1{
        …
}}
```

8051 Architecture µC

8051µC emulator:

- Software – EdSim51di:
  - Officially available online for download (Windows only) – Java program;
  - In dedicated computer rooms on campus – can downloaded from the link above.



EdSim51DI - Version 2.1.1 | adcToDac.asm

System Clock (MHz) 12.0

10000 Update Freq.

SBUF									
R/O	W/O	TH0	TL0	R7	0x00	B	0x00		
0x00	0x00	0x00	0x00	R6	0x00	ACC	0x00		
RXD	TXD			R5	0x00	PSW	0x00		
1	1	TMOD	0x00	R4	0x00	IP	0x00		
SCON	0x00	TCON	0x01	R3	0x00	IE	0x01		
				R2	0x00	PCON	0x00		
pins	bits	TH1	TL1	R1	0x00	DPH	0x00		
0xFF	0xFF P3	0x00	0x00	R0	0x00	DPL	0x00		
0xFF	0xFF P2					SP	0x07		
0xFF	0xFF P1	PC							
0xFF	0xFF P0	0x0034							

8051

SCON 0 0 0 0 0 0 0 0

Modify RAM

Data Memory addr 0x00 0x00 value

```
    0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
00 00 00 00 00 00 00 00 00 45 00 00 00 00 00 00 00
10 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
20 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
30 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
40 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
50 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
60 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
70 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
```

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Executed 0x0032: SETB 0A8H

```
0000|    JMP main             ; jump to the
         ORG 3                ; external 0 i
0003|    JMP ext0ISR          ; jump to the
         ORG 0BH              ; timer 0 inte
000B*    JMP timer0ISR        ; jump to time
         ORG 30H              ; main program
         main:
0030|    SETB IT0             ; set externa
0032|    SETB EX0             ; enable exter
0034|    CLR P0.7             ; enable DAC W
0036|    MOV TMOD, #2         ; set timer 0

0039|    MOV TH0, #-200       ; | put -200 i
                              ; | with syste

003C|    MOV TL0, #-200       ; | put the sa
                              ; | 236 (256 -

003F|    SETB TR0             ; start timer
0041|    SETB ET0             ; enable timer
0043|    SETB EA          ; set the global i
```

```
P0.7 1 Display-select Decoder CS|DAC WR
P0.6 1 Keypad Column 2
P0.5 1 Keypad Column 1
P0.4 1 Keypad Column 0
P0.3 1 Keypad Row 3
P0.2 1 Keypad Row 2
P0.1 1 Keypad Row 1
P0.0 1 Keypad Row 0
P1.7 1 LED 7|Seg. dp|DAC DB7|LCD DB7
P1.6 1 LED 6|Seg. g|DAC DB6|LCD DB6
P1.5 1 LED 5|Seg. f|DAC DB5|LCD DB5
P1.4 1 LED 4|Seg. e|DAC DB4|LCD DB4
P1.3 1 LED 3|... d|..DB3|..DB3|.. RS
P1.2 1 LED 2|... c|..DB2|..DB2|LCD E
P1.1 1 LED 1|Seg. b|DAC DB1|LCD DB1
P1.0 1 LED 0|Seg. a|DAC DB0|LCD DB0
P2.7 1 SW 7|ADC DB7
P2.6 1 SW 6|ADC DB6
P2.5 1 SW 5|ADC DB5
P2.4 1 SW 4|ADC DB4
P2.3 1 SW 3|ADC DB3
P2.2 1 SW 2|ADC DB2
P2.1 1 SW 1|ADC DB1
P2.0 1 SW 0|ADC DB0
P3.7 1 ADC RD|Comparator Output
P3.6 1 ADC WR
P3.5 1 Motor Sensor
P3.4 1 Display-select Input 1
P3.3 1 AND Gate Output|Display-se..t 0
P3.2 1 ADC INTR
P3.1 1 Motor Control Bit 1|Ext. UART Rx
P3.0 1 Motor Control Bit 0|Ext. UART Tx
```

AND Gate Enabled

Key Bounce Disabled

Pulse

U Odd Parity 8-bit UART @ 2400 Baud

2.96 V output

BF 0 AC 0x00 IR 0x00 DR 0x00

3.61 V input

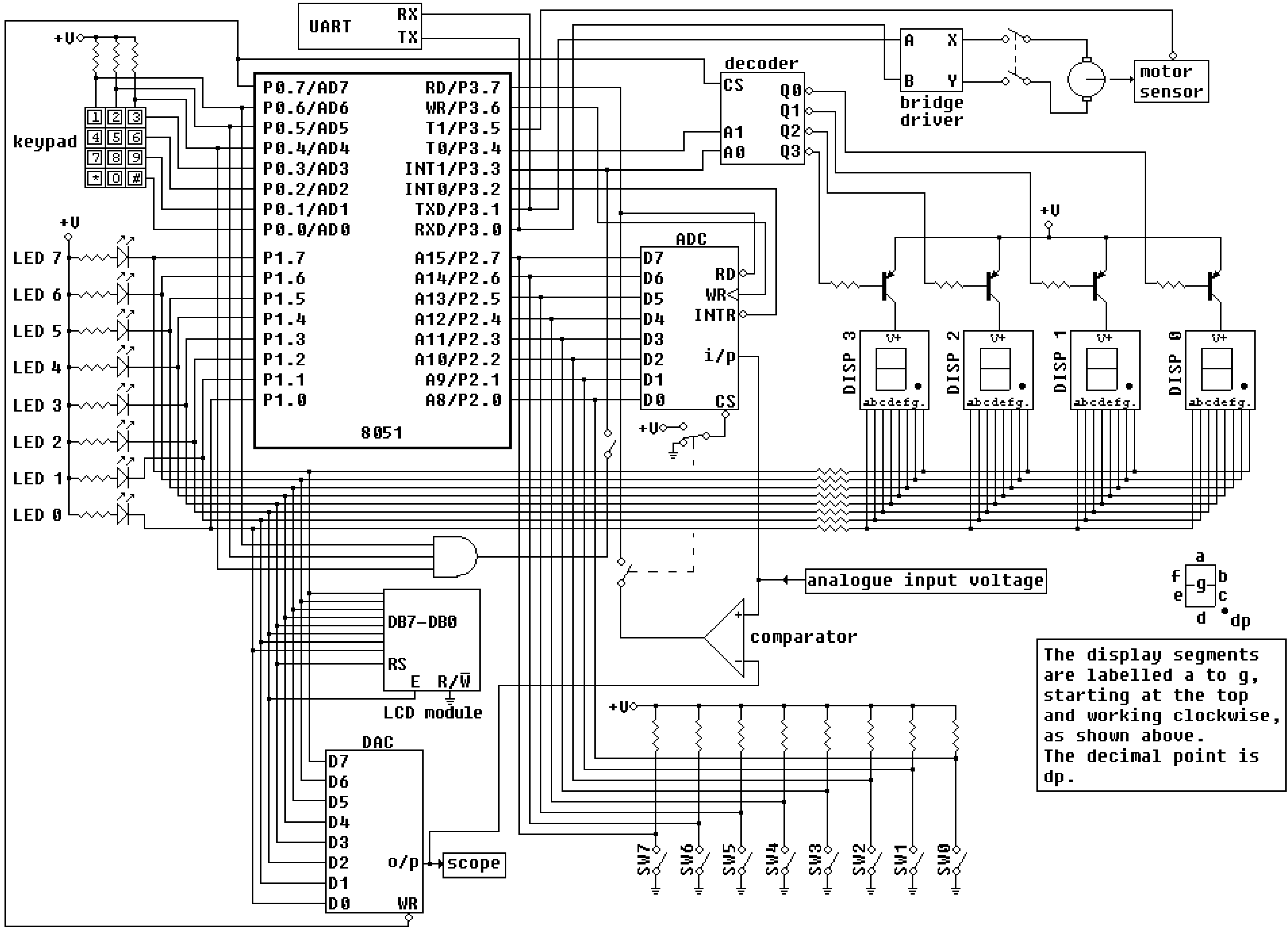
11111111

Motor Enabled

8051 Architecture µC

EdSim51di peripheral logic diagram:

- Analogue-to-Digital Converter (ADC)
- Comparator
- UART
- 4 Multiplexed 7-segment Displays
- 4 X 3 Keypad
- 8 LEDs
- DC Motor
- 8 Switches
- Digital-to-Analogue Converter (DAC) - displayed on oscilloscope



The display segments are labelled a to g, starting at the top and working clockwise, as shown above.
The decimal point is dp.

To sum up

- I/O hardware bridges physical and cyber (computer) worlds;
- µCs mix and match numerous types of I/O hardware:
  - **General-Purpose Digital I/O (GPIO)** – vast application including all below;
  - **Pulse width modulation (PWM)** – deliver variable value (i.e., amount of power) with just a binary state of a signal varying in time;
  - **Serial and parallel interfaces** – provide point-to-point data transfer;
  - **Bus interfaces** – connect multiple devices for data transfer.
- µCs provide hardware and software tools for precise timing and execution of tasks:
  - **Timers** measure internal events (i.e., cycles) for precise timing;
  - **Counters** count the number of external events (i.e., state change of a designated pin);
  - **Interrupts** (almost) instantly response to internal events (timer overflow) or external stimuli to execute predetermined **Interrupt Service Routine (ISR)**.
- **Finite State Machines** can be useful to analyze interactions of the main program and ISR.
- **8051 architecture** accommodates most of the mechanisms available in modern µCs.
- 8051µC can be programmed using **Keil uVision IDE** and tested on **EdSim51di** emulator.

The end!

See you next time – April 3* (optional – mini lecture on Embedded C)

April 10 (next real lecture).

* - Week 8 – reading week.