BeagleBone Black expansion header P8

Pin	CPU Pin	Pin Name	Pin Nummer	Pinmux register offset	mode 0	mode 1	mode 2	mode 3	mode 4	mode 5	mode 6	mode 7	
1	GND												
2	GND												
3	R9	GPMC_AD6		0x818	gpmc_ad6	mmc1_dat6						*gpio1_6	emmc
4	T9	GPMC_AD7		0x81C	gpmc_ad7	mmc1_dat7						*gpio1_7	emmc
5	R8	GPMC_AD2		0x808	gpmc_ad2	mmc1_dat2						*gpio1_2	emmc
6	T8	GPMC_AD3		0x80C	gpmc_ad3	mmc1_dat3						*gpio1_3	emmc
7	R7	GPMC_ADVn_ALE		0x890	gpmc_advn_ale		timer4					*gpio2_2	
8	T7	GPMC_OEn_REn		0x894	gpmc_oen_ren		timer7					*gpio2_3	
9	T6	GPMC_BEn0_CLE		0x89C	gpmc_be0n_cle		timer5					*gpio2_5	
10	U6	GPMC_WEn		0x898	gpmc_wen		timer6					*gpio2_4	
11	R12	GPMC_AD13		0x834	gpmc_ad13	lcd_data18	mmc1_dat5	mmc2_dat1	eQEP2B_in	pr1_mii0_txd1	pr1_pru0_pru_r30_15	*gpio1_13	
12	T12	GPMC_AD12		0x830	gpmc_ad12	lcd_data19	mmc1_dat4	mmc2_dat0	eQEP2A_in	pr1_mii0_txd2	pr1_pru0_pru_r30_14	*gpio1_12	
13	T10	GPMC_AD9		0x824	gpmc_ad9	lcd_data22	mmc1_dat1	mmc2_dat5	ehrpwm2B	pr1_mii0_col		*gpio0_23	
14	T11	GPMC_AD10		0x828	gpmc_ad10	lcd_data21	mmc1_dat2	mmc2_dat6	ehrpwm2_tripzone_input	pr1_mii0_txen		*gpio0_26	
15	U13	GPMC_AD15		0x83C	gpmc_ad15	lcd_data16	mmc1_dat7	mmc2_dat3	eQEP2_strobe	pr1_ecap0_ecap_capin_apwm_o	pr1_pru0_pru_r31_15	*gpio1_15	
16	V13	GPMC_AD14		0x838	gpmc_ad14	lcd_data17	mmc1_dat6	mmc2_dat2	eQEP2_index	pr1_mii0_txd0	pr1_pru0_pru_r31_14	*gpio1_14	
17	U12	GPMC_AD11		0x82C	gpmc_ad11	lcd_data20	mmc1_dat3	mmc2_dat7	ehrpwm0_synco	pr1_mii0_txd3		*gpio0_27	
18	V12	GPMC_CLK		0x88C	gpmc_clk	lcd_memory_clk	gpmc_wait1	mmc2_clk	pr1_mii1_crs	pr1_mdio_mdclk	mcasp0_fsr	*gpio2_1	
19	U10	GPMC_AD8		0x820	gpmc_ad8	lcd_data23	mmc1_dat0	mmc2_dat4	ehrpwm2A	pr1_mii_mt0_clk		*gpio0_22	
20	V9	GPMC_CSn2		0x884	gpmc_csn2	gpmc_be1n	mmc1_cmd	pr1_edio_data_in7	pr1_edio_data_out7	pr1_pru1_pru_r30_13	pr1_pru1_pru_r31_13	*gpio1_31	emmc
21	U9	GPMC_CSn1		0x880	gpmc_csn1	gpmc_clk	mmc1_clk	pr1_edio_data_in6	pr1_edio_data_out6	pr1_pru1_pru_r30_12	pr1_pru1_pru_r31_12	*gpio1_30	emmc
22	V8	GPMC_AD5		0x814	gpmc_ad5	mmc1_dat5						*gpio1_5	emmc
23	U8	GPMC_AD4		0x810	gpmc_ad4	mmc1_dat4						*gpio1_4	emmc
24	V7	GPMC_AD1		0x804	gpmc_ad1	mmc1_dat1						*gpio1_1	emmc
25	U7	GPMC_AD0		0x800	gpmc_ad0	mmc1_dat0						*gpio1_0	emmc
26	V6	GPMC_CSn0		0x87C	gpmc_csn0							*gpio1_29	
27	U5	LCD_VSYNC		0x8E0	lcd_vsync	gpmc_a8	gpmc_a1	pr1_edio_data_in2	pr1_edio_data_out2	pr1_pru1_pru_r30_8	pr1_pru1_pru_r31_8	*gpio2_22	hdmi
28	V5	LCD_PCLK		0x8E8	lcd_pclk	gpmc_a10	pr1_mii0_crs	pr1_edio_data_in4	pr1_edio_data_out4	pr1_pru1_pru_r30_10	pr1_pru1_pru_r31_10	*gpio2_24	hdmi
29	R5	LCD_HSYNC		0x8E4	lcd_hsync	gpmc_a9	gpmc_a2	pr1_edio_data_in3	pr1_edio_data_out3	pr1_pru1_pru_r30_9	pr1_pru1_pru_r31_9	*gpio2_23	hdmi
30	R6	LCD_AC_BIAS_EN		0x8EC	lcd_ac_bias_en	gpmc_a11	pr1_mii1_crs	pr1_edio_data_in5	pr1_edio_data_out5	pr1_pru1_pru_r30_11	pr1_pru1_pru_r31_11	*gpio2_25	hdmi
31	V4	LCD_DATA14		0x8D8	lcd_data14	gpmc_a18	eQEP1_index	mcasp0_axr1	uart5_rxd	pr1_mii_mr0_clk	uart5_ctsn	*gpio0_10	hdmi
32	T5	LCD_DATA15		0x8DC	lcd_data15	gpmc_a19	eQEP1_strobe	mcasp0_ahclkx	mcasp0_axr3	pr1_mii0_rxdv	uart5_rtsn	*gpio0_11	hdmi
33	V3	LCD_DATA13		0x8D4	lcd_data13	gpmc_a17	eQEP1B_in	mcasp0_fsr	mcasp0_axr3	pr1_mii0_rxer	uart4_rtsn	*gpio0_9	hdmi
34	U4	LCD_DATA11		0x8CC	lcd_data11	gpmc_a15	ehrpwm1B	mcasp0_ahclkr	mcasp0_axr2	pr1_mii0_rxd0	uart3_rtsn	*gpio2_17	hdmi
35	V2	LCD_DATA12		0x8D0	lcd_data12	gpmc_a16	eQEP1A_in	mcasp0_aclkr	mcasp0_axr2	pr1_mii0_rxlink	uart4_ctsn	*gpio0_8	hdmi
36	U3	LCD_DATA10		0x8C8	lcd_data10	gpmc_a14	ehrpwm1A	mcasp0_axr0		pr1_mii0_rxd1	uart3_ctsn	*gpio2_16	hdmi
37	U1	LCD_DATA8		0x8C0	lcd_data8	gpmc_a12	ehrpwm1_tripzone_input	mcasp0_aclkx	uart5_txd	pr1_mii0_rxd3	uart2_ctsn	*gpio2_14	hdmi
38	U2	LCD_DATA9		0x8C4	lcd_data9	gpmc_a13	ehrpwm0_synco	mcasp0_fsx	uart5_rxd	pr1_mii0_rxd2	uart2_rtsn	*gpio2_15	hdmi
39	T3	LCD_DATA6		0x8B8	lcd_data6	gpmc_a6	pr1_edio_data_in6	eQEP2_index	pr1_edio_data_out6	pr1_pru1_pru_r30_6	pr1_pru1_pru_r31_6	*gpio2_12	hdmi
40	T4	LCD_DATA7		0x8BC	lcd_data7	gpmc_a7	pr1_edio_data_in7	eQEP2_strobe	pr1_edio_data_out7	pr1_pru1_pru_r30_7	pr1_pru1_pru_r31_7	*gpio2_13	hdmi
41	T1	LCD_DATA4		0x8B0	lcd_data4	gpmc_a4	pr1_mii0_txd1	eQEP2A_in		pr1_pru1_pru_r30_4	pr1_pru1_pru_r31_4	*gpio2_10	hdmi
42	T2	LCD_DATA5		0x8B4	lcd_data5	gpmc_a5	pr1_mii0_txd0	eQEP2B_in		pr1_pru1_pru_r30_5	pr1_pru1_pru_r31_5	*gpio2_11	hdmi
43	R3	LCD_DATA2		0x8A8	lcd_data2	gpmc_a2	pr1_mii0_txd3	ehrpwm2_tripzone_input		pr1_pru1_pru_r30_2	pr1_pru1_pru_r31_2	*gpio2_8	hdmi
44	R4	LCD_DATA3		0x8AC	lcd_data3	gpmc_a3	pr1_mii0_txd2	ehrpwm0_synco		pr1_pru1_pru_r30_3	pr1_pru1_pru_r31_3	*gpio2_9	hdmi
45	R1	LCD_DATA0		0x8A0	lcd_data0	gpmc_a0	pr1_mii_mt0_clk	ehrpwm2A		pr1_pru1_pru_r30_0	pr1_pru1_pru_r31_0	*gpio2_6	hdmi
46	R2	LCD_DATA1		0x8A4	lcd_data1	gpmc_a1	pr1_mii0_txen	ehrpwm2B		pr1_pru1_pru_r30_1	pr1_pru1_pru_r31_1	*gpio2_7	hdmi

BeagleBone Black expansion header P9

Pin	CPU Pin	Pin Name		Pinmux register offset	mode 0	mode 1	mode 2	mode 3	mode 4	mode 5	mode 6	mode 7	
1	GND												
2	GND												
3	3.3V												
4	3.3V												
5	VDD_5V												
6	VDD_5V												
7	SYS_5V												
8	SYS_5V												
9	PWR_BUT												
10	A10	WARMRSTn		0x9B8	*nRESETIN_OUT								
11	T17	GPMC_WAIT0		0x870	gpmc_wait0	gmii2_crs	gpmc_csn4	rmii2_crs_dv	mmc1_sdcd	pr1_mii1_col	uart4_rxd	*gpio0_30	
12	U18	GPMC_BEn1		0x878	gpmc_be1n	gmii2_col	gpmc_csn6	mmc2_dat3	gpmc_dir	pr1_mii1_rxlink	mcasp0_aclkr	*gpio1_28	
13	U17	GPMC_WPn		0x874	gpmc_wpn	gmii2_rxerr	gpmc_csn5	rmii2_rxerr	mmc2_sdcd	pr1_mii1_txen	uart4_txd	*gpio0_31	
14	U14	GPMC_A2		0x848	gpmc_a2	gmii2_txd3	rgmii2_td3	mmc2_dat1	gpmc_a18	pr1_mii1_txd2	ehrpwm1A	*gpio1_18	
15	R13	GPMC_A0		0x840	gpmc_a0	gmii2_txen	rgmii2_tctl	rmii2_txen	gpmc_a16	pr1_mii_mt1_clk	ehrpwm1_tripzone_input	*gpio1_16	
16	T14	GPMC_A3		0x84C	gpmc_a3	gmii2_txd2	rgmii2_td2	mmc2_dat2	gpmc_a19	pr1_mii1_txd1	ehrpwm1B	*gpio1_19	
17	A16	SPI0_CS0		0x95C	spi0_cs0	mmc2_sdwp	I2C1_SCL	ehrpwm0_synci	pr1_uart0_txd	pr1_edio_data_in1	pr1_edio_data_out1	*gpio0_5	
18	B16	SPI0_D1		0x958	spi0_d1	mmc1_sdwp	I2C1_SDA	ehrpwm0_tripzone_input	pr1_uart0_rxd	pr1_edio_data_in0	pr1_edio_data_out0	*gpio0_4	
19	D17	UART1_RTSn		0x97C	uart1_rtsn	timer5	dcan0_rx	I2C2_SCL	spi1_cs1	pr1_uart0_rts_n	pr1_edc_latch1_in	*gpio0_13	
20	D18	UART1_CTSn		0x978	uart1_ctsn	timer6	dcan0_tx	I2C2_SDA	spi1_cs0	pr1_uart0_cts_n	pr1_edc_latch0_in	*gpio0_12	
21	B17	SPI0_D0		0x954	spi0_d0	uart2_txd	I2C2_SCL	ehrpwm0B	pr1_uart0_rts_n	pr1_edio_latch_in	EMU3	*gpio0_3	
22	A17	SPI0_SCLK		0x950	spi0_sclk	uart2_rxd	I2C2_SDA	ehrpwm0A	pr1_uart0_cts_n	pr1_edio_sof	EMU2	*gpio0_2	
23	V14	GPMC_A1		0x844	gpmc_a1	gmii2_rxdv	rgmii2_rctl	mmc2_dat0	gpmc_a17	pr1_mii1_txd3	ehrpwm0_synco	*gpio1_17	
24	D15	UART1_TXD		0x984	uart1_txd	mmc2_sdwp	dcan1_rx	I2C1_SCL		pr1_uart0_txd	pr1_pru0_pru_r31_16	*gpio0_15	
25	A14	MCASP0_AHCLKX		0x9AC	mcasp0_ahclkx	eQEP0_strobe	mcasp0_axr3	mcasp1_axr1	EMU4	pr1_pru0_pru_r30_7	pr1_pru0_pru_r31_7	*gpio3_21	
26	D16	UART1_RXD		0x980	uart1_rxd	mmc1_sdwp	dcan1_tx	I2C1_SDA		pr1_uart0_rxd	pr1_pru1_pru_r31_16	*gpio0_14	
27	C13	MCASP0_FSR		0x9A4	mcasp0_fsr	eQEP0B_in	mcasp0_axr3	mcasp1_fsx	EMU2	pr1_pru0_pru_r30_5	pr1_pru0_pru_r31_5	*gpio3_19	
28	C12	MCASP0_AHCLKR	100	0x99C	mcasp0_ahclkr	ehrpwm0_synci	mcasp0_axr2	spi1_cs0	eCAP2_in_PWM2_out	pr1_pru0_pru_r30_3	pr1_pru0_pru_r31_3	*gpio3_17	HDMI
29	B13	MCASP0_FSX		0x994	mcasp0_fsx	ehrpwm0B		spi1_d0	mmc1_sdcd	pr1_pru0_pru_r30_1	pr1_pru0_pru_r31_1	*gpio3_15	
30	D12	MCASP0_AXR0		0x998	mcasp0_axr0	ehrpwm0_tripzone_input		spi1_d1	mmc2_sdcd	pr1_pru0_pru_r30_2	pr1_pru0_pru_r31_2	*gpio3_16	
31	A13	MCASP0_ACLKX		0x990	mcasp0_aclkx	ehrpwm0A		spi1_sclk	mmc0_sdcd	pr1_pru0_pru_r30_0	pr1_pru0_pru_r31_0	*gpio3_14	
32	VADC												
33	C8	AIN4			*AIN4								
34	AGND												
35	A8	AIN6			*AIN6								
36	B8	AIN5			*AIN5								
37	B7	AIN2			*AIN2								
38	A7	AIN3			*AIN3								
39	B6	AIN0			*AIN0								
40	C7	AIN1			*AIN1								
41	D14	XDMA_EVENT_INTR1		0x9B4	xdma_event_intr1		tclkin	clkout2	timer7	pr1_pru0_pru_r31_16	EMU3	*gpio0_20	
41,1	D13	MCASP0_AXR1		0x9A8	mcasp0_axr1	eQEP0_index		mcasp1_axr0	EMU3	pr1_pru0_pru_r30_6	pr1_pru0_pru_r31_6	*gpio3_20	
42	C18	ECAP0_IN_PWM0_OUT		0x964	eCAP0_in_PWM0_out	uart3_txd	spi1_cs1	pr1_ecap0_ecap_capin_apwm_o	spi1_sclk	mmc0_sdwp	xdma_event_intr2	*gpio0_7	
42,1	B12	MCASP0_ACLKR		0x9A0	mcasp0_aclkr	eQEP0A_in	mcasp0_axr2	mcasp1_aclkx	mmc0_sdwp	pr1_pru0_pru_r30_4	pr1_pru0_pru_r31_4	*gpio3_18	
43	GND												
44	GND												
45	GND												
46	GND												