Sebastian Lerner (sl7ey)

Assignment 3

Section 105

Due: February 27, 2015

***Problem Statement:***

The problem posed in the lab was to design a simple finite state machine to generate a specific output sequence.

***Solution:***

In order to solve this problem, I first created the 4-1 MUX using only AND, OR, and inverter gates. Once this was completed, the next step was to convert this to using only NAND gates, and I did this with Boolean algebra. Once I created the circuit in Logisim with solely NANDS, I went to lab and built the actual circuit. In order to test it, I used the most efficient method, which only involved testing eight inputs rather than every possible option. The last portion of the lab was to do the second part, which involved creating a 4 bit 4-1 MUX that had 18 inputs. Additionally, I created a 16-1 circuit in Logisim. IN order to figure out how to do this, I thought about how to scale from a 4-1 to a 16-1 and how the pieces were similar.

***Problems Encountered:***

I had some issues with the in-lab portion. A better way to approach it would have been to build a small piece, and test it, then continue once it worked. Rather, I built the whole thing and then proceeded to test it, and only half of it worked. At that point, it was tough to debug, however, I managed to get most of it working eventually.

***Conclusions:***

In conclusion, the lab provided an interesting situation to create an actual MUX, and it is pretty easy to see how this could be an important tool when it comes to electronics. The lab was very straightforward, however, I still learned a great amount.