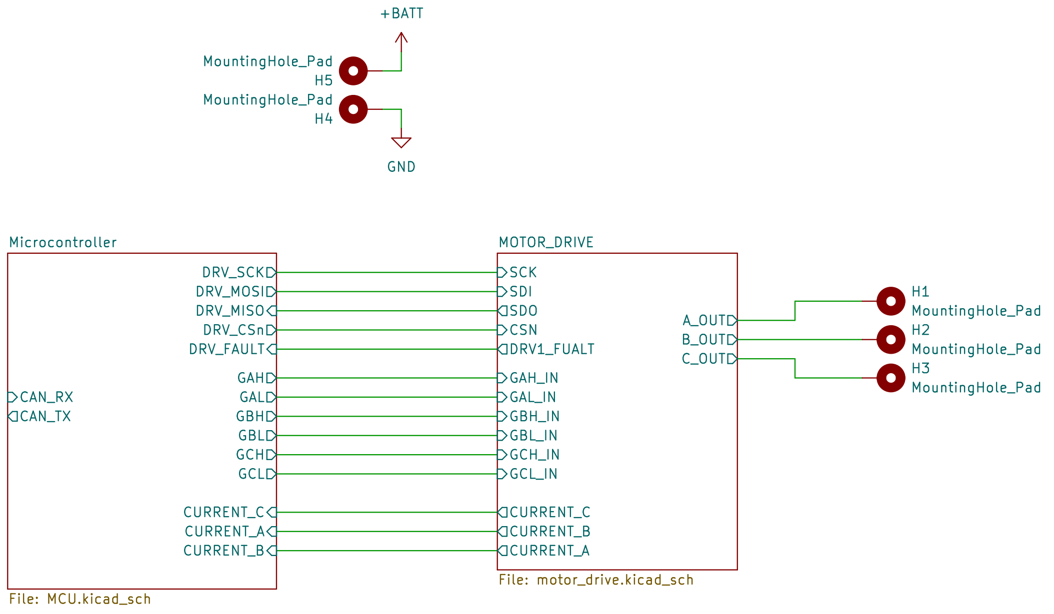

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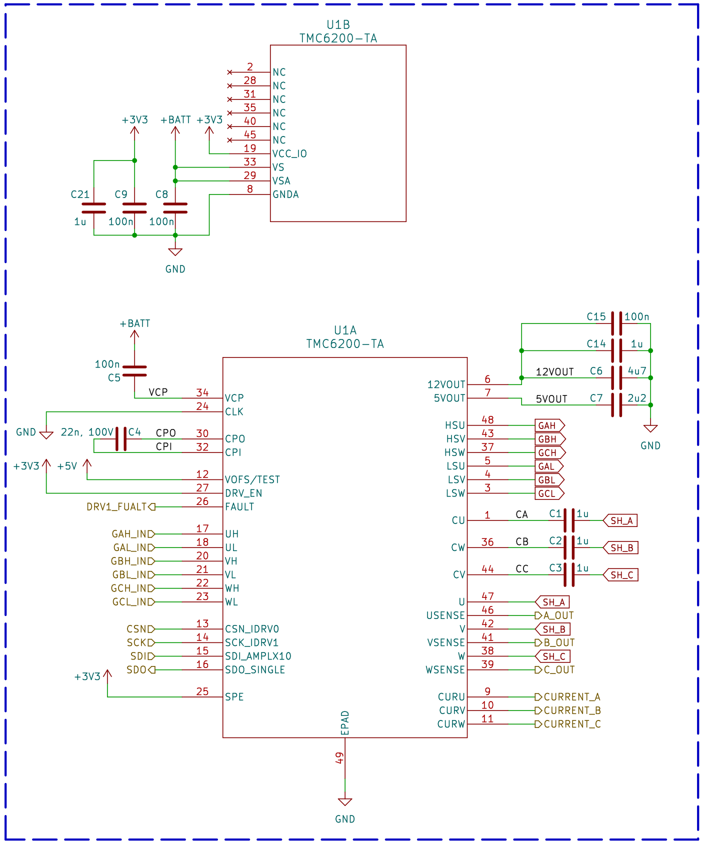
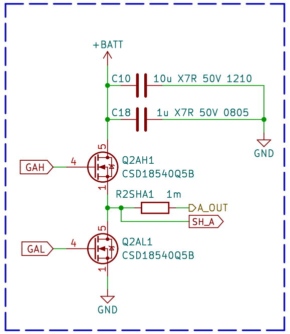
THREE PHASE BLDC DRIVER



PHASE A HALF-BRIDGE



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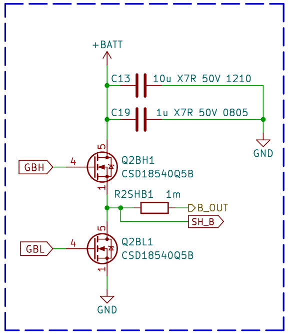

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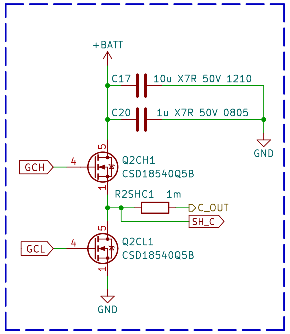

CURRENT SENSE RESISTORS

-> P_SENSE = I^2 * R = 50^2 * 1 / 1000 = 2.5 W
-> V_SENSE = IR = +- 50 * 1 / 1000 = +- 50 mV

Therefore with the TMC6200-TA's 5 V/V gain setting:
-> V_SENSE_OUT = +- 50 mV * 5 V/V = +- 0.25 V

With V_REF = 1.65 V, we get V_OUT in the range [1.4 V, 1.9 V]

The STM32's internal OPAMP gain can the be programmed with a gain of 4 to get [0.65, 2.65]. It is done this way to supporta wider range of currents.

For example if your motor's max current is 10A, we get 50mV drop across R_SH, to give an initial range of +- 0.05V (ideal range would be +- 1.6V) and we can use an internal opamp gain of 32 to get +- 1.6V.

Note gain options: 1, 2, 4, 8, 16, 32, 64.
This means that sensing can be optimised for currents between 1A and 100A

CSD18543Q3A MOSFET INFO:

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	60		V
Q_g	Gate Charge Total (10 V)	41		nC
Q_{gd}	Gate Charge Gate-to-Drain	6.7		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 4.5 V	2.6	mΩ
		V_{GS} = 10 V	1.8	
$V_{GS(th)}$	Threshold Voltage	1.9		V

Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package Limited)	100	A
	Continuous Drain Current (Silicon Limited), T_C = 25°C	205	
	Continuous Drain Current[(1)]	29	
I_{DM}	Pulsed Drain Current, T_A = 25°C[(2)]	400	A
P_D	Power Dissipation[(1)]	3.8	W
	Power Dissipation, T_C = 25°C	188	
T_J, T_{stg}	Operating Junction, Storage Temperature	–55 to 175	°C
E_{AS}	Avalanche Energy, Single Pulse I_D = 80 A, L = 0.1 mH, R_G = 25 Ω	320	mJ

(1) Typical $R_{\theta JA}$ = 40°C/W on a 1-in^2, 2-oz Cu pad on a 0.06-in thick FR4 PCB.
(2) Max $R_{\theta JC}$ = 0.8°C/W, pulse duration ≤ 100 µs, duty cycle ≤ 1%.

MOSFET DECOUPLING

C = (I * dt) / dV
= (50A * 10ns) / 0.2 V = 2.5 uF
I use 10uF + 1uf MLCCs close to each MOSFET for a total of 11uF per MOSFET for some margin

This calculation uses the rise time (dt) and the allowable voltage drop on the decoupling cap (dV) to calculate the required capacitance of the cap

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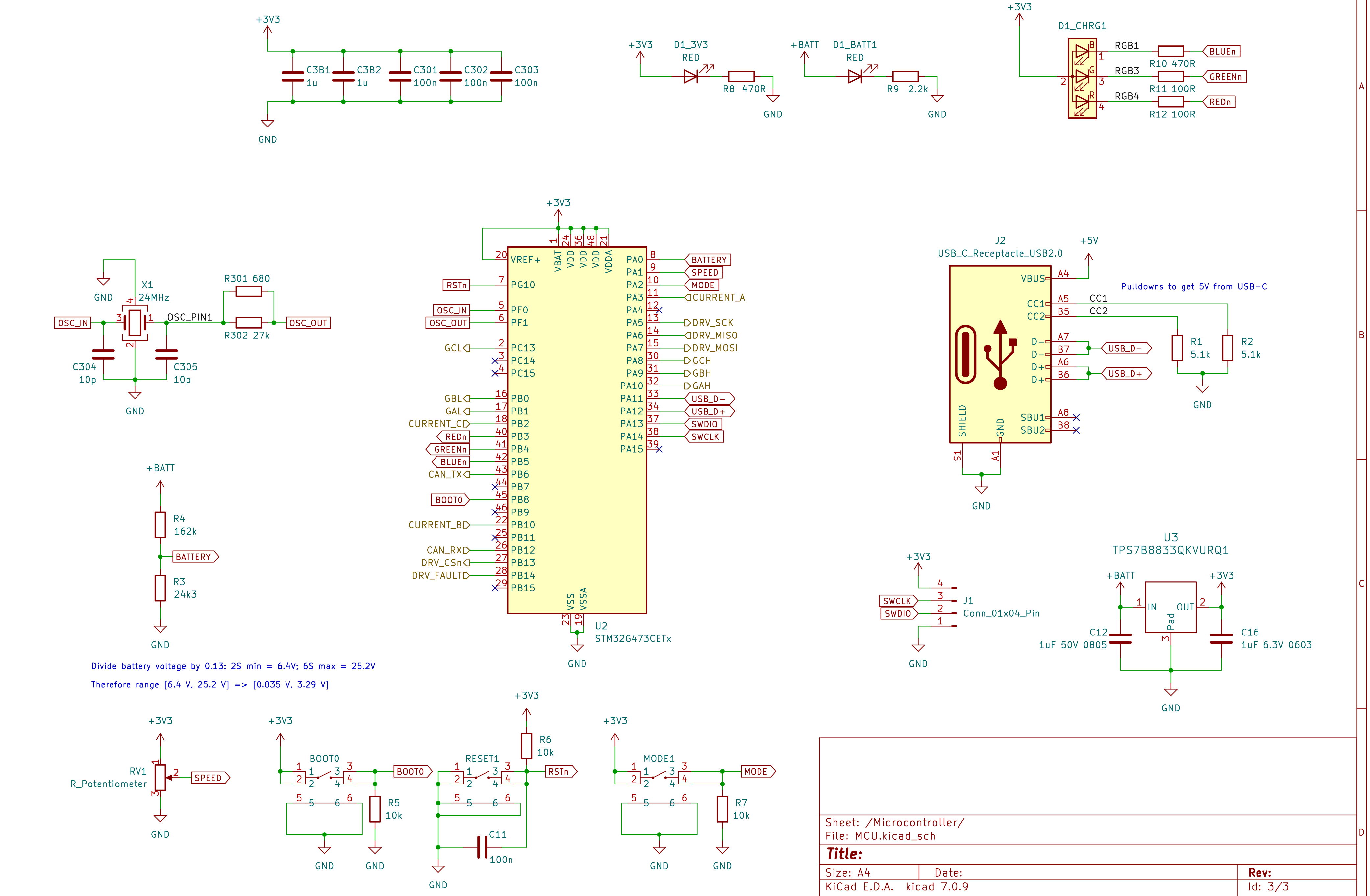

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