

## Instructions for programming the new AVR based voice module

Remove and SD card.

Connect a programmer to the board, set the fuses as detailed below, then program in the file optiboot\_atmega328.hex.

Disconnect the programmer.

Connect a serial interface to the external serial connections, and power the board normally.

Use Avrdude to program the file amod\_last.hex. A batch file write328.bat contains an example Avrdude command line. Check the port value is correct for your system. Power off.

Disconnect the serial interface, replace the SD card, and power up normally.

Updating the application (amod\_last.hex) should now be possible just by connecting the serial interface and writing a new version.

### ATMEGA328P

Boot size 256

Preserve EEPROM

Brown out 2.7V

Ext crystal Osc; Frequency 8.0- MHz; Start-up time PWRDWN/RESET: 16CK/14CK + 65 ms

NO clock divide by 8

NO watchdog

Boot Flash section size=256 words Boot start address=\$3F00

☒ BOOTRST

☐ Reset Disabled (Enable PC6 as i/o pin); [RSTDISBL=0]

☐ Debug Wire enable; [DWEN=0]

☒ X Serial program downloading (SPI) enabled; [SPIEN=0]

☐ Watchdog Timer always on; [WDTON=0]

☒ Preserve EEPROM memory through the Chip Erase cycle; [EESAVE=0]

☐ Brown-out detection level at VCC=2.7V; [BODLEVEL=101]

☐ Divide clock by 8 internally; [CKDIV8=0]

☐ Clock output on PORTBO; [CKOUT=0]

Ext Crystal Osc; Frequency 8.0- MHz; Start-up time PWRDWN/RESET: 16CK/14CK + 65 ms; [CKSEL=1111 SUT=11]

Extended      0xFD

High            0xD6

Low             0xFF

### ATMEGA88

Boot size 256

Preserve EEPROM

Brown out 2.7V

Ext crystal Osc; Frequency 8.0- MHz; Start-up time PWRDWN/RESET: 16CK/14CK + 65 ms

NO clock divide by 8

NO watchdog

Boot Flash section size=256 words Boot start address=\$0F00

☒ BOOTRST

☐ Reset Disabled (Enable PC6 as i/o pin); [RSTDISBL=0]

☐ Debug Wire enable; [DWEN=0]

☒ X Serial program downloading (SPI) enabled; [SPIEN=0]

☐ Watchdog Timer always on; [WDTON=0]

☒ Preserve EEPROM memory through the Chip Erase cycle; [EESAVE=0]

☐ Brown-out detection level at VCC=2.7V; [BODLEVEL=101]

☐ Divide clock by 8 internally; [CKDIV8=0]

☐ Clock output on PORTBO; [CKOUT=0]

Ext Crystal Osc; Frequency 8.0- MHz; Start-up time PWRDWN/RESET: 16CK/14CK + 65 ms; [CKSEL=1111 SUT=11]

Extended	0xFC
High	0xD5
Low	0xFF