Course Description and Outcome Form
Department of Computer Science and Engineering
School of Engineering and Computer Science
BRAC University

A. Course General Information:

Course Code:	CSE 340
Course Title:	Computer Architecture
Credit Hours (Theory + Lab):	3+0
Contact Hours (Theory + Lab):	3+0
Category:	Program Core
Type:	Required, Engineering, Lecture
Prerequisites:	CSE260
Co-requisites:	None

B. Course Catalog Description (Content):

A systematic study of the various elements in computer design, including circuit design, storage mechanisms, addressing schemes, and various approaches to parallelism and distributed logic. Information representation and transfer; instruction and data access methods; the control unit; hardware and microprogrammed; memory organization; RISC and CISC machines.

C. Course Objective:

The objectives of this course are:

a) Introduce different processor technologies, performance metrics, representation of numbers, and arithmetic operations.
b) Introduce MIPS architecture, demonstrate its instruction formats, and translation of simple C/Java code snippets to MIPS assembly language.
c) Teach how to design processor datapaths, recognize pipelining hazards, and use different techniques to overcome them.
d) Introduce and explain memory hierarchy and performance analysis.
e) Introduce parallel architecture and parallel programming.

D. Course Outcomes (COs):

Upon completing this course, students will be able to:

Sl.	CO Description	Weightage (%)
CO1	**Explain** the processor technologies and performance metrics alongside the representation of numbers and arithmetic operations	25
CO2	**Demonstrate** various instruction formats, their encoding, translation from C/Java code to MIPS instruction	25
CO3	**Visualize** the datapath of different instructions and recognize various pipelining hazards and hazard overcoming techniques	20
CO4	**Outline** memory hierarchy and performance analysis and **review** various parallel architecture and its programming	10

E. Mapping of CO-PO-Taxonomy Domain & Level- Delivery-Assessment Tool:

Sl.	CO Description	POs	Bloom's taxonomy domain/level	Delivery methods and activities	Assessment tools
CO1	**Explain** the processor technologies, performance metrics alongside the representation of numbers and arithmetic operations	a	Cognitive	Lectures, slides, notes	Midterm, Final
CO2	**Demonstrate** various instruction formats, their encoding, translation from C/Java code to MIPS instruction	a	Cognitive	Lectures, slides, notes	Midterm, Final
CO3	**Visualize** the datapath of different instructions and **recognize** various pipelining hazards and hazard overcoming techniques	b	Cognitive	Lectures, slides, notes	Midterm, Final
CO4	**Outline** memory hierarchy and performance analysis and **review** various parallel architecture and its programming	a	Cognitive	Lectures, slides, notes	Midterm, Final

F. Course Materials:

i. Text and Reference Books:

Sl.	Title	Author(s)	Publication Year	Edition	Publisher	ISBN
1	Computer Organization and Design: The Hardware/Software Interface	D. A. Patterson, J. L. Hennessy	2013	5th Edition	Morgan Kaufmann	978-0124077263
2	Computer Architecture: A Quantitative Approach	D. A. Patterson, J. L. Hennessy	2017	6th Edition	Morgan Kaufmann	978-0128119051
3	Computer Architecture and Organization	J. P. Hayes	1997	3rd Edition	McGraw Hill	0-07-027366-9

ii. Other materials (if any)

Lecture Notes, Slides, Practice Sheets

G. Lesson Plan:

No	Topic	Week/Lecture#	Related CO (if any)
1	Various Computer Architecture Models, Measuring Performance CPI, Performance Equation, RISC and CISC Architecture	1,2	CO1
2	Introduction of the Computer Architecture, Introduction to MIPS Assembly Language, Instruction sets, Conversion from High-level code to MIPS equivalent form, how function call works, etc.	2, 3, 4, 5, 6	CO2
3	Arithmetic for Computers: Addition, Subtraction, Multiplication, Division, IEEE-754 floating-point conversion, floating-point operations in MIPS architecture	6, 7	CO1
Midterm			
4	MIPS non-pipelined datapath/control path, how single-cycle datapath works for various instruction, advantages, disadvantages of single-cycle datapath	8	CO3
4	MIPS pipelined datapath, how it works, advantages and disadvantages, designing pipelined datapath, Hazard and hazard overcoming techniques	9	CO3
5	Memory Hierarchy, Memory Technology, Cache Introduction and Improving Cache Performance, Virtual memory, Cache Miss	10, 11	CO4
6	Introduction of Parallel Processors, SISD, MIMD, SIMD, SPMD, and Vector, Multicore, multi-threading, GPU	12, 13	CO4
Final			

H. Assessment Tools:

Assessment Tools	Weightage (%)
1. Participation in class	5
2. Quizzes/Class Tests	15
3. Assignments	15
4. Mid Term Examination	25
5. Final Examination	40
Total	100%

I. CO Assessment Plan:

Assessment Tools	Course Outcomes			
	CO1	CO2	CO3	CO4
1. Quizzes/Class Tests				
2. Mid-Term Examination	√	√		
3. Assignments				
4. Final Exam	√	√	√	√

J. CO Attainment Policy:

As per Department of CSE Course Outcome Attainment Policy

K. Grading policy:

As per BRAC University grading policy

L. Course Coordinator:

Nabuat Zaman Nahim (NZN)