CSE340: Computer Architecture

Assignment 2

Chapter 2 - Instructions: Language of the Computer (MIPS Instructions)

Total Marks: 20 (Marks are indicated in third brackets after each question)

1. What is the difference between Program Counter and $zero? In the case of 16-bit and 128-bit architecture, what would be the increment in memory address for sequential instruction execution? [2]

2. Let us consider the instruction lw $4, X($5). Now, we have an array A and the base address of that array is 256 in decimal. If we are looking to load the contents of A[5], find the value of X in the lw instruction in the case of 256-bit architecture. [1]

3. Assume that the base address of the array *A* is in *$s0*, and the values of *i* and *f* are stored in *$s1* and *$s2*. Then translate the following statement into MIPS assembly code. [2]

   f = A[i]

4. Let us consider the set of instructions given below. Here, X and Y are in registers $s0 and $s1 respectively. The base address of the array Arr is in $s4. Now, write the equivalent MIPS code for the given set of instructions, identify the instruction type, and write the machine code for each instruction. [5]

   X = 15Y - 5;
   Arr[5] = 2X + Arr[10];

5. Calculate the branch destination address of the instruction beq $9, $8, 124 if the PC holds 0x1278A4B1. Show all the steps and write the calculated branch address in hex. [3]

6. What is the jump address of the instruction j 1590 if the PC holds 0x00AB1203? Show the steps in your calculations and write the final address in hex. [2]

7. Consider the instruction: lw $8, 52($17). If the base address is 0x15632017. What is the **memory address** of the data that will be loaded to $8? [1]

8. Given the following code sequence:

```
for (i = 0; i<10; i++) {
    if (A[i] ! = 5)
        A[B[i]] += 1
    else
        A[i] =  B[i+1] }
```

If the base address of arrays A and B are in $s1 and $s2 respectively and i, 5, and 1 are in $s3, $s4, $s5. write the equivalent MIPS code. [4]