SET A

Department of Computer Science and Engineering
FINAL EXAMINATION
Fall 2023
CSE 340 / EEE410: Computer Architecture

Total Marks: 40 ***Time Allowed: 2 Hours***

- **Answer ALL the questions. Numbers in the right margin indicate marks for each question. Understanding the question is part of the exam.**
- **Please complete your answer within 2 hours. You'll have extra 10 minutes to upload your answer. Please note that only .pdf file is allowed**

Note- Please mention your student ID, full name, CSE340 section number and SET Number on top of your answer script.

1. CO1
   a. Multiply 3.021 and 0.71 using IEEE 754 single precision floating point representation. Also, **show** the status of the result (overflow or underflow). Consider 7 decimal digits when you are converting from decimal to binary. You should show the decimal equivalent of your final output. **3**
   b. **Convert** -91.312 into IEEE 754 floating point representation. Consider you have a register that is 21-bit in length and in the register, one bit is reserved for the sign of the number, the following five bits are for the exponent, and the rest for the fraction part. Show the equivalent Hex representation of your conversion. **3**
   c. Consider $X=7CAC2000_{Hex}$ and $Y=28CDC000_{Hex}$, and **perform** X+Y using IEEE 754 single precision floating point representation. You should also show the decimal equivalent of your final result. **3**
   d. **Justify** your answer briefly: **2*1.5**
      i. Why Pseudo instructions don't fall under the available MIPS instruction types?
      ii. PC is part of the register file and it can be used to store data, true or false?
2. CO2
   a. **Show** the examples of each addressing scheme with name available in MIPS. **2**
   b. **Write** the MIPS instructions for the following code snippets. Suppose the base of arrays A and F are in $s0 and $s4 respectively and i and n are stored in $s1, $s2. Please remember that you cannot use the multiplication instruction and your MIPS code should be optimized. **2*2.5**

      i.
      ```
      if (A[2] == A[F(7)])
                  F[5] = 9*A[3] - 18*A[2] - 10;
      ```

      ii.
      ```
      for (i = 0; i < n; i++)
                  A[i] = 14*A[A[i]];
      ```

c. If PC = 0x44000040 **calculate** the branch target address for the instruction **2*2**

i. bne $5, $6, 512

ii. JAL 512

Your answer should show the detailed calculations along with the diagrams.

3. CO3 a. If memory operation takes 60 ps, register operation takes 30 ps and combinational logic stage takes 50 ps, then **calculate** the time required to complete a lw and a sw instructions in a single cycle Datapath and in a pipeline implementation. Please note that you have to calculate the timing for individual instructions. **3**

b. **Design** a single cycle datapath for the below instruction. Your design should have all the labeling. **3**

Bne $10, $11, 1004

c. i. **Explain** the double data hazard scenario with example. Also, **write** double data hazard overcoming logic. **2*2**

ii. **Explain** in a memory operation instruction how pipeline system identifies whether it's a memory read or memory write operation. Your answer should have justification with necessary logics.

d. Consider the code sequence given below and answer the following questions. For time calculation please use the data provided in question 3(a). **2+1+4**

```
 i.   lw $10, 40($11)
 ii.  add $5, $10, $7
 iii. sub $3, $7, $4
 iv.  sll $5, $5, 3
 v.   lw $13, 48($5)
 vi.  lw $13, 32($13)
```

i. **Calculate** the total time and average CPI required for the above code sequence in case of an ideal pipeline (no hazard). You should have a supporting diagram along with your calculation.

ii. How many data hazards are there in the given code sequence?

iii. Apply only *stall* to overcome the data hazards. **Calculate** the total time (in ps) and average CPI required after applying the method. Your answer should contain the necessary diagram.