

BRAC UNIVERSITY
Department of Computer Science and Engineering

Examination: Final
Duration: 2 hours

Semester: Fall 2023
Full Marks: 40

CSE 340: Computer Architecture

- Answer ALL the questions. Numbers in the right margin indicate marks for each question. Understanding the question is part of the exam.
- Please mention your student ID, full name, and CSE340 section number on top of your answer script. Please remember that it is a proctored exam so faculty members are monitoring your activity during the exam. If the faculty members detect any suspicious activity, your exam can be canceled. At the end of the exam, you will be given 15 more minutes to scan and upload your answer script using the given Google Form link.

1. CO2 a) Consider the below code sequence. **Convert** this code to an equivalent MIPS assembly code. Assume that variables X and Z are in register \$s0 and \$s1 respectively and the base address of A and B are in register \$t5 and \$t6 respectively. Y is in register \$f0. Here Array A and B are float arrays. 4

```
(int) X = (float) Y + (int) 7*Z;  
(float) Y = (int) X + A[4] - 77;  
B[8] = (float) Y
```

- b) **Translate** the MIPS Assembly instruction `andi $8, $16, -8` to its corresponding 32-bit binary machine code. You may assume that the opcode for `andi` instruction is $(9)_{10}$. 2

- c) **Write** the MIPS instructions for the following code snippets. Suppose the base address of C is in \$s4 and i is in \$t0. 5

```
if (C[i] % 3 == 0) {  
    C[i] = 7;  
else {  
    C[i+1] = C[i] * 7;  
}
```

- 2. CO3** a) **Write** down the binary representation of the floating-point decimal number $(-286.4892)_{10}$ in the IEEE-754 40-bit format, with a 6-bit exponent field. You have to take 10 bits after the binary point during the decimal-to-binary conversion. **4**
- b) **Calculate** the addition of the two binary floating-point numbers represented in the IEEE-754 standard single-precision format. The two numbers are $(5E815010)_{16}$ and $(BC061102)_{16}$ in hexadecimal format. You must show all the steps involved in the calculation. **6**
- 3. CO4** a) Consider the instructions: addi (add immediate), beq (branch if equal), sub (subtract). **Explain** the operation performed at the decode and execution stage of the Datapath for each of these instructions. **3**
- b) **Draw** the datapath for the following instruction. Make sure that all the data and control links are properly labeled. You must mention the control bits and the select bits for the MUX. **5**
- addi \$7, \$16, -11
- c) Write the MIPS code for storing \$s3 and \$s4 in stack. **3**
- d) Consider the code sequence given below and answer the following questions **8**
1. lw \$10, 40(\$11)
 2. add \$5, \$12, \$7
 3. sub \$3, \$7, \$4
 4. sll \$5, \$1, 3
 5. srl \$7, \$7, 8
- i) How many clock cycles are required for the above code sequence in case of single cycle datapath and for pipelining?
- ii) **Calculate** the CPI for both cases.
- iii) Consider, the following durations for each stage
 IF = 500ns
 ID = 150ns
 EX = 300ns
 MEM = 200ns
 WB = 200ns
Calculate the clock periods and the total amount of time taken to complete the 4 instructions in both single cycle datapath and pipelining.

“It is possible to commit no mistakes and still lose. That is not a weakness. That is life.”