Assignment 03

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Section: 09

Course: CSE 340

Answer to the question no 1

Given that,

add	20%
addi	20%
not	0%
beq	25%
lw	25%
sw	10%

Among the given instructions only lw and sw will be used for data memory.

∴ Therefore, in (25 + 10)% = 35% fraction of all cycles is the datee memory used.

Answer to the question no 2

Among the given instructions only addi, beq, lw and sw instructions will use the sign extender circuit.

∴ Therefore, addi + beq + lw + sw

= 20% + 25% + 25% + 10%

= 80%.

∴ Therefore, in 80% fraction of all cycles of input of the sign-extender circuit needed.

Answer to the question no 3

Given MIPS instructions are as follows:

lw $t0, 36 ($t1) ——— instruction (i)

lw $t2, 40 ($t0) ——— instruction (ii)

lw $t3, 44 ($t2) ——— instruction (iii)

sll $t3, $t2, 2. ——— instruction (iv)

sub $t0, $t3, $t2. ——— instruction (v)

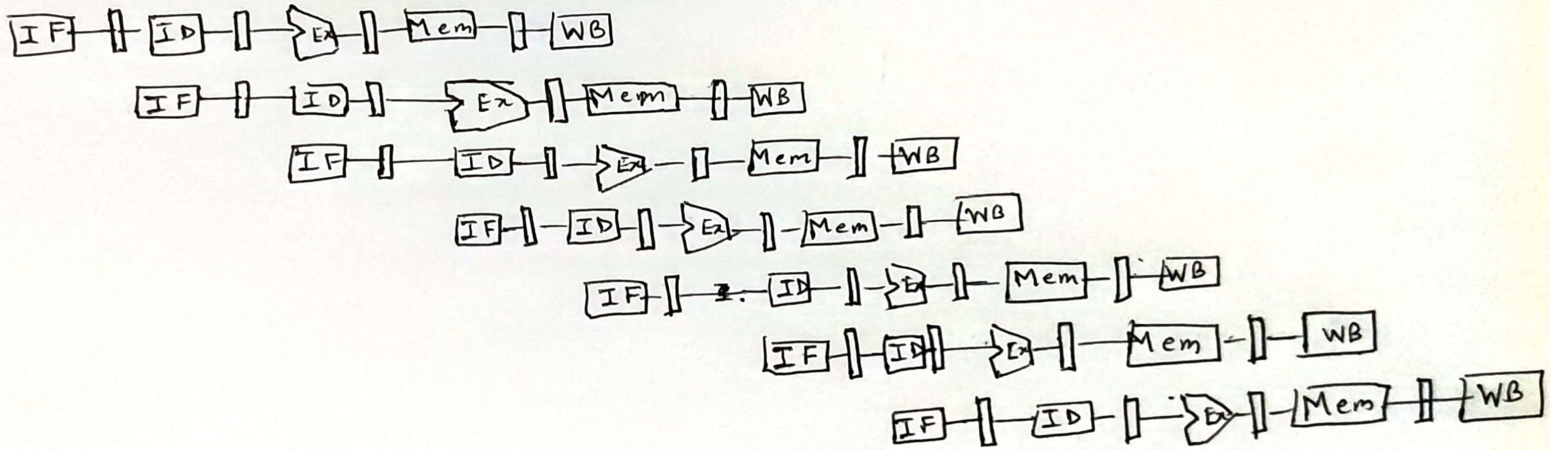
addi $t0, $t0, 2. ——— instruction (vi)

srl $t0, $t3, 2 ——— instruction (vii)

Answer to the question no 3

For the given code sequence datapath using pipeline stages would look like.

```
lw   $t0, 36($t1)
lw   $t2, 40($t0)
lw   $t3, 44($t2)
sll  $t3, $t3, 2
sub  $t0, $t3, $t2
addi $t0, $t0, 2
srl  $t0, $t3, 2.
```



lw $t0, 36 ($t1)

lw $t2, 40 ($t0)

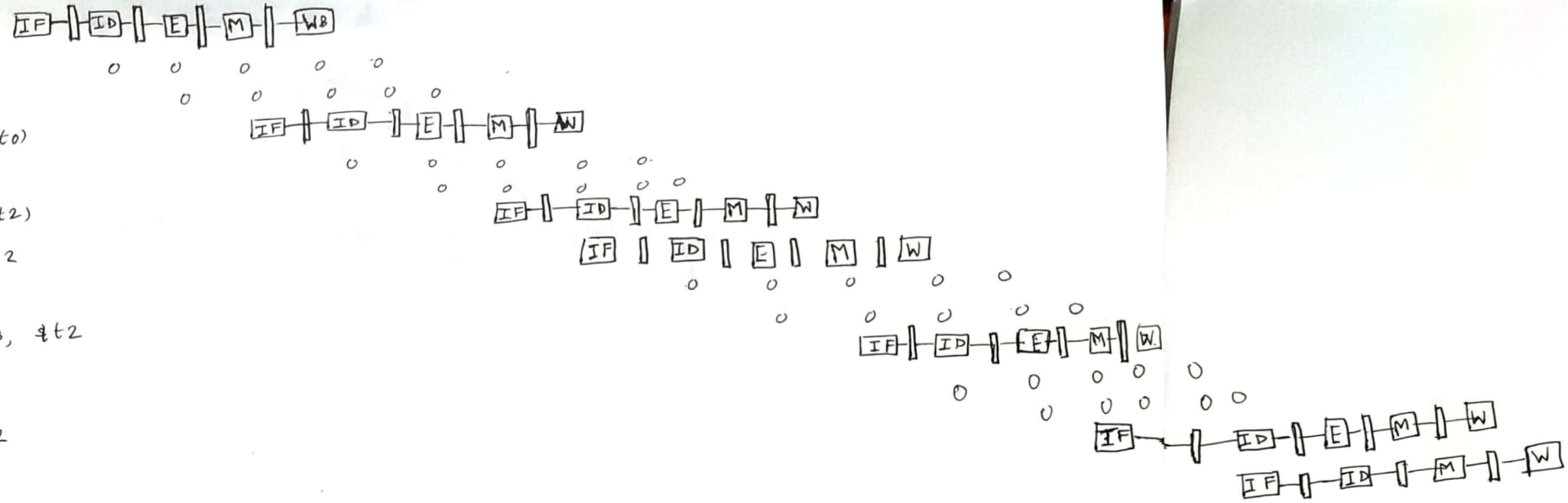
lw $t3, 44 ($t2)

sll $t3, $t2, 2

sub $t0, $t3, $t2

addi $t0, $t0, 2

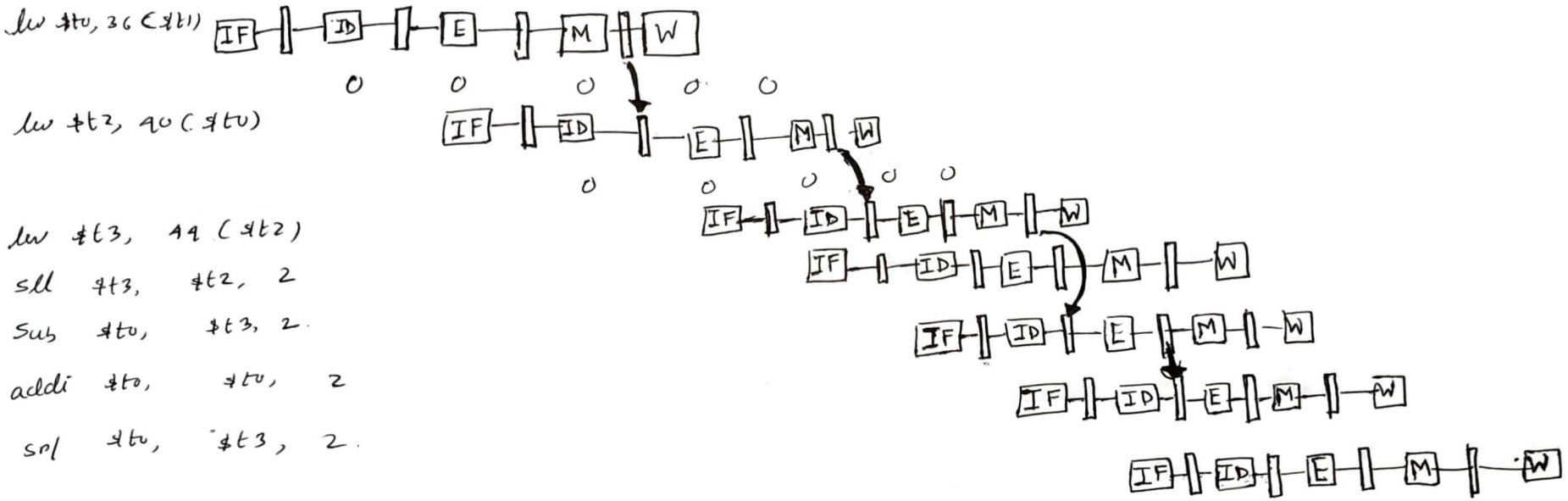
srl $t0, $t3, 2



∴ Updated Clock Cycle = 19

∴ Updated CPI = 19/7 = 2.714

Answer to the question no 4



Updated Clock Cycle = 13

∴ Updated CPI = 13/7 = 1.857

Answer to the question no 5

There is no code scheduling possible for the given code sequences. As they are directly dependent on each other. Therefore, we can't do code scheduling here. So, the clock cycle and CPI for this question would be the same as the answer of question no 4.

∴ Updated Clock cycle = 13.

∴ Updated CPI = 13/7 = 1.857