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CSE 340

Online Proctored Exam

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Section: 09

Answer to the question no 1

(a)

Let, $X = 2.021$ and $Y = 0.91$

X in Binary

Binary of 2 = 10.

Binary of 0.021 = 000000 10.

$0.021 \times 2 = 0.042$ 0
$0.042 \times 2 = 0.084$ 0
$.084 \times 2 = 0.168$ 0
$.168 \times 2 = 0.336$ 0
$0.336 \times 2 = 0.672$ 0
$0.672 \times 2 = 1.344$ 1
$0.344 \times 2 = 0.688$ 0

∴ X in Binary = 10. 0000010

∴ X in Binary normalized = 1.0000010×2^1

Y in Binary

Binary of Y = 0. 1110100

$0.91 \times 2 = 1.82$ 1
$0.82 \times 2 = 1.64$ 1
$.64 \times 2 = 1.28$ 1
$.28 \times 2 = 0.56$ 0
$.56 \times 2 = 1.12$ 1
$.12 \times 2 = 0.24$ 0
$0.24 \times 2 = 0.480$

∴ Y in Binary normalized form

$= 1.110100 \times 2^{-1}$

Now multiplying X * Y.

∴ $X * Y = (1.0000010 * 1.1101 00) * 2^1 \times 2^{-1}$

$= (1.0000010 * 1.1101 00) * 2^0$

$= 11.1 \quad 0100 \quad 1110 \quad 1000 \times 2^0$

~~X in single~~

Now multiplying X * Y.

$X * Y = (1.00000010 * 1.110100) * 2^{-1} \times 2^{1}$

$= (1.00000010 * 1.110100) \times 2^{0}$

$= (11.1\ 0100\ 1110\ 1000) \times 2^{0}$

$= (1.11\ 0100\ 1110\ 1000) \times 2^{1}$

-05

Decimal, underflow

(b)

Given that,

20 bit register and 5 bit for exponent

∴ fraction part is 14 bits.

-61.312 ∴ Sign bit = 1.

Binary of $61. = 11\ 1101$

Binary of $.312 = .0100\ 11111$

$.312 \times 2 = 0.624$ 0
$.624 \times 2 = 1.248$ 1
$.248 \times 2 = 0.496$ 0
$.496 \times 2 = 0.992$ 0
$.992 \times 2 = 1.984$ 1
$.984 \times 2 = 1.968$
$.968 \times 2 = 1.936$ 1
$.936 \times 2 = 1.872$
$.872 \times 2 = 1.744$

Binary of 61.312 in Normalized form

$= 11\ 1101.\ 0100\ 11111$

$= 1.\ 11101\ 0100\ 11111 \times 2^5$

Here, fraction part = $0.\ 11101\ 0100\ 11111$

Actual exponent = 5.

As there is 5 bit for exponent.

∴ bias $= 2^{5-1} - 1 = 15$.

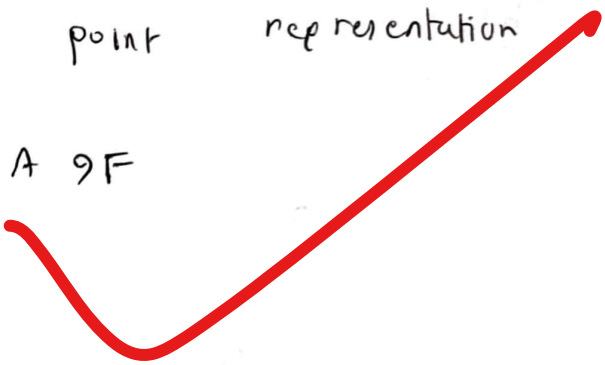
∴ Biased exponent = $15 + 5 = 20$

∴ Floating point representation would be,

1	10100	11101	0100	11111

∴ Floating point representation in hex would be,

= D3A 9F



(c)

$X = 7AAC\,2000$; $Y = 2BCD\,C000$

$\therefore$ X in binary = 0 | 111 1010 1 | 010 1100 0010 0000 0000 0000

0 : sign bit
111 1010 1 : biased exp.
010 1100 0010 0000 0000 0000 : Mantissa.

$\therefore$ Biased exponent = 111 1010 1 = 245.

$\therefore$ Actual exponent = 245 − 127 [$\because$ An bias = 127 bit 8 bit exponent due to bias = 2^{n-1}]

= 118

$\therefore$ X in Binary normalized = $1.010\ 1100\ 0010\ 0000\ 0000\ 0000 \times 2^{118}$

Y in binary = 0 | 010 1011 | 100 1101 1100 0000 0000 0000

$\therefore$ sign bit = 0 ; biased exponent = 010 1011

= 87.

$\therefore$ Actual exponent = 87 − 127

= −40

$\therefore$ Y in binary normalized = $1.100\ 1101\ 1100\ 0000\ 0000\ 0000 \times 2^{-40}$

∴ Now updated y in binary normalized form

$= 0.[157\ 0's]\ 1100\ 1101\ 1100\ 0000\ 0000\ 0000 \times 2^{118}$

∴ X + Y

$= 2^{118}(1.0101\ 1100\ 0010\ 0000\ 0000\ 0000 + 0.[157\ 0's]\ 1100\ 1101\ 1100\ 0000\ 0000\ 0000)$

$=(1.0101\ 1100\ 001[147\ 0's]1111\ 1101\ 1100\ 0000\ 0000\ 0000) \times 2^{118}$

$=(2^0 + 2^{-2} + 2^{-4} + 2^{-5} + 2^{-10} + 2^{-158} + 2^{-159} + 2^{-162} + 2^{-163} + 2^{-165} + 2^{-166} + 2^{-167}) \times 2^{118}$

$= 1.3447265625 \times 2^{118}$

$= 4.4686204849 \times 10^{35}$.

(d)

(i) Pseudo instructions don't fall under the available MIPS instruction type because these instructions are there to give us a basic idea how the original instructions work. One of the pseudo instruction is: mult rd rs, rt. where as original mult instruction is mult rs, rt.

(ii) The given statement is False. As, PC just hold the address of the current instruction that is being executed. Moreover, PC is a register.

Answer to question no 2

(a)

There are ~~6~~ 5 addressing schemes present in MIPS. And these are memory address, branch address and jump address. Example:

x = A[5]

Here A[5] is the memory address of A[5]. Memory address would be (5×4) + base address of A.

Moreover

beq $s1, $s2, L1 this is an example of branch addressing. If L1 value is 2. Then branch address would be, PC+4+ (2*4)

Moreover,

J L2 is an example of jump instructions. and the jump address would be, (PC+4)'s MSB 4 bits concated with (L2*2)

-1

Not a proper answer

(b)

(i)

A → $s0, F → $s4, i → $s1, n → $s2

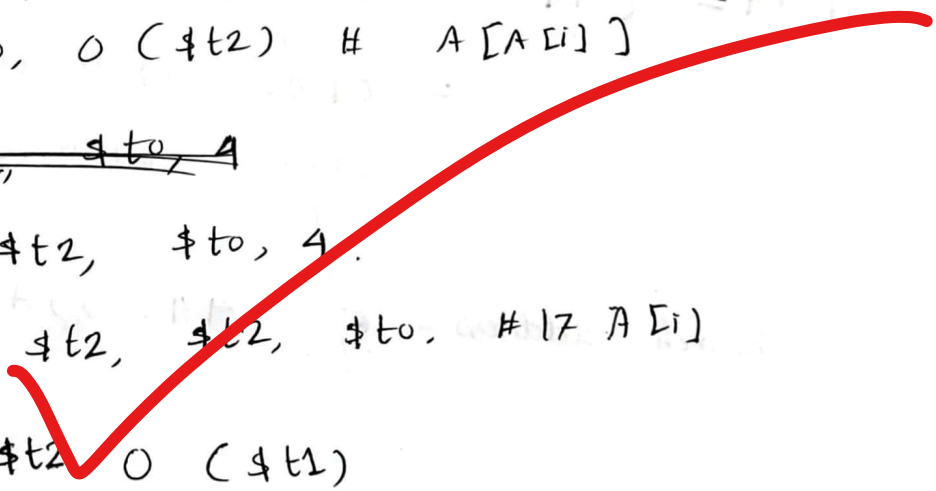
```
lw $t0, 8($s0)    # A[2]
lw $t1, 28($s4)   # F[7]
sll $t1, $t1, 2
add $t1, $t1, $s0
lw $t2, 0($t1)    # A[F[7]]

bne $t0, $t2, Exit
    lw $t1, 12($s0)   # A[3]
    sll $t2, $t1, 3   # 8 A[3]
    add $t2, $t2, $t1
    add $t2, $t2, $t1
    add $t2, $t2, $t1  # 11 A[3]
    sll $t1, $t0, 4    # 16 A[2]
    add $t1, $t1, $t0
    add $t1, $t1, $t0
    add $t1, $t1, $t0
    add $t1, $t1, $t0  # 20 E A[2]
    sub $t1, $t2, $t1
    addi $t1, $t1, -100
    sw $t1, 20($s4)

Exit:
```

(ii)

```
add   $s1,  $zero,  $zero.      # i=0
Loop:
      slt $to,$s1,  $s2
      beq   $to,    $zero,  Exit.
       sll   $t1,   $s1, 2
       add   $t1,   $t1,   $so   # Mem address of A[i]
       lw    $t2,  0($t1)  #   A[i]
       sll   $t2,   $t2,  2.
       add   $t2,   $t2,   $so.
       ~~sw  $to, 0($t2)~~
       lw    $to,  0($t2)  #   A[A[i]]
       ~~sll  $t2,  $to, 4~~
       sll   $t2,   $to, 4.
       add   $t2,   $t2,   $to.   # If A[i]
       sw    $t2    0   ($t1)
      addi   $s1,   $s1, 1.
       j Loop:
Exit:
```



(c)

(i)

branch address = PC+4 + (Constant x 4)

= 4400040 + 4 + (600 x 4)

= (4400 1844)$_{16}$

-1

(ii)

Jump address = (PC+4)'s MSB bit concated with (Constant x 4)

∴ PC+4's MSB 4 bit = 0100

∴ Constant x 4 = ~~0000 1000 0000 0000 00~~

= 00 0000 0000 0000 1000 0000 0000 00

∴ Jump address = 0100 00 0000 0000 0000 1000 0000 0000 00

-1

= (4000 2000)$_{16}$

Ans to question no 3

(a)

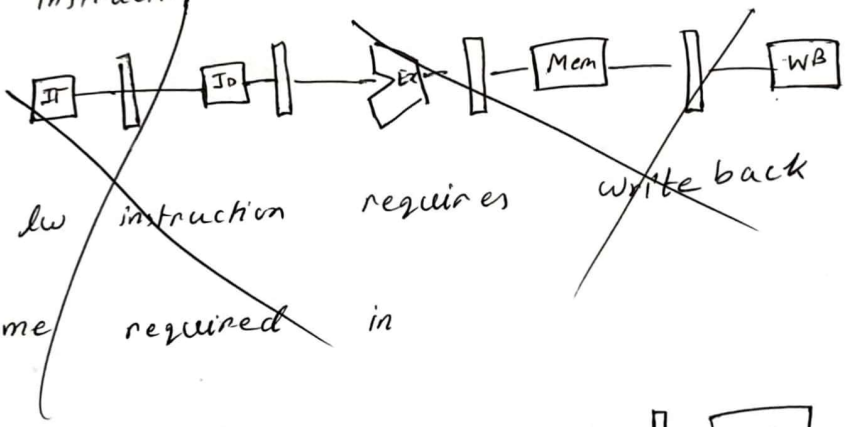
Memory operation = 65 ps.

register " = 33 ps.

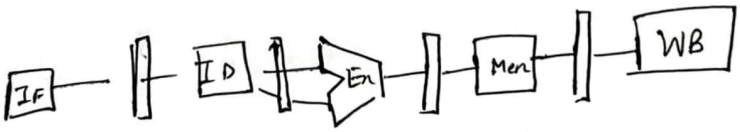
Combinational logic stage = 52 ps.

An, Memory operation takes more time so, clock period for single cycle datapath would be = 65 ps.

lw instruction



∴ An, lw instruction requires write back so, time required in



lw

sw.

∴ in single cycle datapath time required.

~~(65+33+52) x 2~~ ps

= (65 x 5) x 2 ps

= 650 ps

in pipelined stage.

lw

sw

∴ in pipelined stage time required.

∴ = (65 × 5) +

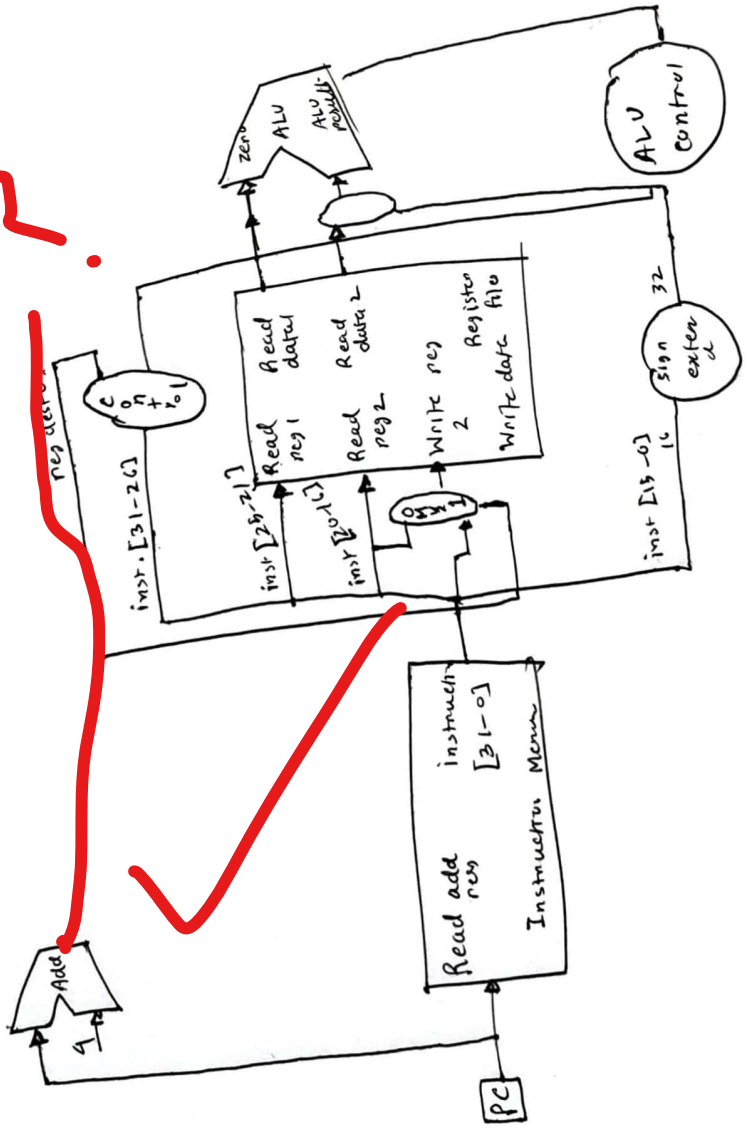
= 390 ns.

(b)

bne $10, $11, 1024

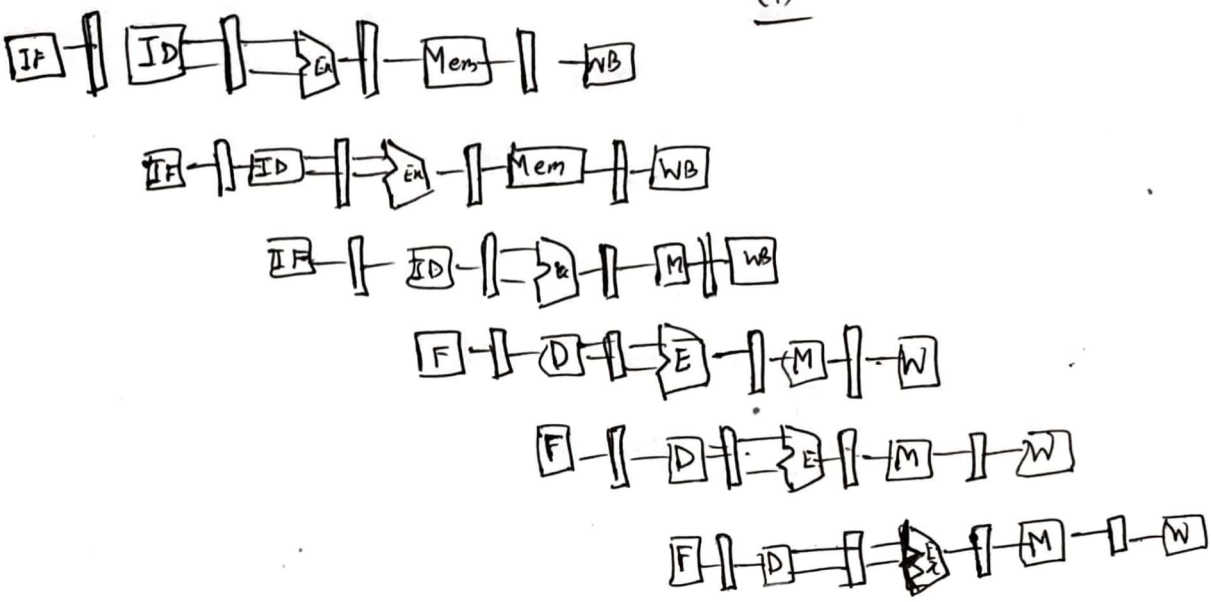
-0.5

2.



(a)

(i)



∴ Clock Cycles = 10

∴ Total time = (65 × 5) + (65 × 5)

= 650 ps

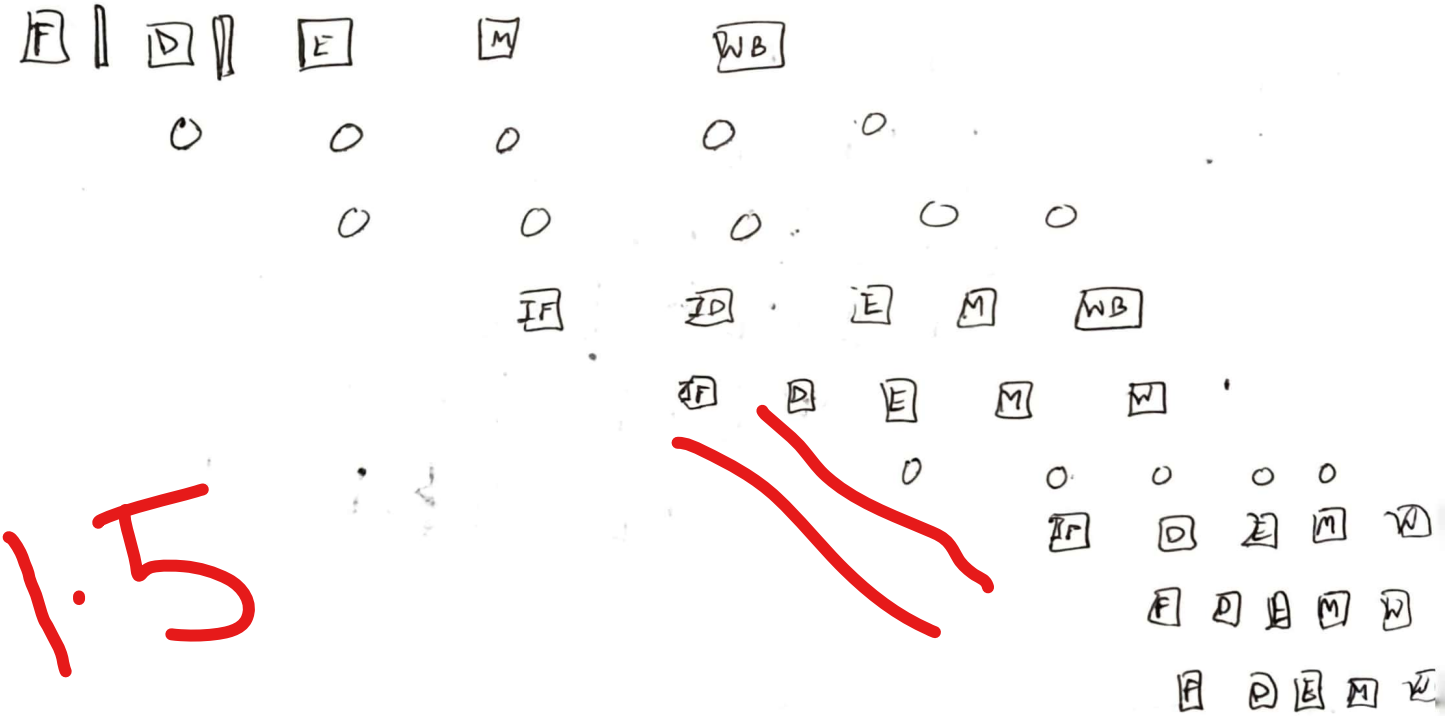
∴ CPI = $\frac{10}{6}$ = 1.67

(ii)

There are two data hazard in code sequence two and code sequence four.

-0.5

(h1)



-1.5

Clock Cycle = 13 X 17

∴ CPI = $\frac{13}{6}$ = 2.17

3c)-4