Slide - 29

$$P = \frac{1}{E.T}$$

Computer A:

Clock Rate = 2GHz

CPU Time = 10s

Computer B:

CPU Time = 6s

Clock Cycle = 1.2

$$\text{Clock Rate} = \frac{\text{clock Cycles}}{\text{CPU Time}}$$

Computer A:

Clock Cycles = CPU Time x Clock Rate

Clock Cycles = Instruction Count x Cycles per Instruction

CPU Time = Instruction Count x CPI x clock cycle time

$$= \frac{\text{Instruction Count} \times \text{CPI}}{\text{Clock Rate}}$$

Computer A : Cycle Time = 250 ps ,
CPI = 2.0

Computer B : Cycle Time = 500 ps ,
CPI = 1.2

Same ISA (Instruction Count = 1)

$$\frac{P_A}{P_B} = \frac{E_B}{E_A}$$

CPU Time = Instruction Count x CPI x Cycle time

$$\frac{\text{CPU Time}_B}{\text{CPU Time}_A}$$

$$\text{clock cycles} = \sum_{i=1}^{n} (\text{CPI}_i \times \text{Instruction}_i)$$

$$\text{CPI} = \frac{\text{Clock Cycles}}{\text{Instruction Count}}$$

$$= \sum_{i=1}^{n} \left(CPI_i \times \underbrace{\frac{\text{Instruction Count}_i}{\text{Instruction Count}}}_{\text{Relative Frequency}} \right)$$

1 → add → 2 → 3 cycles / ins.
2 → sub → 5 → 2 cycles / ins.
3 → mult → 3 → 5 cycles / ins.

$\overline{10}$

$$= \frac{\overbrace{(2\times3)+(5\times2)+(3\times5)}^{\text{Total Clock Cycle}}}{10}$$

$n = 3$

Class	A	B	C
CPI for class	1	2	3
IC in seq. 1	2	1	2
IC in seq. 2	4	1	1

Seq 1: IC = 5
Clock Cycles
$= 2\times1 + 1\times2 + 2\times3$
$= 10$

Seq 2: IC = 6
Clock Cycles
$= 4\times1 + 1\times2 + 1\times3$
$= 9$

Avg. CPI = 10/5 = 2 | Avg. CPI = 9/6 = 1.5

$$\text{CPU Time} = \frac{\text{Instruction}}{\text{Program}} \times \frac{\text{Clock cycles}}{\text{Instruction}} \times \frac{\text{Seconds}}{\text{Clock cycle}}$$

$$\text{Power} = \text{Capacitive load} \times \text{Voltage}^2 \times \text{Frequency}$$

Power ↓ ×30

Voltage ↓ 5V – 1V

Frequency ↓ ×1000

Slide 39, 40, 41, 44, 45 – নেই

$$\text{Spec Ratio} = \frac{\text{Reference Time}}{\text{Execution Time}}$$

Geometric Mean:

$$\sqrt[n]{\prod_{i=1}^{n} \text{Execution time ratio}_i}$$

Amdahl's Law

$$T_{improved} = \frac{T_{affected}}{\text{improvement factor}} + T_{uneffected}$$

$$\text{Execution Time} = T_{affected} + T_{unaffected}$$

multiply accounts for 80s/100s

$$\underset{100s}{\text{Execution Time}} = \underset{80s}{T_{affected}} + \underset{20s}{T_{unaffected}}$$

$$T_{improved} = \frac{T_{affected}}{\text{improvement factor}} + T_{uneffected}$$

$$100 \times 5\% = \frac{80}{n} + 20$$

$$20 = \frac{80}{n} + 20$$

$\frac{80}{n} = 0$ X Can't be done

$$MIPS = \frac{\text{Instruction count}}{\text{Execution time} \times 10^6}$$

$$= \frac{\text{Instruction count}}{\frac{\text{Instruction} \times CPI}{\text{Clock Rate}} \times 10^6}$$

$$= \frac{\text{Clock Rate}}{CPI \times 10^6}$$

The Von Neumann Model

The Harvard Architecture

CISC / RISC

MIPS follow RISC.