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Department of Computer Science and Engineering
MAKEUP FINAL EXAMINATION
Fall 2020
CSE 340: Computer Architecture

Total Marks: 60 Time Allowed: 2.00 Hours

Name: _____ ID: _____ Section: _____

1.	a.	In MIPS we have two types of branching, conditional and unconditional. In both cases, we have to consider the address stored in the program counter (PC). Assume that Program Counter (PC) holds the value 0x12220000. If offset value is 66, then calculate the conditional and unconditional branch target.	4

	b.	Consider the C code given below. Variable i is represented by 4-bit (ABCD). So, for example i=0 is represented as A=0, B=0, C=0, and D=0, where A is the MSB and D is LSB. Draw the truth table considering the below C code, perform a sum of product simplification of z, and design the circuit for the simplified expression.
		int i,x=1,y=1,z=0;
		for(i=0;i<16;i++){
		x=x+y+i;
		y=3*i;
		if(x%7==0||y%5==0)
		z=1;
		else
		z=0;}
			6

2		Consider the below C code segment. Convert the given segment into MIPS assembly code. Consider that x, y and z, i are in registers $f0 and $t0 and $f1, $t1 respectively. Base address of A is in register $s0. [Please note: do not use mult instruction to perform the multiplication]
		For (i=0;i<10;i++){
		(float) x =(int) y+(float) z;
		(int) y = (float) x+ (float) z;
		float (z)= (int) y+(float) z; A[i]=(float) z+2*(int) y;
			10

3		Consider the below set of instructions. Identify the data hazards and overcome the hazards using all the available methods. Your answer should contain all the necessary diagrams, required total cycle count in each solution along with average CPI.
		Add \$10,\$11,\$12
		Add \$13,\$10,\$11
		Sub \$7,\$13,\$6
		Lw \$8,40(\$7)
		Sll \$3,\$8,2
		Addi \$11,\$9,\$6
			10

4.	a.	Let's assume in a pipeline execution, two instructions are trying to access the RAM in the same clock cycle for performing two different operations. What are those operations, what situation can arise because of those operations and how that situation can be handled?	2
	b.	Design a PLA for the expressions: i. $y_1 = X'YZ' + XY'Z + XYZ$ ii. $y_2 = XY'Z' + X'YZ' + XY'Z$ iii. $y_3 = X'Y'Z' + XY'Z + X'YZ$	4
	c.	Suppose you are designing a direct mapped cache with 256 blocks (with 16-bit addresses) where each block is of size 16 bytes. What is the size of the tag field in bits in the address? To what block number does address 1500 map? What would be the miss ratio if, among 30 accesses, there were 10 hits?	4

THE END