

Stage 2

Divyanshu Pabia - RA2111003011373

The epwaves shown are the result of the testbench that I have submitted along with my code in this zip file. I have tested my design on the two test examples given to us. I would have tested extensively on more examples, but sadly I couldn't get the time to do so, as my minors finished just one day before the deadline. Also, I would request that this assignment uses my credit day of the last assignment.

Design Description:

In my main processor.vhd file, I have 8 components, namely – Program counter, Register File, Data Memory, Program Memory, ALU, Flag updater, Condition checker, Decoder. I have attached their synthesis reports below. All these components have been instantiated under the processor architecture. The data path signals flow through them. The control signals are given to the processor by the decoder. The last control signal Psrc, is given by the condition checker. I have simulated and synthesized on edaplayground.com

The design works up to the expectation and nothing has been hardcoded. I have attached the epwave outputs of as many signals as I could/are relevant. I have given a looped clock input of 25 iterations for this stage. I will add a reset signal in further stages. The PW control signal that I have declared is redundant in this stage.

Synthesis Reports:

0. Processor

Device Utilization for 7A100TCSG324

```
# Info: *****
# Info: Resource                Used    Avail    Utilization
# Info: -----
# Info: I/Os                    1       210      0.48%
# Info: Global Buffers          0        32      0.00%
# Info: LUTs                     0     63400      0.00%
# Info: CLB Slices               0     15850      0.00%
# Info: Dffs or Latches          0    126800      0.00%
# Info: Block RAMs               0       135      0.00%
# Info: DSP48E1s                 0       240      0.00%
# Info: -----
# Info: *****
```

Info: Library: work Cell: processor View: behavior

```
# Info: *****
# Info: Number of ports : 1
# Info: Number of nets : 0
# Info: Number of instances : 0
# Info: Number of references to this view : 0
# Info: Total accumulated area :
# Info: Number of gates : 0
# Info: Number of accumulated instances : 0
# Info: *****
```

IO Register Mapping Report

```
# Info: *****
# Info: Design: work.processor.behavior
# Info: +-----+-----+-----+-----+-----+
# Info: | Port      | Direction | INFF  | OUTFF | TRIFF |
# Info: +-----+-----+-----+-----+-----+
# Info: | clock     | Input    |       |       |       |
# Info: +-----+-----+-----+-----+-----+
# Info: Total registers mapped: 0
```

Netlist:

```
//
// Verilog description for cell processor,
// Sun Feb 20 13:05:04 2022
//
// Precision RTL Synthesis, 64-bit 2021.1.0.4//

(* PSEUDO_BBOX = "1" *)
module processor ( clock ) ;

input clock ;

endmodule
```

1. Condition Checker:

Device Utilization for 7A100TCSG324

```
# Info: *****
# Info: Resource                Used    Avail    Utilization
# Info: -----
# Info: IOs                    14      210      6.67%
# Info: Global Buffers         1       32       3.12%
# Info: LUTs                   1      63400    0.00%
# Info: CLB Slices             1     15850    0.01%
# Info: Dffs or Latches        1     126800   0.00%
# Info: Block RAMs             0       135     0.00%
# Info: DSP48E1s               0       240     0.00%
# Info: -----
# Info: *****
# Info: Library: work    Cell: condition    View: rtl
# Info: *****
# Info: Number of ports :                14
# Info: Number of nets :                 17
# Info: Number of instances :            11
# Info: Number of references to this view :      0
# Info: Total accumulated area :
# Info: Number of Dffs or Latches :          1
# Info: Number of LUTs :                  1
# Info: Number of Primitive LUTs :          1
# Info: Number of accumulated instances :     11
```

2. Data Memory

Device Utilization for 7A100TCSG324

```
# Info: *****
# Info: Resource                Used    Avail    Utilization
# Info: -----
# Info: IOs                    75      210     35.71%
# Info: Global Buffers         1       32      3.12%
# Info: LUTs                   32     63400    0.05%
# Info: CLB Slices              8     15850    0.05%
# Info: Dffs or Latches         0     126800    0.00%
# Info: Block RAMs              0       135     0.00%
# Info: Distributed RAMs
# Info:   RAM64X1S             32
# Info: DSP48E1s               0       240     0.00%
# Info: -----
# Info: *****
# Info: Library: work    Cell: DM    View: BEV
# Info: *****
# Info: Number of ports :                75
# Info: Number of nets :                150
# Info: Number of instances :            76
# Info: Number of references to this view :    0
# Info: Total accumulated area :
# Info: Number of LUTs :                32
# Info: Number of Primitive LUTs :       32
# Info: Number of LUTs as Distributed RAM : 32
# Info: Number of accumulated instances :   107
```

3. ALU

Device Utilization for 7A100TCSG324

```
# Info: *****
# Info: Resource                Used    Avail    Utilization
# Info: -----
# Info: IOs                    114     210     54.29%
# Info: Global Buffers         0       32      0.00%
# Info: LUTs                   201    63400    0.32%
# Info: CLB Slices             27    15850    0.17%
# Info: Dffs or Latches        0    126800    0.00%
# Info: Block RAMs             0      135     0.00%
# Info: DSP48E1s               0      240     0.00%
# Info: -----
# Info: *****
# Info: Library: work    Cell: alu    View: rtl
# Info: *****
# Info: Number of ports :                114
# Info: Number of nets :                493
# Info: Number of instances :            381
# Info: Number of references to this view :      0
# Info: Total accumulated area :
# Info: Number of LUTs :                201
# Info: Number of Primitive LUTs :        233
# Info: Number of LUTs with LUTNM/HLUTNM :      64
# Info: Number of MUX CARRYs :           64
# Info: Number of accumulated instances :    478
```

4. Program Counter:

Device Utilization for 7A100TCSG324

```
# Info: *****
# Info: Resource                Used    Avail    Utilization
# Info: -----
# Info: IOs                    58      210     27.62%
# Info: Global Buffers         1       32       3.12%
# Info: LUTs                   90     63400     0.14%
# Info: CLB Slices             23     15850     0.15%
# Info: Dffs or Latches        30     126800     0.02%
# Info: Block RAMs             0       135      0.00%
# Info: DSP48E1s               0       240      0.00%
# Info: -----
# Info: *****
# Info: Library: work    Cell: pc    View: rtl
# Info: *****
# Info: Number of ports :                    58
# Info: Number of nets :                   326
# Info: Number of instances :                300
# Info: Number of references to this view :      0
# Info: Total accumulated area :
# Info: Number of Dffs or Latches :           30
# Info: Number of LUTs :                     90
# Info: Number of Primitive LUTs :            90
# Info: Number of MUX CARRYs :                59
# Info: Number of accumulated instances :      300
```

5. Decoder:

Device Utilization for 7A100TCSG324

```
# Info: *****
# Info: Resource                Used    Avail    Utilization
# Info: -----
# Info: IOs                    146     210     69.52%
# Info: Global Buffers         1       32      3.12%
# Info: LUTs                   25     63400   0.04%
# Info: CLB Slices              3     15850   0.02%
# Info: Dffs or Latches        17     126800  0.01%
# Info: Block RAMs             0       135     0.00%
# Info: DSP48E1s               0       240     0.00%
# Info: -----
# Info: *****
# Info: Library: work    Cell: Decoder    View: Behavioral
# Info: *****
# Info: Number of ports :                146
# Info: Number of nets :                229
# Info: Number of instances :            197
# Info: Number of references to this view :      0
# Info: Total accumulated area :
# Info: Number of Dffs or Latches :        17
# Info: Number of LUTs :                 25
# Info: Number of Primitive LUTs :        31
# Info: Number of LUTs with LUTNM/HLUTNM :    12
# Info: Number of accumulated instances :    197
```

6. Instruction Memory:

Device Utilization for 7A100TCSG324

```
# Info: *****
# Info: Resource                Used    Avail    Utilization
# Info: -----
# Info: IOs                    38      210     18.10%
# Info: Global Buffers         0       32      0.00%
# Info: LUTs                   12     63400    0.02%
# Info: CLB Slices              2     15850    0.01%
# Info: Dffs or Latches         0     126800   0.00%
# Info: Block RAMs              0       135     0.00%
# Info: DSP48E1s               0       240     0.00%
# Info: -----
# Info: *****
# Info: Library: work    Cell: IM    View: BEV
# Info: *****
# Info: Number of ports :                      38
# Info: Number of nets :                      59
# Info: Number of instances :                  53
# Info: Number of references to this view :      0
# Info: Total accumulated area :
# Info: Number of LUTs :                      12
# Info: Number of Primitive LUTs :            14
# Info: Number of LUTs with LUTNM/HLUTNM :      4
# Info: Number of accumulated instances :       53
```


7. Register File

Device Utilization for 7A100TCSG324

```
# Info: *****
# Info: Resource                Used    Avail    Utilization
# Info: -----
# Info: IOs                    110     210     52.38%
# Info: Global Buffers         1       32       3.12%
# Info: LUTs                   48     63400    0.08%
# Info: CLB Slices             12     15850    0.08%
# Info: Dffs or Latches        0      126800    0.00%
# Info: Block RAMs             0       135     0.00%
# Info: Distributed RAMs
# Info:   RAM32M               10
# Info:   RAM64M                2
# Info: DSP48E1s               0       240     0.00%
# Info: -----
# Info: *****
# Info: Library: work    Cell: RF    View: BEV
# Info: *****
# Info: Number of ports :                110
# Info: Number of nets :                220
# Info: Number of instances :            111
# Info: Number of references to this view :      0
# Info: Total accumulated area :
# Info:   Number of LUTs :                48
# Info:   Number of Primitive LUTs :        48
# Info:   Number of LUTs as Distributed RAM :    48
# Info:   Number of accumulated instances :    123
```

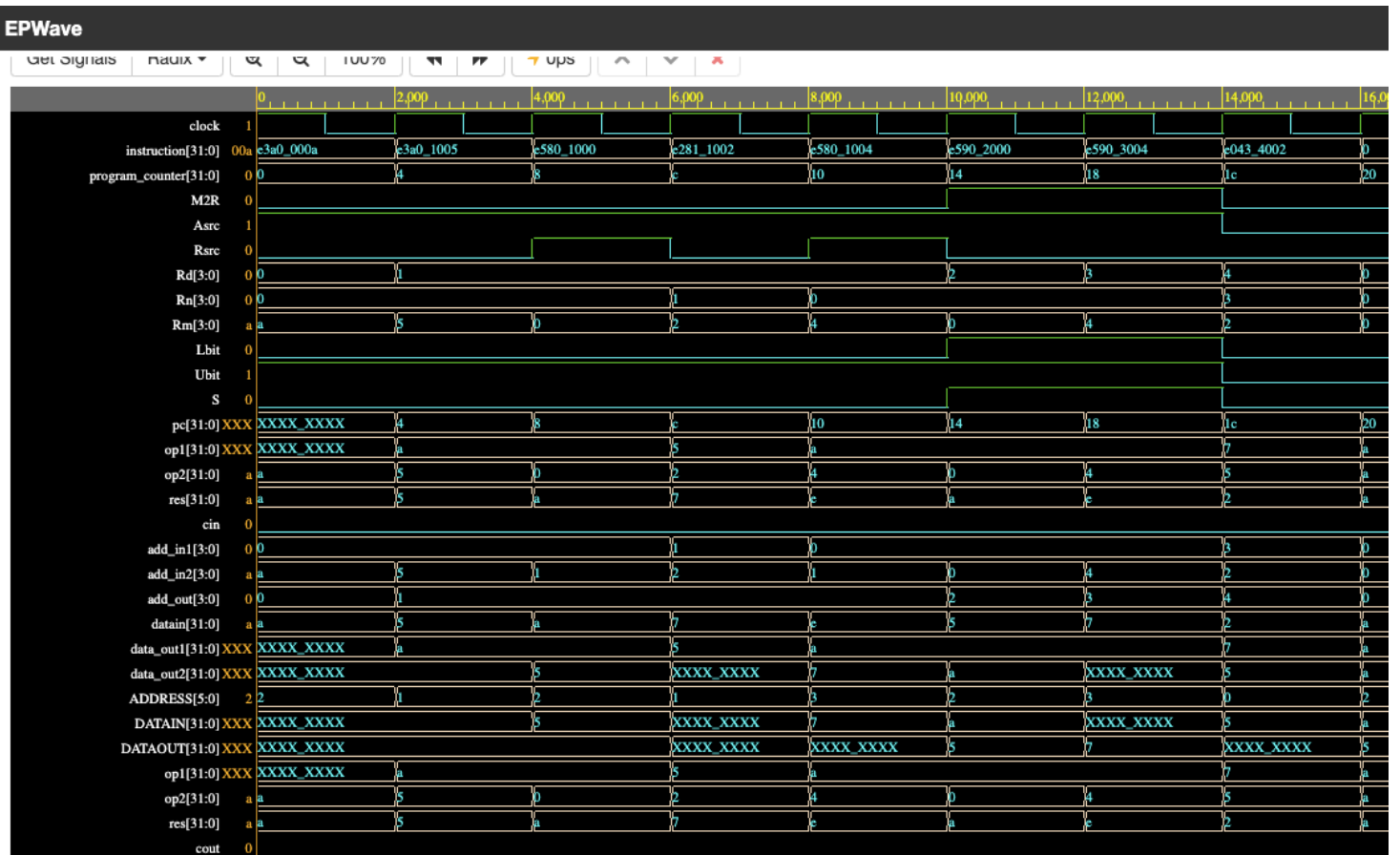
8. Flag Updater

Device Utilization for 7A100TCSG324

```
# Info: *****
# Info: Resource                Used    Avail    Utilization
# Info: -----
# Info: I0s                     119     210     56.67%
# Info: Global Buffers          1       32       3.12%
# Info: LUTs                    11     63400    0.02%
# Info: CLB Slices              2     15850    0.01%
# Info: Dffs or Latches         4     126800    0.00%
# Info: Block RAMs              0       135     0.00%
# Info: DSP48E1s                0       240     0.00%
# Info: -----
# Info: *****
# Info: Library: work    Cell: flags    View: rtl
# Info: *****
# Info: Number of ports :                119
# Info: Number of nets :                127
# Info: Number of instances :            74
# Info: Number of references to this view :    0
# Info: Total accumulated area :
# Info: Number of Dffs or Latches :        4
# Info: Number of LUTs :                11
# Info: Number of Primitive LUTs :        12
# Info: Number of LUTs with LUTNM/HLUTNM :    2
# Info: Number of accumulated instances :    74
```

Test Cases and Output:

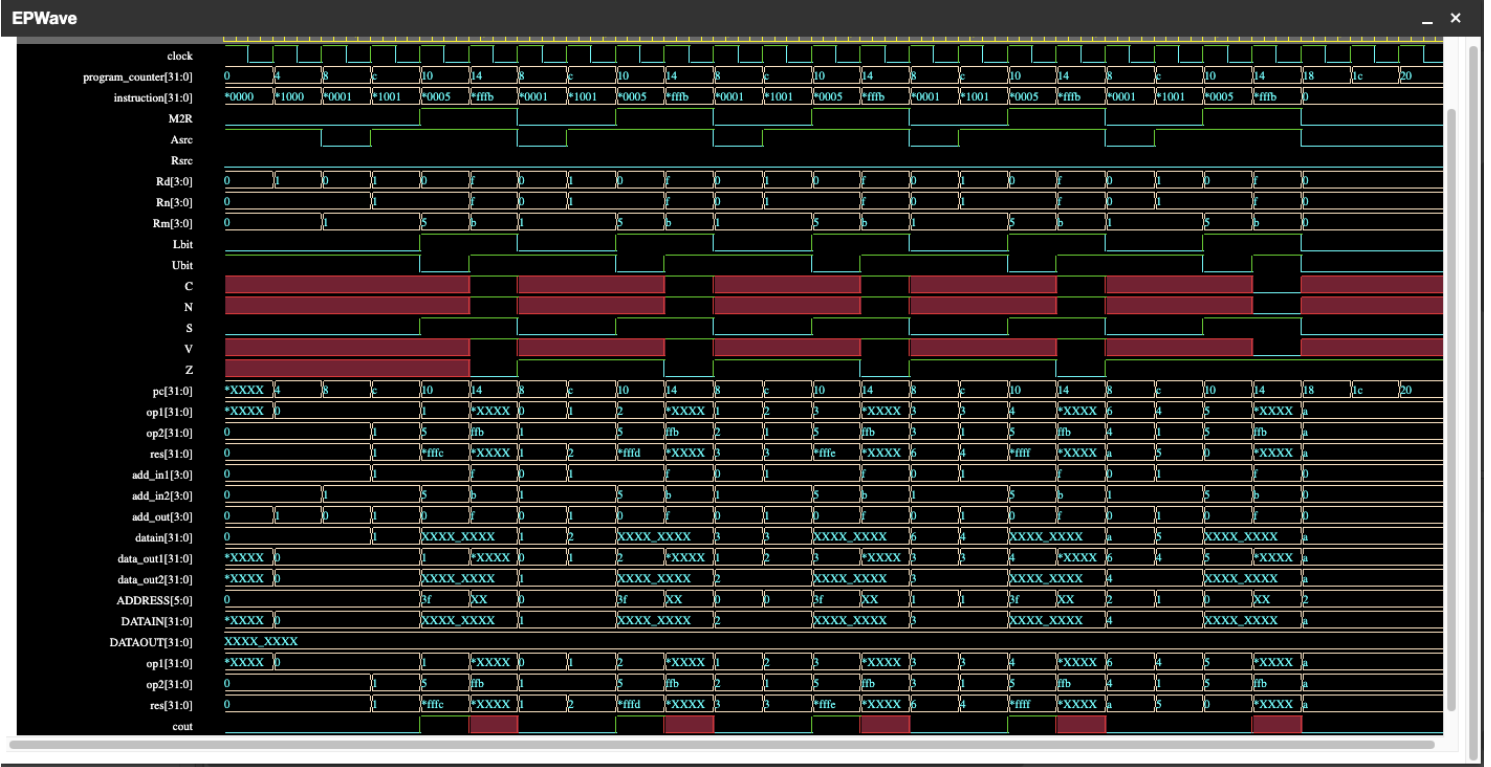
1. Here is the epwave output of the first example program:



Description: If we take a look at the datain[31:0] port, it shows the values that are being fed to the Register File. The port just above it, shows the address of the register to which the data is going to be written. To show that the program has been executed correctly, it is enough to see that at the end of the instructions, datain[31:0] = 2 and add_out[31:0] = 4. This means that $r4 = 2$ at the end which is actually true, since $r3 = 7$ and $r2 = 5$, $r3 - r2 = 2$. The names of the other ports are self-explanatory and can be verified.

(The program should have $r0 = 8$ initially instead of 10)

2. The epwave output of the second test program:



In this, the program will run 5 times until r1 reaches 0. ($r1 = -4, -3, -2, -1, 0$). To see the incremented values of r1 in each iteration, we can take a look at the datain[31:0] ports each time the program_counter is at "c". In the port above it, '1' represents that $r1 = \text{datain}$. The program branches back to instruction 8 4 times before exiting. To do this, the condition checker component has been used, which uses the signed branch offset to decide the instruction to go to. All the flag updations can be verified in this epwave.