University of Jeddah College of Computer Science and Engineering Department of Computer & Network Engineering		جامعة جدة كلية علوم و هندسة الحاسب قسم هندسة الحاسب و الشبكات

CCCN212 : Digital logic design
Assignment#2 CLO2.1
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Question 1: Flip Flop

Consider the following flip flop

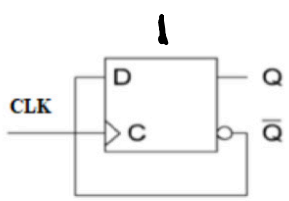


Fig1

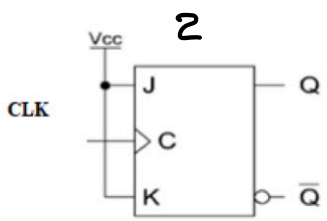


Fig2

1. Give the name of each flip flops used in the fig1 and fig2

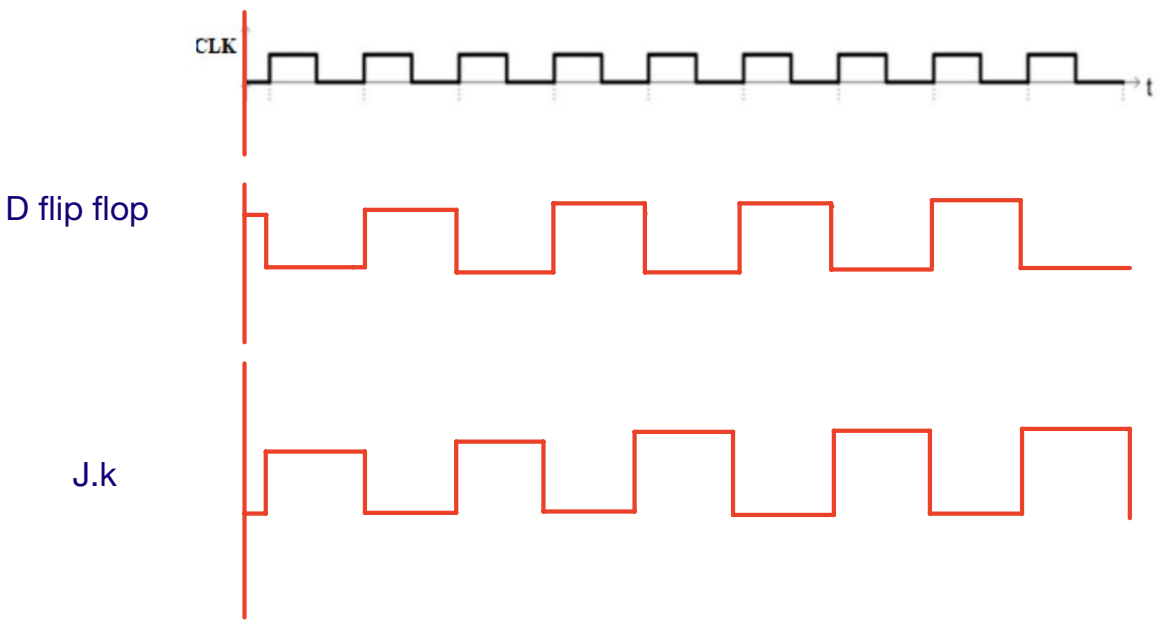
1-The first one is D flip flop
2-j-k flip flop

2. Give the timing diagram for each circuit considering the signal CLK

Qis+ The truth table of the D flip flop:

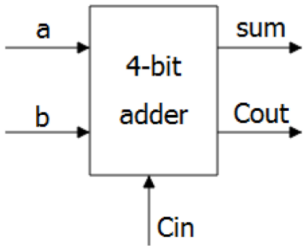
CLK	D	Q
↑	0	0
↑	1	1
0	0	not change
0	1	not change

So in the case D=$\overline{Q}$ and in the fig 2 we know that j=k=VCC =1
So the timing diagram is



Question2: BCD adder

Consider a 4 bit Adder given the following figure, where A and B are 4 bit numbers:



1- Dress the corresponding truth table
2- To realize a BCD adder, we need to:

- Step1: First add the two binary numbers A and B
- Step2: If the sum is less or equal than 9, then the value of BCD sum and binary sum will be the same otherwise we will add 6 (0110 in binary)

a) Dress the truth table for the BCD sum (from decimal numbers 0 to 15)
b) Give the conditions from the truth table where we need to add 6 to the binary sum? Give a logic equation
c) Design a BCD adder using two 4 bits' adder and gate AND and OR

1)

A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1 Yea

Q2)

a)

To make a truth table for BCD sum ,we need to consider the decimal number from 0 to 15 and determine their corresponding BCD sum .the BCD sum is a 4-bit number ,so we will have four output columns for the BCD sum bits (S3,S2,S1,S0)