Q2:

Include answers to the following questions in your written report:

* List the reported Fmax of your design after pipelining.

Fmax = 72.06 MHZ

* List the cycle time of your design after pipelining. Show your work.

CT = 1 / 72.06 MHZ = 13.9 ns

* List the instruction count for miner\_tb from the ModelSim simulation after pipelining.

IC: 193729

* List the cycle count for miner\_tb from the ModelSim simulation after pipelining.
* CC: 204668
* Compute the CPI and execution time (# of cycles x cycle time) after pipelining.

CPI = CC/IC = 204668/193729 = 1.06

ET = CC \* CT = 192729 \* 13.9 ns = 2678933.1ns

* List the number of registers used, the number of combinational functions used, and the number of memory bits used after pipelining.

What is your speedup (baseline execution time/optimized execution time)? See [FAQ](https://docs.google.com/document/d/16ryDES9L5L2vk7V0K0EEo5MZzPLvDCKLxxiU_jabscU/edit#heading=h.okyrfwxw6jdk) for clarifications on speedup.

#registers = 230

#combinational functions = 1606

#memory bits = 20480

speedup = BET/OET = 3355909.218 ns /2678933.1ns = 1.253