**Homework 2**

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**Problem 1**

According to the problem description, we know that cache block size is 64B, so block offset is 6 bits. Total cache size is 512B, so we can calculate that there are 512B / 64B = 8 blocks. In view of 2-way set associative, the number of sets is 8 / 2 = 4, which can be represented by 2 bits. Note that the address space is 20 bits, therefore, we can use 20-6-2 = 12 bits as a tag.

Trace:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Address** | **Tag bits** | **Index bits** | **Block offset bits** | **Result** |
| 0xABCDE | 101010111100 | 11 | 011110 | Miss |
| 0x14327 | 000101000011 | 00 | 100111 | Miss |
| 0xDF148 | 110111110001 | 01 | 001000 | Miss |
| 0x8F220 | 100011110010 | 00 | 100000 | Miss |
| 0xCDE4A | 110011011110 | 01 | 001010 | Miss |
| 0x1432F | 000101000011 | 00 | 101111 | Hit |
| 0x52C22 | 010100101100 | 00 | 100010 | Miss |
| 0xABCF2 | 101010111100 | 11 | 110010 | Hit |
| 0x92DA3 | 100100101101 | 10 | 100011 | Miss |
| 0xF125C | 111100010010 | 01 | 011100 | Miss |

Final cache content:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Set #** | **Way 0** | | | **Way 1** | | |
| **Valid** | **Tag** | **Data** | **Valid** | **Tag** | **Data** |
| 0 | 1 | 000101000011 | 0x14327 | 1 | 010100101100 | 0x52C22 |
| 1 | 1 | 111100010010 | 0xF125C | 1 | 110011011110 | 0xCDE4A |
| 2 | 1 | 100100101101 | 0x92DA3 | 0 | \ | \ |
| 3 | 1 | 101010111100 | 0xABCF2 | 0 | \ | \ |

**Problem 2**

1. AAT = 1 + 0.03\*(15 + 0.3\*300) = 4.15 cycles
2. AAT = 1 + 0.1\*(15 + 0.05\*300) = 4 cycles